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BIF-476W-043-70

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A PAYLOAD STUDY

FOR

MAIN BEAM COLLECTION (MBC)

SUBMITTED BY CONTRACTOR 476W

29 JULY 1970

Study which led to MABELE

"Competitor"

file.

J. C. de BROEKERT

Handle Via
BYEMAN
Control System Only

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1.0 INTRODUCTION

1.1 BACKGROUND

The overhead ELINT collection program has evolved from the simple payloads of the early sixties to the relatively sophisticated high accuracy emitter locating systems of today. Great studies have been made in improving payload measurement accuracies with corresponding advances in both on-board and ground based signal processing technology. The major upgrading effort has been directed, however, toward the class of collection systems which collect minor lobe radiation from target emitters, examples being the Bird Dog, Setter, Multigroup, Thresher and Reaper family; the P-11 pencil beam series such as SAMPAN, et al, and the high altitude programs.

On the other hand, the class of collection systems which receive radar main beam radiation, have received far less attention. Poppy has been upgraded (within the limitations of the down link), however, the P-11 main beam channels have, within recent years, been instead degraded to favor the minor lobe collection payload performance.

In view of these established trends, it is perhaps worthwhile to briefly examine the relative merits of main beam vs minor lobe collection systems. The advantages of minor lobe collectors are well known; these include high accuracy d-f, high intercept probability on emitters not illuminating the collection vehicle, and generally accurate frequency and PRI measurements.

Problem areas for minor lobe collectors include the inability to make measurements of emitter transmitted power, beam width and shape, scan patterns, and main lobe polarization. Since minor lobe radiated data are often perturbed by multipath, measurements of FMOP and pulse width are not infrequently distorted and unreliable. In some frequency ranges, heavily interleaved pulse trains or CW-like interference make processing difficult or impossible. Low PRF signals may be rejected by on board processing or payload frequency scan or antenna dwell time

limitations. These problem areas are exactly where the main beam concept can provide high quality data, including those items of great value to the SOI analyst.

The success of main beam collection in obtaining first intercept on new emitters is widely recognized. This success is no doubt in part due to the relative ease of processing low to moderate data-rate main beam collected data as contrasted to the difficulties inherent in deinterleaving the high density data collected by most minor lobe systems. The data output from main-beam collection systems, by virtue of lower average data rates, can be readily processed for low PRF emitters. This again points up the necessity of having a compatible collection-processing system which must be treated as a unified system in order to maximize the output flow of processed intelligence product.

1.2 GENERAL CONCEPT

The following report presents the system design of a main-beam collection payload with a substantially expanded signal parameter measurement capability compared to existing systems. This concept can provide all the basic radar signal parameter measurements, single pulse direction of arrival in azimuth and elevation, instantaneous frequency, PRF, pulse duration, precision TOA, antenna scan patterns, and ERP, which are required to define emitters, in a single payload.

This receiving system also provides a capability for handling both frequency jump and modulated PRF emitters which may be encountered in future environments. These may be extracted by sorting on direction-of-arrival in processing. The system also defines the beam patterns of multibeam and frequency scanned emitters and offers the possibility of being expanded to include a polarization measurement capability and a CW main beam intercept capability.

Although the basic concept can be applied to earth oriented stabilization, obtained either by gravity gradient, or gas or magnetic stabilization, this study was directed specifically to the use of a spinning P-11 vehicle using a horizon sensor to calculate the instan-

taneous rotation angle of the vehicle.

The vehicle will need to be of sufficient size to carry a payload consisting of receivers and collection antennas totaling approximately 100 lbs.

1.3 SCOPE OF STUDY

The concept of using a Main Beam Collection (MBC) System to satisfy the New Weapons Search requirements was described in Reference 1. Both an Amplitude-Monopulse and a Phase-Monopulse DF technique were studied and reported in Reference 1. The two approaches when considered together offered the possibility of covering the entire 50 MHz to 12 Gc frequency range.

The study described in this report expands on the Amplitude-Monopulse technique and describes in detail a Payload and Antenna System covering the 2 to 12 GHz frequency range. The payload was studied in depth and the critical circuit techniques investigated to further verify the feasibility of the payload.

2.0 GENERAL DESCRIPTION OF AMPLITUDE DF TECHNIQUE[1]

2.1 DIRECTION-FINDING ANTENNA CONFIGURATION

A reasonably detailed explanation of this antenna system is presented in Reference 1; a portion of that description will be repeated here for completeness.

2.1.1 Antenna Requirements

Since the receiving system requirements dictate monopulse direction-finding over a reasonably large aperature (120° cone), an array of broad beamwidth antennas such as shown in Figure 2-1 is proposed for making the DF and ERP measurements. The array shown will provide a 120° cone of coverage which rotates at the spin rate of the vehicle and is discussed in more detail in Section 2.2. The antennas are small (typically 2.5 in. x 2.5 in. at 2.0 GHz or higher frequencies) flat-spiral types which posses small boresight shifts, low axial ratios, reasonably constant beamwidths, and well behaved gain patterns to beyond 70° from boresight. A typical pattern for this type of antenna is shown in Figure 2-2. A more detailed description of the antenna characteristics, including a summary of data from measured patterns is presented below in Section 4.0.

2.1.2 Antenna Geometry

The six DF antennas are arranged in the pattern shown in Figure 2-1. The center antenna boresight coincides with the overall DF pattern boresight; the other five peripheral DF antenna boresights lie on the surface of a cone (half-angle of 64°) around the center antenna boresight. The antenna locations (or boresight angles) for the above model are based on the geometry of the regular icosahedron (the regular polyhedron with twelve vertices and twenty equilateral triangular faces). The center antenna has five neighboring antennas, each boresighted 64° from its own boresight; also, the angle between any two adjacent boresights of the peripheral antennas is 64°.

[1] Ref. 1 - [redacted] J. C. de Broekert "A MBC System Study (U)" Contract No. [redacted] November 1969 Stanford Electronics Laboratories, Stanford, California. (Report SECRET-E)

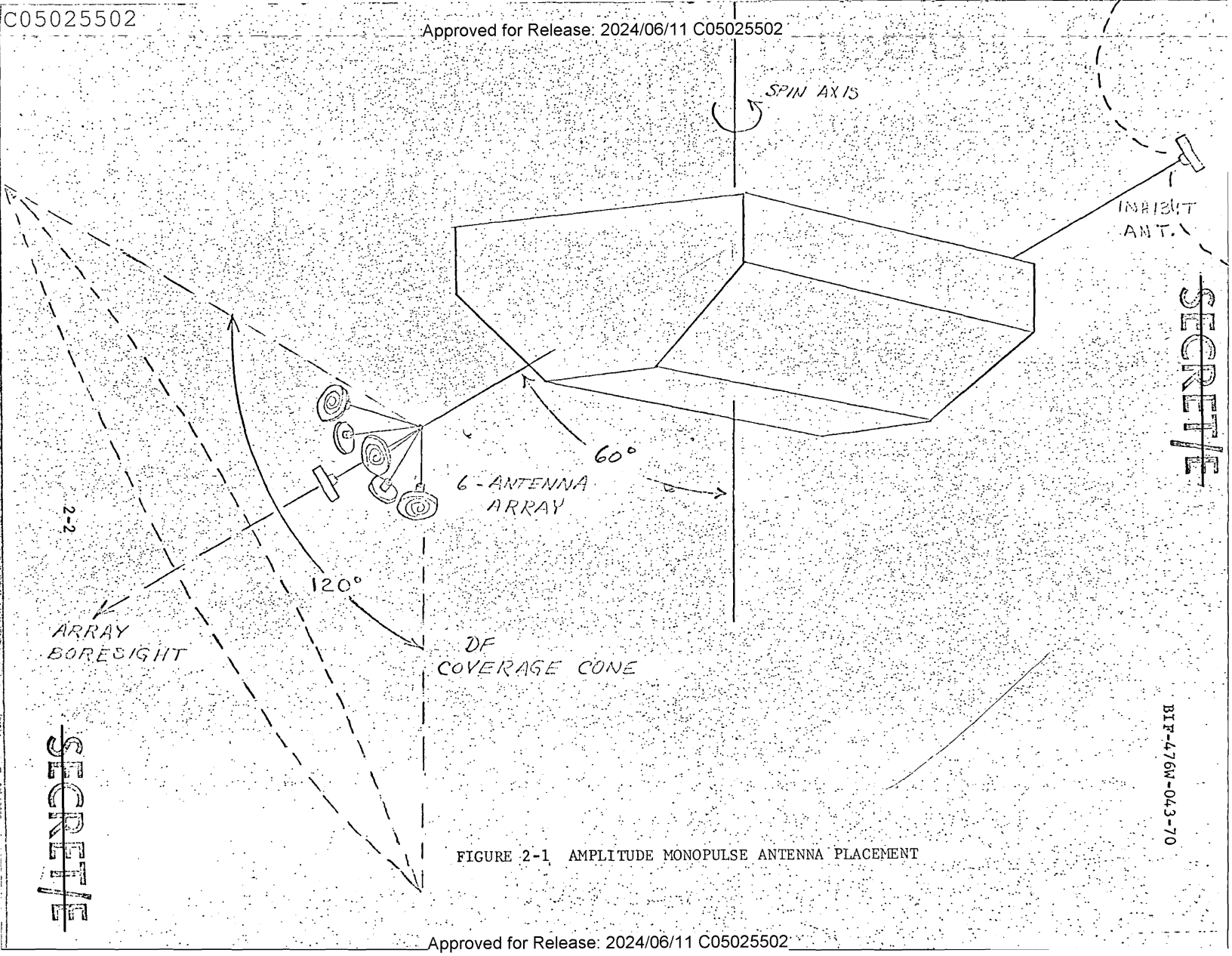

FIGURE 2-1 AMPLITUDE MONOPULSE ANTENNA PLACEMENT

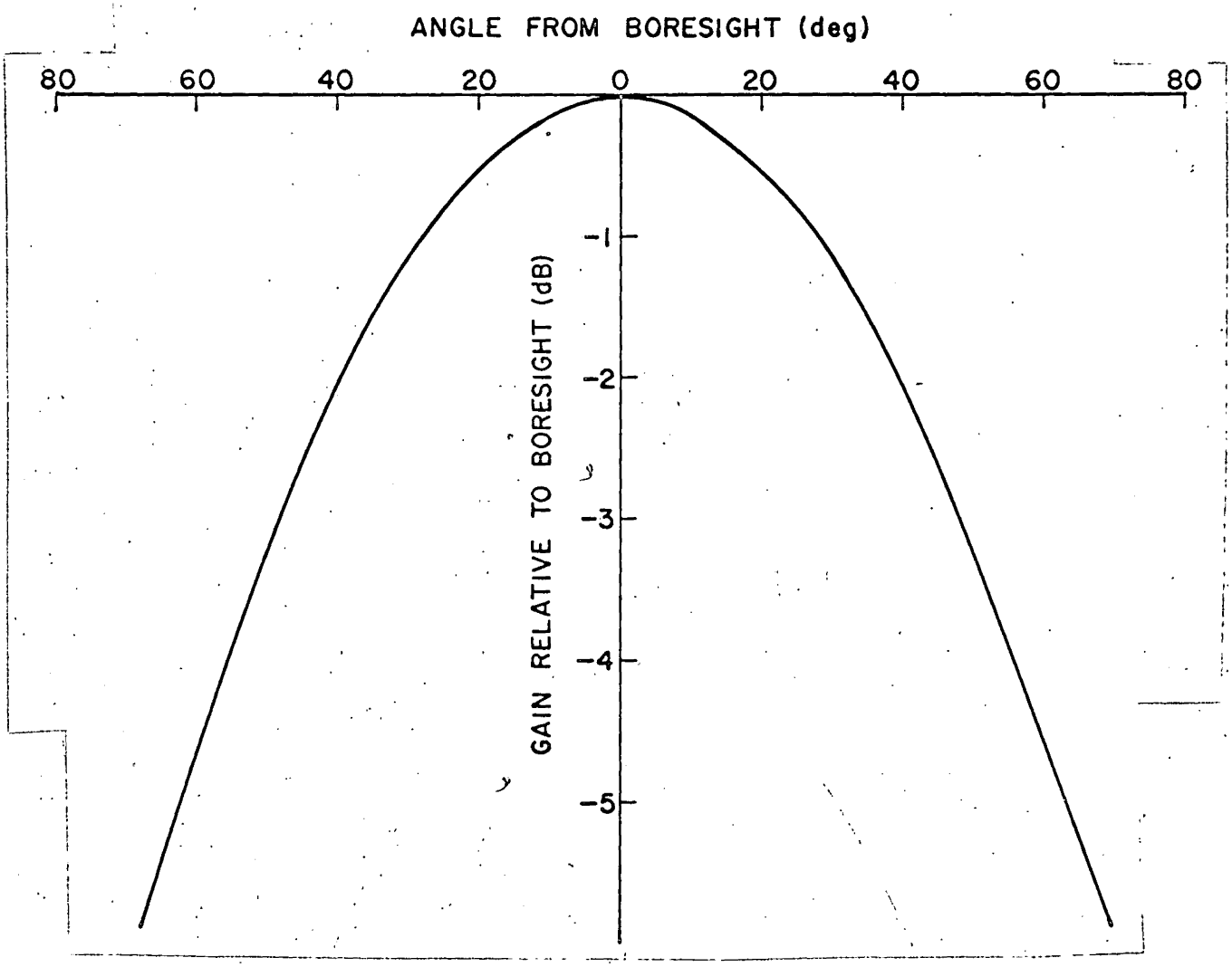

FIGURE 2-2 TYPICAL FLAT-SPIRAL GAIN PATTERN

2.1.3 DF Measurements

Coarse DF Measurements

Amplitude information from three of the six DF antennas is required to make the monopulse DF measurement. Figure 2-3 indicates that any three adjacent antennas define a face of the icosahedron (shown inscribed in the unit sphere) and it is evident that an arbitrary signal vector can be located at one of the existing five triangles (faces) by determining the three antennas with the highest amplitude signals. This determination is the basis for the coarse DF measurement. The signal vector can be further located to within a right triangle one-sixth the size of the large triangle by examining the relative amplitudes of antennas A_1, A_2 and A_3. For example, in Figure 2-3, the signal vector shown is located to the small triangle bcd by noting that $A_2 > A_1 > A_3$. Thus, the coarse DF measurement locates the signal vector to one of 30 triangular wedges of angular extent as indicated in Figure 2-4.

Fine DF Measurements

After locating the signal vector to a sector typical of that shown in Figure 2-4, the DF measurement can be further refined by taking amplitude ratios of the three highest amplitude antennas.

The point at which the signal vector shown in Figure 2-3 intersects the surface of triangle bcd could be used to specify its angle-of-arrival; therefore, it is useful to investigate lines, in the plane of triangle bcd, which represent contours of constant antenna gain ratio[2]. These contours, based on the antenna pattern of Figure 2-2, are plotted in Figure 2-5 for both A_2/A_1 and A_2/A_3; for the present example, A_2/A_1 = 3.15 dB and A_2/A_3 = 3.55 dB. If the ratios are quantized into discrete intervals (such as 0.5 dB in Figure 2-5) the number of intervals required will depend on the required resolution and expected system errors.

[2]Ref. 2 "Propogation and Electronic and Optical Techniques (U)"QPPR 7 and 8 and Final Report on Contract [redacted] 1 May through 31 October 1969. Stanford Electronics Laboratories, Stanford, California (Report SECRET)

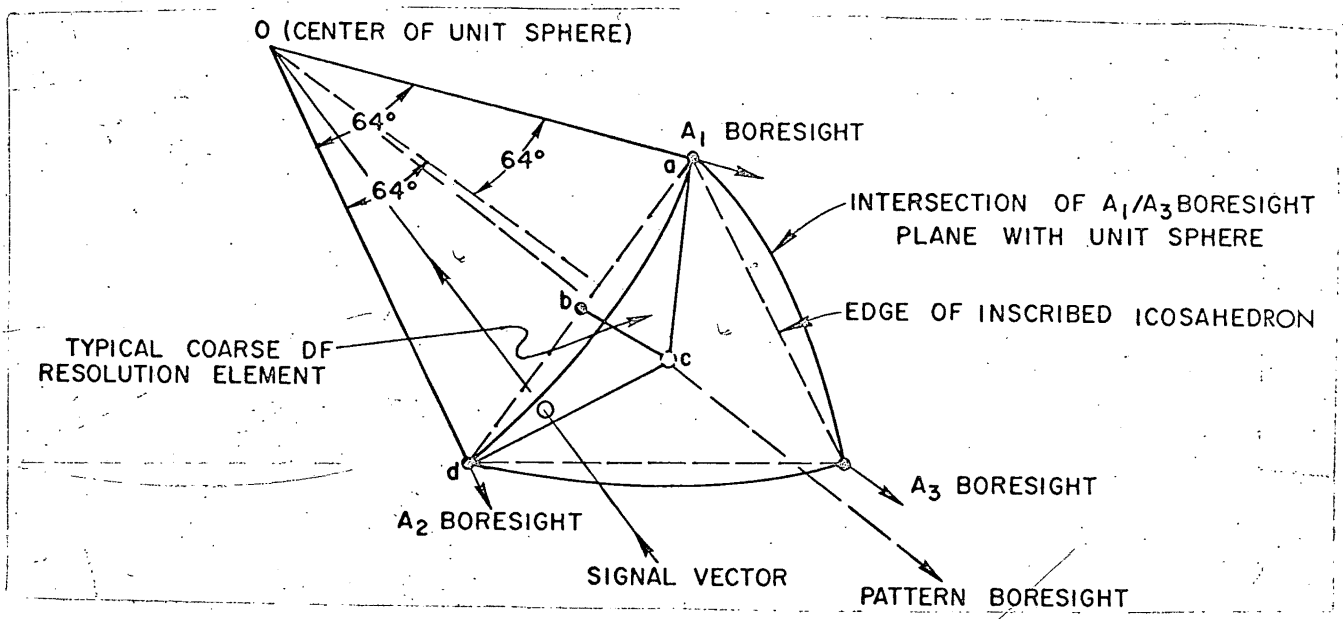

FIGURE 2-3 TYPICAL 3-ANTENNA ARRANGEMENT
(1 OF 5 IDENTICAL CONTIGUOUS PATTERNS COVERING 120° CONE)

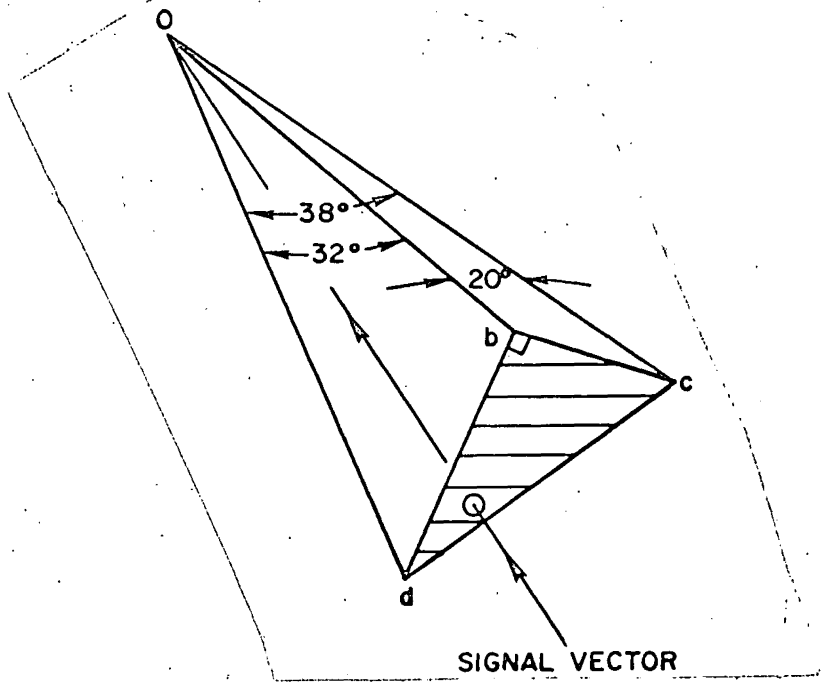

FIGURE 2-4 COARSE DF-RESOLUTION ELEMENT

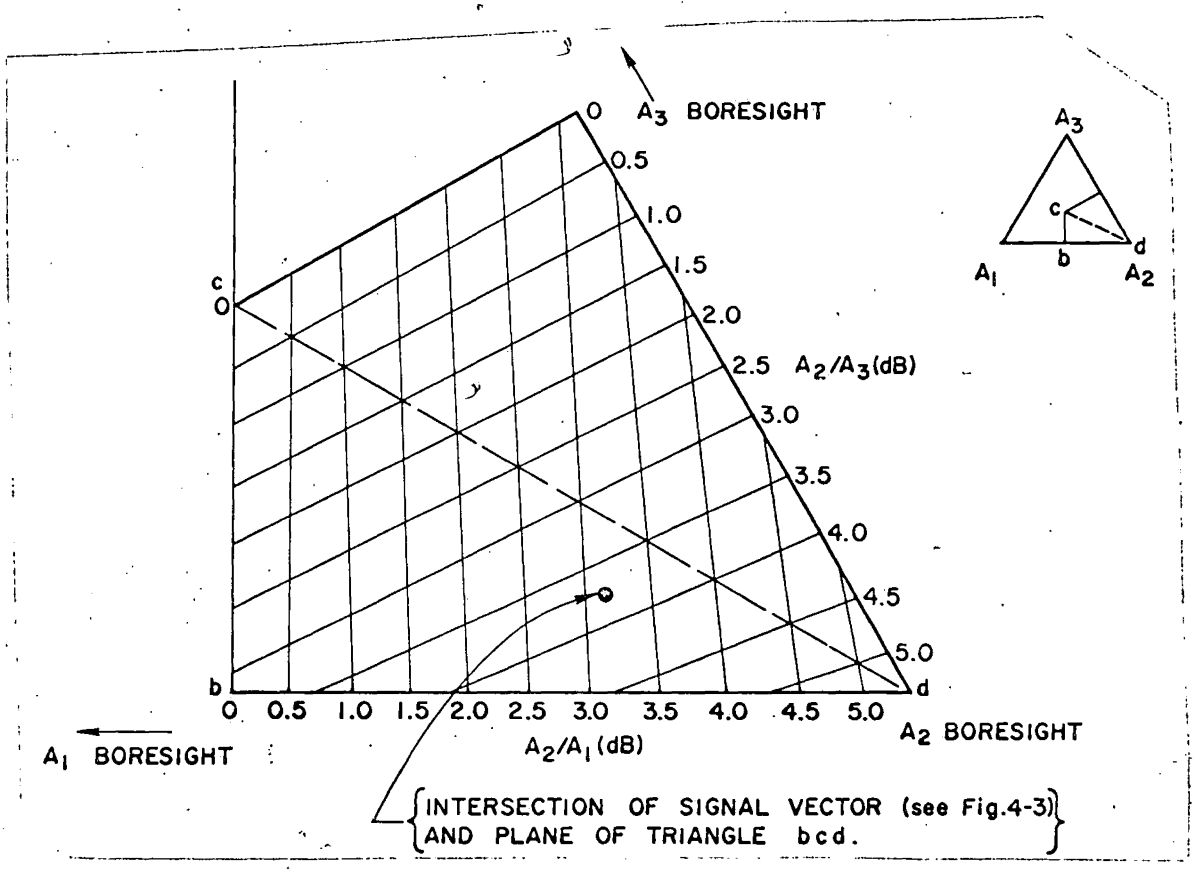

FIGURE 2-5 CONSTANT RATIO CONTOURS

2.2 DIRECTION-FINDING COVERAGE

The boresight of the DF array would be mounted at a half cone angle of 60° with respect to the -Y Axis as shown in Figure 2-1 and the inhibit antenna pointed 180° relative to the DF array. This arrangement would result in coverage consisting of a cone of revolution extending from the -Y axis to within 60° of the +Y axis as the vehicle rotates.

It is also suggested that attitude control of the spin axis be employed to tilt the spin axis 35° relative to the earth's spin axis as shown in Figure 2-6. This would align the spin axis perpendicular to the earth surface at approximately 55° N latitude on descending passes and the array would continually scan the horizon and provide coverage from the sub-satellite point to the horizon. This spin axis position provides 100% horizon to horizon coverage from 20° to 80° N latitude on descending passes and is optimized for coverage of emitters with relatively low elevation beams near the horizon. As can also be observed from Figure 2-6, on ascending passes, the spin axis will be approximately parallel to the earth surface over the region of interest. This alignment provides excellent coverage to beams pointed at relatively high elevation angles. In summary, with the spin axis tilted 35° relative to the earth's spin axis, the coverage will be optimized for low elevation horizon based intercepts on descending passes and optimized for under track high elevation intercepts on ascending passes.

Since the instantaneous array coverage is a 120° cone, the probability that the array will be looking at a given radar beam as it illuminates the vehicles on a single spin is approximately 30%. However, since a scanning radar will illuminate the vehicle many times during a pass, the cumulative probability of intercept quickly approaches 100%. Generally, from each emitter, there will be several intercepts spaced out along the flight path.

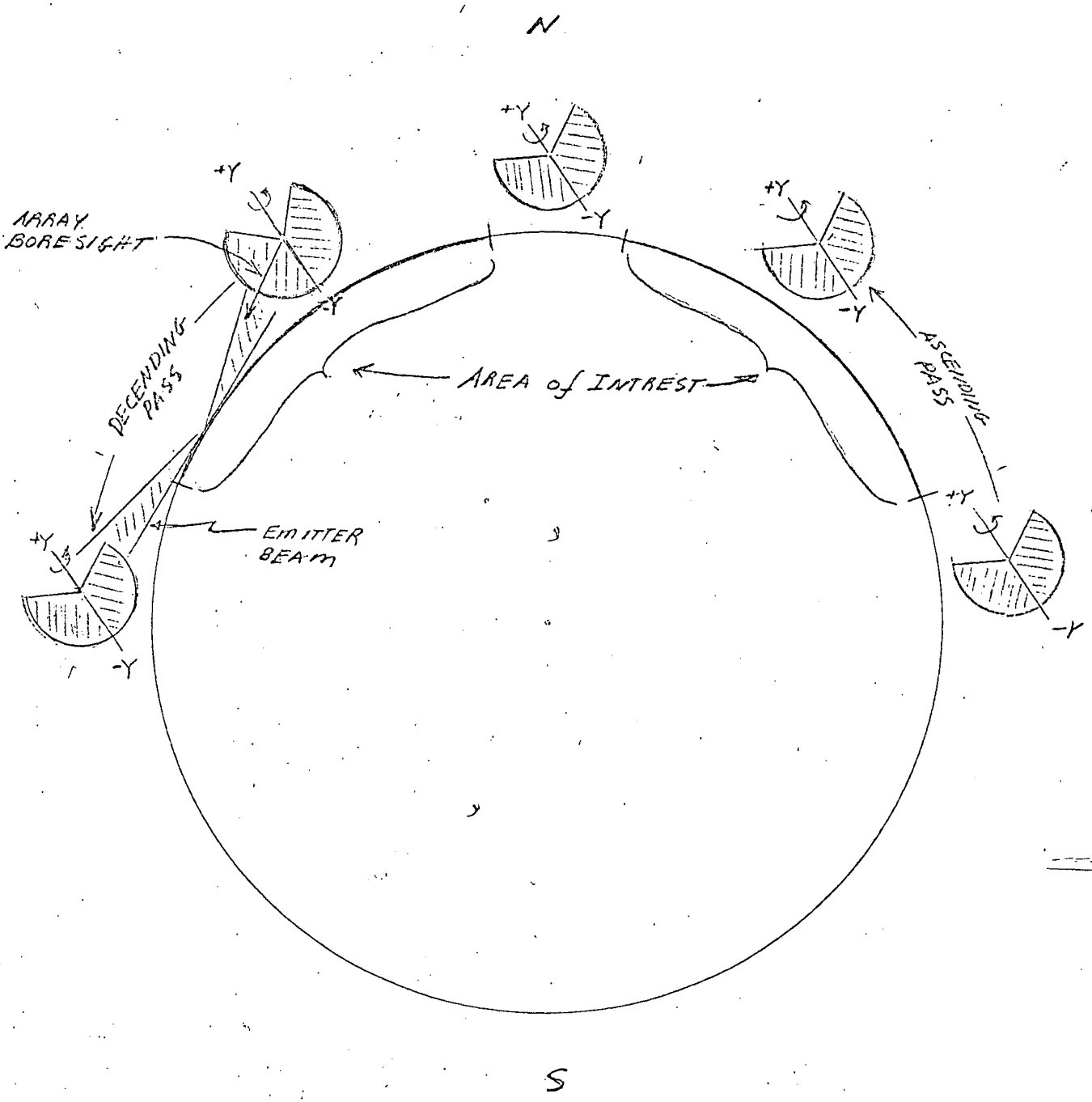

FIGURE 2-6 DF COVERAGE

As will be shown later in Section 6.0 the estimated overall 1σ DF accuracy of the system will be approximately 5^{o} in both azimuth and elevation. The footprint of a single look from one emitter will be an elongated ellipse which would provide reasonably good azimuth location accuracy but poor radial (or range) accuracy for horizon based emitters (5^{o} in Azimuth corresponds to approximately 100 miles at 1200 miles slant range). However, since the baseline over which the collection system will intercept a given scanning emitter is quite large (hundreds of miles), there will be several intercepts spaced out along this baseline from each radar as illustrated in Figure 2-7. The intercepts of several ellipses at different azimuth angles will provide improved radial location accuracy over the single intercept.

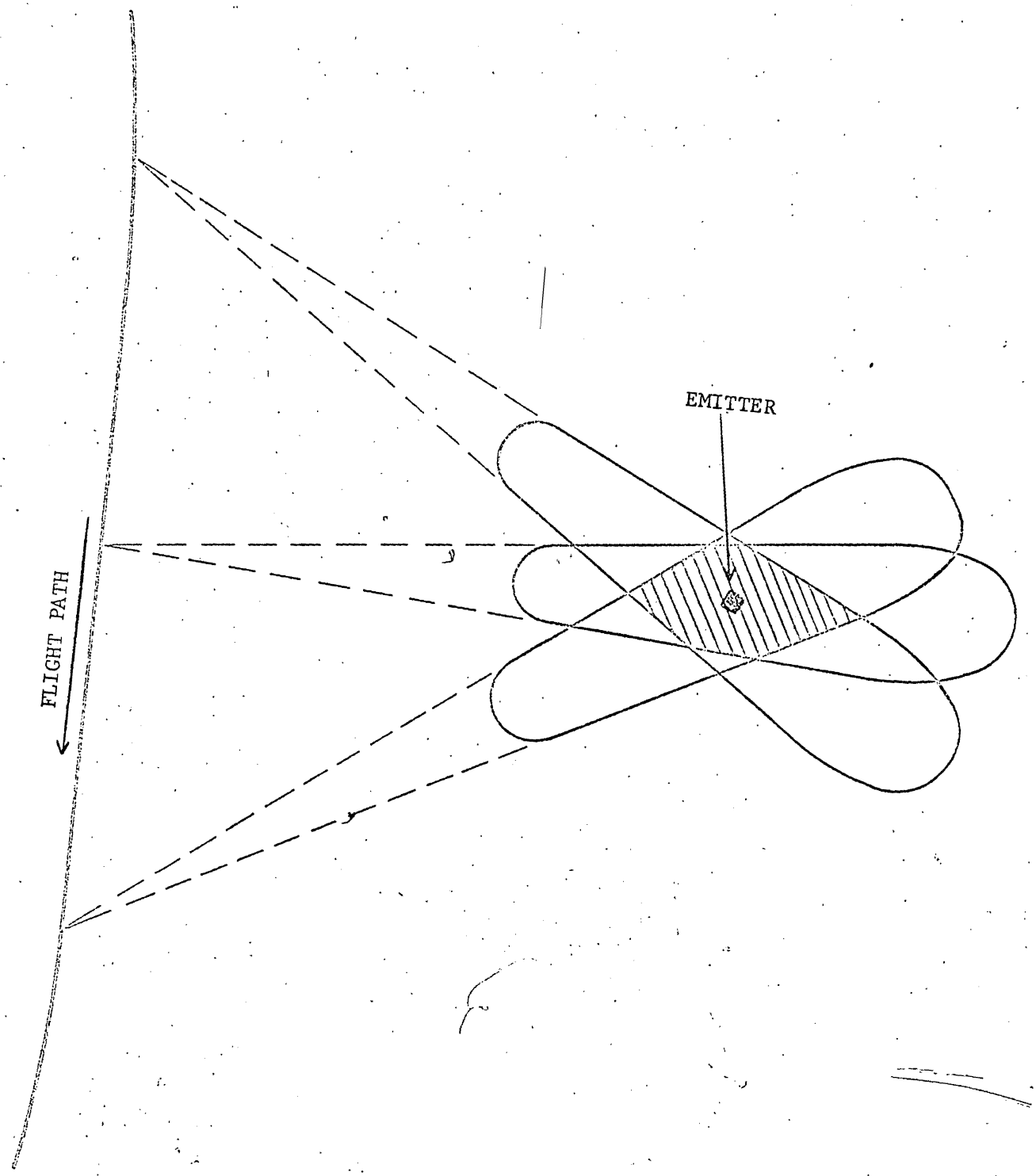

FIGURE 2-7 TYPICAL INTERCEPT

3.0 PAYLOAD DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

The simplified block diagram of the receiver payload is given in Figure 3-1. The system as studied, has instantaneous coverage over a 2 GHz frequency range which can be command selectable to any one of five sub-bands between 2 and 12 GHz. A brief review of the signal parameter measurements made by the receiving system will be given here with a more detailed description presented in Sections 3.2 through 3.7.

DF Measurement

The amplitude monopulse system employs six RF channels to provide a 120^{o} cone of instantaneous DF coverage. The six parallel matched RF receiver channels can simultaneously be command selected to cover any one of the five 2 GHz sub-bands. Each RF channel down converts the selected RF band to a common IF band which is then detected and amplified in the Video Post Detection Amplifier and then entered into the DF Video Processor.

In addition to the six DF channels, there is an additional inhibit channel which restricts the DF coverage to the forward hemisphere of the six antenna cluster.

The DF Video Processor measures and produces a digital output for the signal amplitude in the highest channel (the received power level measurement) and the relative signal levels in the next two highest channels (the angle of arrival in both azmuth and elevation). These three measurements are then digitally outputted to the output format generator. A total of 28 bits are required to read out the absolute power level of the highest channel to $\pm$ 0.3 dB and the DF power ratios of the 2nd and 3rd highest channels also to $\pm$ 0.3 dB resolution.

Frequency Measurement

Instantaneous frequency measurements are made on a pulse-by-pulse basis with two broadband delay-line frequency discriminators pre-

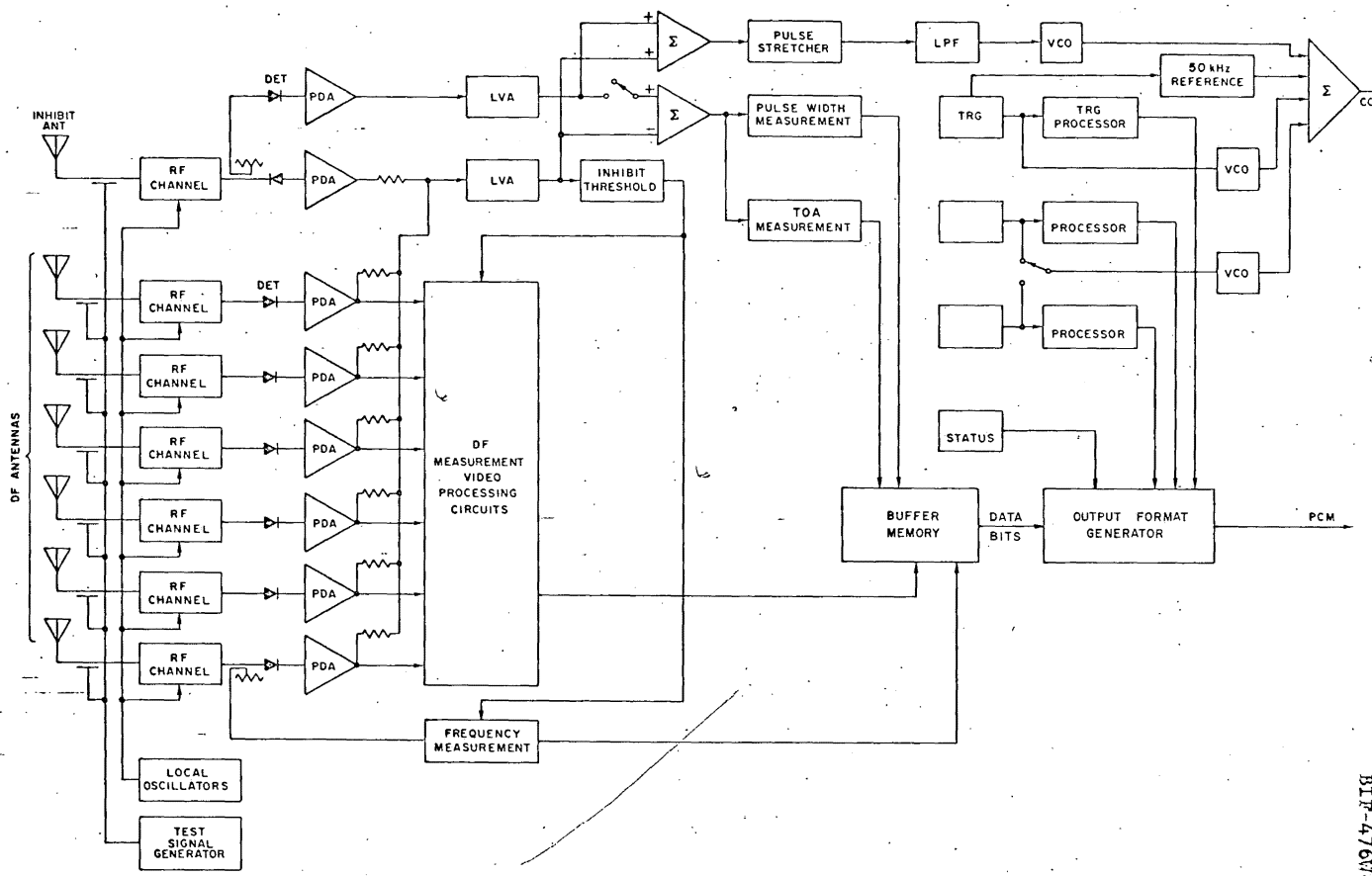

FIGURE 3-1 SIMPLIFIED PAYLOAD BLOCK DIAGRAM

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ceded by a 2 GHz broadband TDA limiter. The two discriminators are used for both a coarse and fine frequency resolution to provide an overall 1σ accuracy of 4 MHz. Ten data bits are needed to readout the frequency word to a 2 MHz resolution over the 2 GHz RF input band. The frequency measurement is inhibited by the same threshold as the DF measurement, thus resulting in equal coverage for both measurements.

Pulse Duration Measurement

A high accuracy pulse duration measurement is made similar to those made in the recent P-11 receivers. With clean multipath free main-beam pulses received, measurements should be consistently generated with an absolute accuracy of 0.05 μsec. Assuming an input pulse-width range of 0.1 μsec to 10 μsec, a seven bit binary word will report this measurement with a .0625 μsec resolution for pulse durations from 0.1 to 5 μsec and 0.125 μsec resolution from 5.125 to 10 μsec pulse widths.

Time-of-Arrival Measurement

A time-of-arrival (TOA) measurement is made and converted to a digital word to be included in the output PCM bit stream. Eight bits are needed to report this word to 1 μsec resolution. To provide complete scan characteristics, both the TOA and pulse duration measurements are reported over the entire spherical coverage area whereas the DF and frequency measurements will be reported over only the forward hemisphere. Spherical coverage for these two measurements is obtained be summing the detected video pulses from the inhibit channel with the sum of the DF channels.

Other Outputs

In addition to the above measurements, a Time Word (one per second), Horizon Sensor pulses, Sun Sensor pulses, and payload status are converted to digital words and time multiplexed into the PCM bit stream.

The PCM bit stream is the primary payload output; however, there are other data outputs which are frequency multiplexed with the PCM bit stream on the down link. The detected output of the inhibit

antenna is dynamic range compressed, pulse stretched and used to deviate a VCO. This output will provide wide-open Omni-Video data 360° around the spin cycle for continuous recording of emitter scan characteristics. A choice of either the Horizon or Sun Sensor can be command selected and also transmitted on a VCO channel. The TRG is put on a third VCO channel and all three VCO's along with a 50 KHz reference tone are summed together and later frequency multiplexed into the link containing the PCM word.

To verify the operation of the receiver and to also provide accurate on-board payload calibration, a pulsed RF test signal is inserted at the input of each RF channel and excited for a period of 0.36 sec. at one minute intervals by the TRG.

3.2 RECEIVER RF FRONT END DESCRIPTION

3.2.1 RF Channel Description

The block diagram of a typical RF channel is given in Figure 3-2.

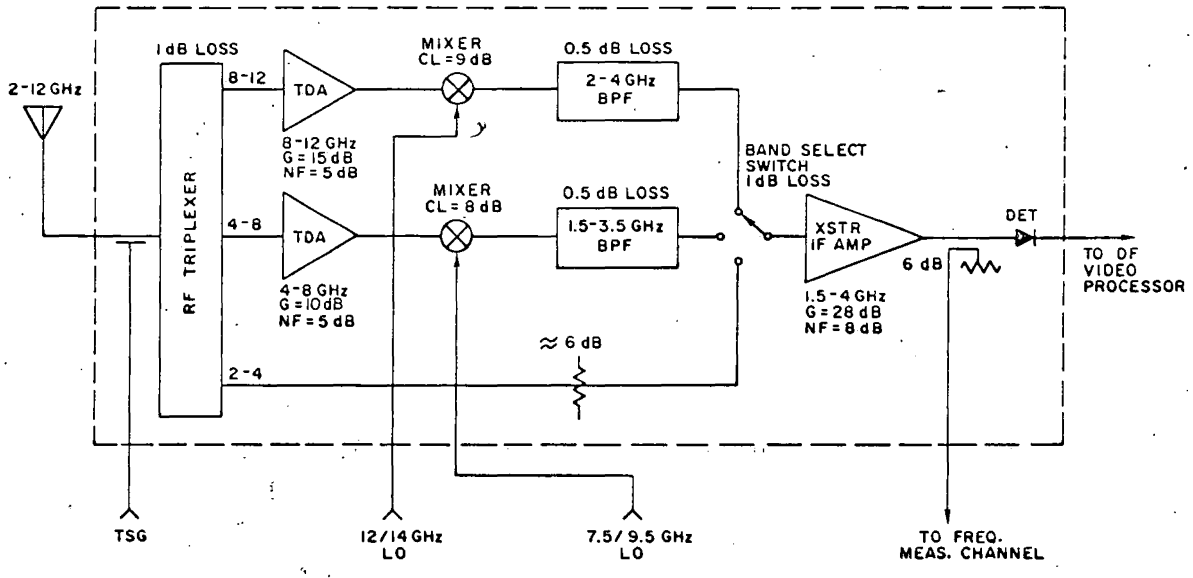


FIGURE 3-2 TYPICAL RF CHANNEL

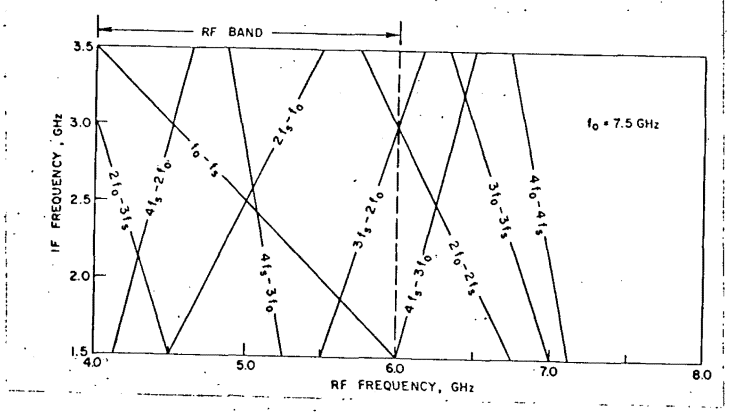
With the exception of the channel having the output coupler to also drive the frequency measuring channel, all seven RF channels are identical.

The 2-12 GHz input band is separated into the three bands 2-4, 4-8 and 8-12 GHz in the input RF triplexer. In the 2-4 GHz sub-band the signal is coupled directly to the IF amplifier through a 6 dB attenuator to set the sensitivity at the desired level. The 4-8 GHz band is down converted in 2 GHz sub-band segments to a 1.5 to 3.5 GHz IF band by selecting the local oscillator frequency of either 7.5 or 9.5 GHz. Similarly, the 8-12 GHz band is down converted in 2 GHz segments to a 2-4 GHz IF band using either a 12 or 14 GHz local oscillator. The IF band of 1.5 to 3.5 GHz was chosen for the 4-8 GHz RF band to insure frequency separation between the RF and IF frequencies at the lower edge of this band. The desired 2 GHz sub-band is command selected from the 5 available by 1) positioning the RF band select switch and, 2) exciting the appropriate local oscillator.

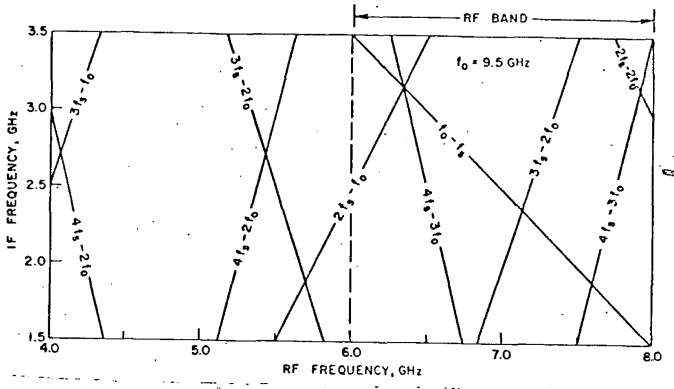
The test signal is coupled in at the input through a capactive coupling network. This network's coupling coefficient increases at a rate of 6 dB per octave, however, since a broadband multiplier is suggested whose output will drop off with increasing frequency, the amplitude response of the cascaded devices will approximately compensate each other.

3.2.1.1 Local Oscillator Frequency Selection and Spurious Response Considerations

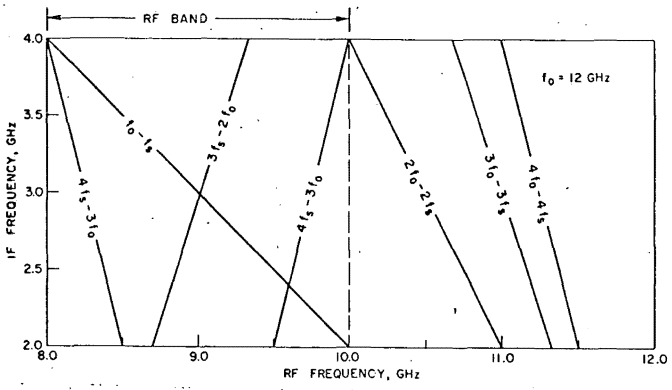
The local oscillator frequencies were chosen in all cases to be on the high side of the RF band. This was done to avoid many of the additional higher level spurious responses which would exist if the low side LO were used. This choice does however necessitate higher frequency local oscillators, but presents no difficulties with the availability of Gunn effect oscillators. The spurious responses up to the fourth order were investigated in all bands and the results shown in Figures 3-3, a through d. The highest level spur of consequences is



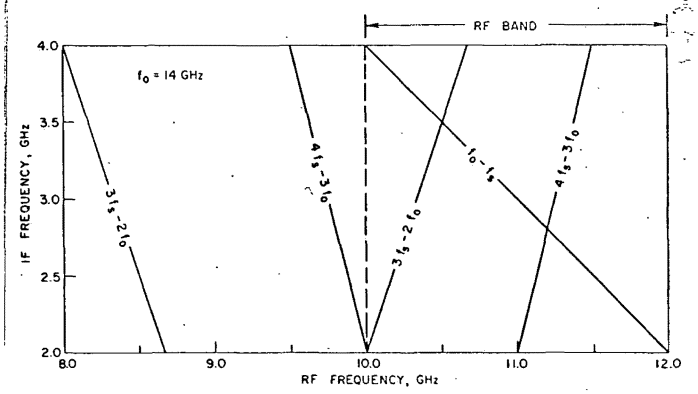
a. Band II, 4-6 GHz



b. Band III, 6-8 GHz



c. Band IV, 8-10 GHz



d. Band V, 10-12 GHz

FIGURE 3-3 DOWN CONVERTER MIXER SPURIOUS RESPONSES

the $2f_o-2f_s$ component. Aertech has published data taken on a double balanced MX-2000 mixer, Figure 3-4, which indicates this spurious is greater than 40 dB below the desired component, f_o-f_s, at an input power level of -15 dBm (the highest level the mixer will see in this application). To further verify these data, measurements were performed on an MX 8000 mixer and are given in Figure 3-5. It was noted that the relative level of the $2f_o-2f_s$ response varied with input frequency, hence a frequency was chosen for this measurement for which this component was highest. Although the $2f_o-2f_s$ response was not as low as that shown by the Aertech data, it is adequately suppressed for this application. Its level was -33 dB relative to (f_o-f_s) at an input level of -15 dBm and was decreasing 2 dB for each 1 dB reduction in input level. All other in-band spurious responses, as can be seen in Figures 3-4 and 3-5, are even further down in level.

3.2.1.2 Input Equivalent Noise Figure Calculation

Since the TDA preamplifier gains are relatively low, the mixer and IF amplifier noise will contribute to the overall input noise figure. The equivalent noise figure, NF, of two cascaded devices can be expressed as

$$F_{12} = F_1 + \frac{F_2 - 1}{G_1}, \tag{3.1}$$

where

F_1 = NF of input device

F_2 = NF of second device

and

G_1 = Gain or loss of input device.

As an example, consider the C-band equivalent noise figure calculation given below.

Let

F_{12}' = the equivalent NF at mixer input

and

Mixer NF = 8 dB

Mixer conversion loss = 8 dB

IF NF = 8 dB

BPF loss = 0.5 dB

Microwave switch loss = 1 dB.

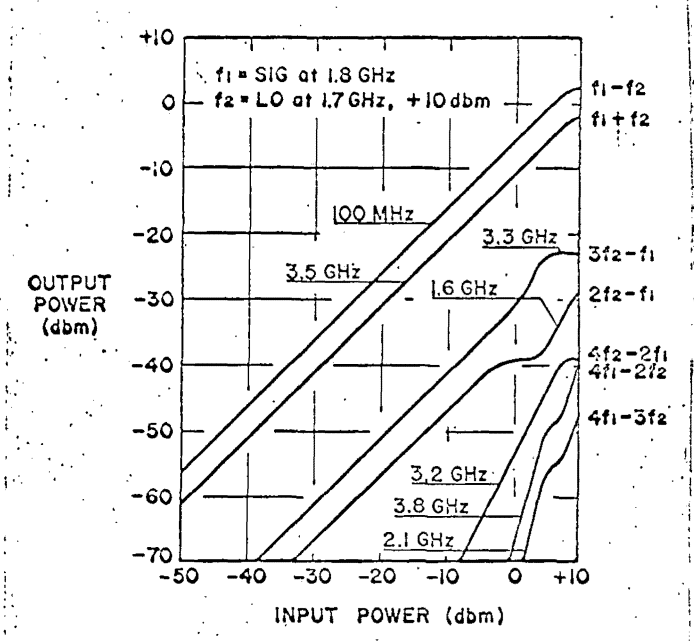


Fig. 7 — Fixed level and level dependent IM products at the IF output with the first order sum and difference frequency outputs shown for reference (MX2000).

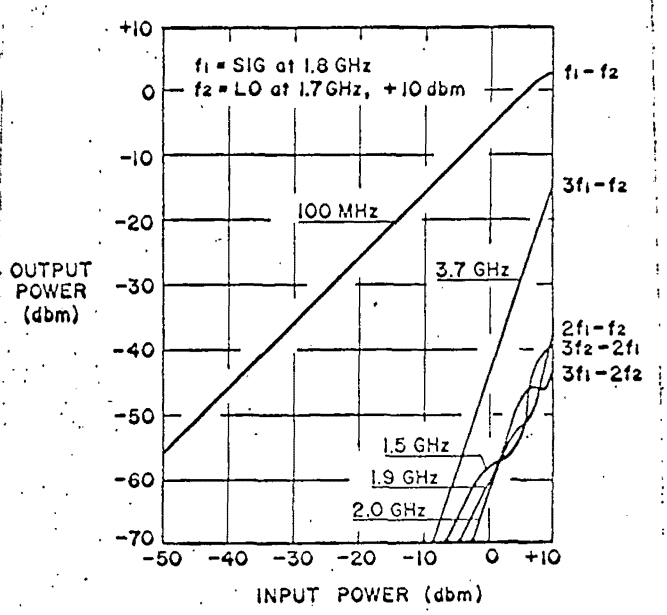


Fig. 8 — Level dependent IM products at the IF output with the first order difference frequency shown for reference (MX2000).

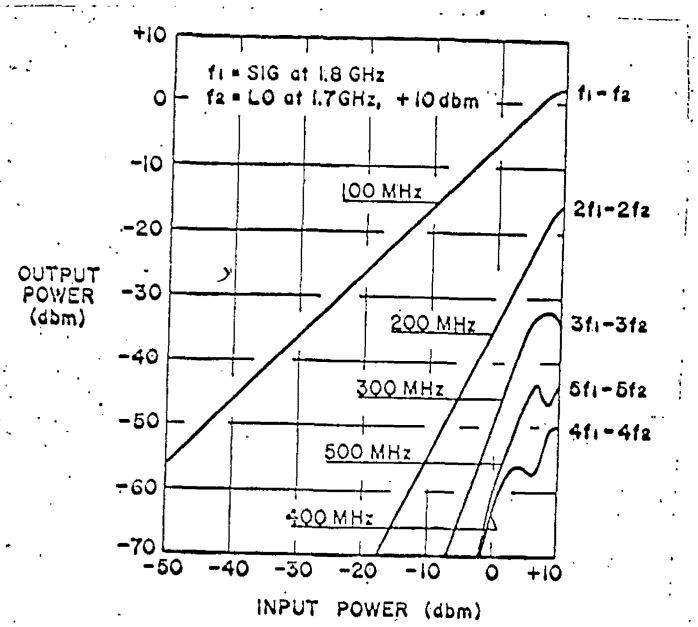


Fig. 9 — "IF harmonic" level dependent IM products with the fundamental IF output shown for reference (MX-2000).

FIGURE 3-4 AERTECH MEASURED DATA ON THE MX-2000 MIXER (PUBLISHED DATA)

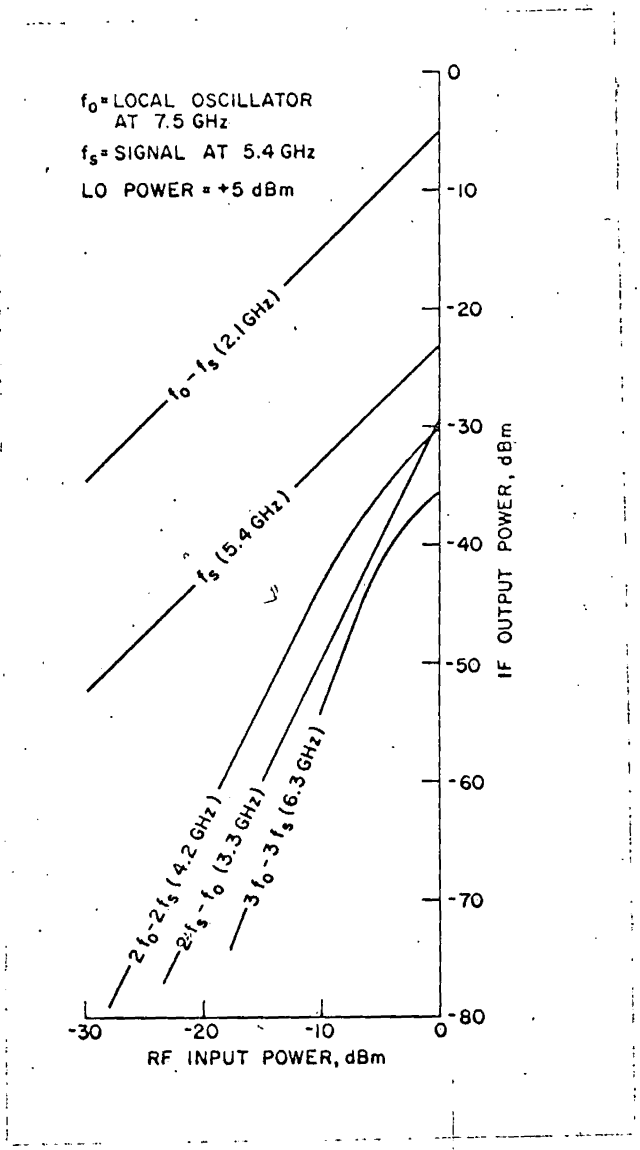


FIGURE 3-5 MEASURED AERTECH MX 8000 SPURIOUS RESPONSE DATA S/N 2197 (This data was for a worst case signal frequency where $2f_o - 2f_s$ response was highest.)

therefore

$$G_1 = -9.5 \text{ dB } (0.112)$$
$$F_1 = F_2 = 8 \text{ dB } (6.33)$$

and using eq. 3.1 above,

$$F_{12}' = 6.33 + 5.33/0.112 = 53.8 \text{ (17.3 dB)}.$$

Let

$$F_{12} = \text{equivalent NF at TDA input,}$$

and

$$F_1 = 5 \text{ dB } (3.16)$$
$$G_1 = 10 \text{ dB } (10)$$
$$F_2 = 17.3 \text{ dB } (53.8),$$

therefore

$$F_{12} = 3.16 + 52.8/10 = 8.44 \text{ (9.3 dB)}.$$

The equivalent noise figures for all the bands are summarized in Table 1 at the end of Section 3.2.1.4.

3.2.1.3 Maximum Input Power Considerations

In the breadboard feasibility model of the DF processing circuits, tunnel detectors have been used which limit the maximum input power to -12 dBm at the detector input. It was originally thought necessary to operate only in the square law region of the detector; however, it has more recently been realized that this is not a necessary restriction and it is possible to operate on up into the linear region of the detector. Since hot carrier diode detectors have a linear detection region extending to + 20 dBm, it would be possible to use these detectors instead of the tunnel detectors if the additional dynamic range were necessary. The maximum input power calculations shown here will be based on both the use of the hot carrier diode detectors and the tunnel detectors used in this study.

As an example, the parameters that determine the maximum input power level capability in C-band are given below:

1)	TDA 1 dB Compression point (output level)	-15 dBm
2)	Maximum level of ($2f_o-2f_s$) spurious response relative to (f_o-f_s) response for a mixer input power of -15 dBm (See Figure 3-5).	-36 dBm
3)	Mixer, filter and rf switch losses	9.5 dB
4)	Maximum power level at IF amplifier input	-24.5 dBm
5)	IF amplifier gain	28 dB
6)	Maximum power level out of IF amplifier	+3.5 dBm
7)	IF amplifier 1 dB compression point (output level)	+7 dBm
8)	a) Hot carrier detector maximum input power for linear detection	+20 dBm
	b) Tunnel detector maximum input power	-12 dBm
9)	Net RF gain (receiver input to detector input)	27.5 dB
10)	Maximum receiver input power level	
	a) Using hot carrier detectors	-24 dBm
	b) Using tunnel detectors	-39.5 dBm

If a hot carrier diode detector were used, the maximum input power capability would be limited by the TDA 1 dB compression point in both C and X bands, and the IF amplifier 1 dB compression point in S-band. If a tunnel detector were used, it would be the element that limited the maximum input power capability in all three bands.

The maximum power levels referred to both the detector and receiver inputs are also summarized for all bands in Table 1 at the end of Section 3.2.1.4.

3.2.1.4 Receiver DF Measurement Sensitivity and Dynamic Range Calculation

The DF measurement sensitivity and dynamic range will be calculated in this section using the calculated equivalent noise figures and maximum input powers calculated in Sections 3.2.1.2 and 3.2.1.3 above. As an example, the C-band calculations are shown below in detail and the results for all bands summarized in Table 1.

3.2.1.4.1 C-Band DF Measurement Sensitivity Example Calculation

Frequency Ranges	4-6 GHz
	6-8 GHz
RF Bandwidth, B_r	2 GHz
Video Bandwidth, B_v	5 MHz
Equiv. NF (TDA input), F_{eq}	9.3 dB
Input RF Triplexer Filter Loss	1 dB
Net RF gain, G (TDA to Detector Input)	28.5 dB
Detector voltage sensitivity, K	1000 μV/μW
Detector video resistance, R_v	100 ohms
Required detected output signal-to-noise ratio $(S/N)_0$	14 dB

The noise power referred to the TDA input, P_{N1}, is

$$P_{N1} = -114 \text{ dBm} + 10 \log_{10} B_r + F_{eq} = -71.7 \text{ dBm}. \quad (3.2)$$

Assuming a noise limited system, (i.e. a system where the RF front end noise is the dominant noise source) the detected output signal-to-noise ratio, $(S/N)_0$ is given by

$$(S/N)_0 = \frac{(S/N)_i^2}{(1 - \frac{B_v}{2B_r}) + 2\,(S/N)_i} \times \frac{B_r}{2B_v} . \quad (3.3)$$

Using the above parameters, and solving for $(S/N)_i$

$$(S/N)_i = -2.6 \text{ dB}.$$

Therefore, the signal power at the TDA input, P_{S1} is

$$P_{S1} = P_{N1} + (S/N)_i = -74.3 \text{ dBm.} \tag{3.4}$$

To determine the relative contribution of front end noise, the detected noise voltage due to the front end noise power will be determined both with and without a RF signal present and then compared with the post detection noise voltage introduced at the detector output.

No Signal Case (noise alone)

First consider the detected front end noise.

The equivalent bandwidth, B_e, can be expressed as

$$B_e = \sqrt{2 B_v B_r - B_v^2} = 144 \text{ MHz.} \tag{3.5}$$

The front end noise power referred to the detector input, P_{N2}, is

$$P_{N2} = P_{N1} + G_n - 10 \log_{10}\left(\frac{B_r}{B_e}\right) = -54.6 \text{ dBm } (0.35 \times 10^{-2} \mu W) \tag{3.6}$$

and, the detected noise voltage due to P_{N2}, e_{N2}, is

$$e_{N2} = P_{N2} \times K = 3.5 \mu v. \tag{3.7}$$

Second, consider the noise generated at the detector output.

Assume post detection NF, $F_2 = 3$ dB, $R_v = 100$ ohms, $B_v = 5$ MHz and and -

$$e_{N3} = \sqrt{4KT B_v F_2 R_v} = 4\mu V \tag{3.8}$$

Therefore, when there is no signal present, the detected output noise level will have equal contributions from both the post detection noise and the RF front end noise.

Signal Present Case

With the signal present, the noise component due to detected RF noise will increase because of the presence of the signal X noise terms in the detection process. Recall from eq. 3.4 that the required signal power at the TDA input, P_{S1}, for a $(S/N)_0$ = 14 dB is -74.3 dBm and the net RF gain, G_n, is 28.5 dB. Therefore, the signal power at the detector input, P_{S2}, becomes

$$P_{S2} = P_{S1} + G_n = -45.8 \text{ dBm } (2.6 \times 10^{-2} \mu W). \quad (3.9)$$

and, the detected output signal voltage, e_{S2}, due to P_{S2} is

$$e_{S2} = K P_{S2} = 26 \mu V. \quad (3.10)$$

Recall, for [illegible] = 14 dB,

$$P_{S1} = -74.3 \text{ dBM}, \ (S/N)_0 = 14 \text{ dB}.$$

Therefore,

$$e_{N4} = 5.2 \mu V$$

where e_{N4} is the detected noise voltage due to the rf front end noise with a signal present and zero contribution of post detection noise is assumed. Also recall, from eq. 3.4 the noise generated at the detector output, e_{N3}, is 4μV.

Therefore, the total detected signal-present noise voltage, e_N, is

$$e_N = \sqrt{e_{N3}^2 + e_{N4}^2} = 6.5 \mu V. \quad (3.11)$$

When the signal is present, there will be approximately a 1 dB increase in the detected noise, and the reduction in sensitivity over the noise limited case to the contribution of post detection noise is approximately 1.0 dB.

Recall the input triplexer loss = 1dB. Therefore, the required signal power, P_S, at the receiver input for $S/N)_0$ = 14 dB is

$$P_S = -74.3 \text{ dBm} + 1 \text{ dB} + 1 \text{ dB} = -72.3 \text{ dBm}.$$

As will be shown later in Section 4.0, the required measurement dynamic range is approximately 9 dB.

Therefore the minimum signal level referred to the receiver input, for a DF measurement, P_{min} is

$$P_{min} = P_S + 9 \text{ dB} = -63.3 \text{ dBm}.$$

The DF measurement sensitivity and input dynamic range for all bands is summarized in Table 1.

TABLE 1

RECEIVER SENSITIVITY AND DYNAMIC RANGE CHARACTERISTICS

		2-4 GHz	4-8 GHz	8-12 GHz
1. Equivalent NF				
a. Mixer input	dB	NA	17.3	19.8
b. TDA input	dB	8*	9.3	7.2
c. Receiver input	dB	16	10.3	8.2
2. Net RF gain (receiver input to detector input)	dB	20	27.5	31.5
3. Maximum power level, detector input				
a. Tunnel detector	dBm	-12	-12	-12
b. Hot carrier diode detector	dBm	+ 7	+ 3.5	+ 2.5
4. Maximum power level, receiver input				
a. Tunnel detector	dBm	-32	-39.5	-43.5
b. Hot carrier diode detector	dBm	-13	-24	-29
5. DF measurement sensitivity receiver input **	dBm	-58.6	-63.3	-65.4
6. Input dynamic range**				
a. Tunnel detector	dB	26.6	23.8	21.9
b. Hot carrier diode detector	dB	45.6	39.3	36.4

* IF Amplifier Input

** Includes a 9 dB measurement dynamic range in C and X band and approximately a 4 dB measurement dynamic range in S band, see Section 4.0.

3.2.1.4.2 Receiver Sensitivity and Dynamic Range Conclusions

The DF measurement sensitivity referred to the receiver input is -58.6*, -64, and -67 dBm in S, C and X band respectively. In S-band the desired sensitivity is well below the maximum attainable. In C and X bands the input equivalent noise figure is pacing the sensitivity. In these bands, the receiver is already at maximum realistic sensitivity and one would have to consider increased antenna gains or reducing bandwidths to realize additional sensitivity. One could also consider TDA preamps at the antennas to override the cable and filter losses, however, due to the extreme ambient temperature excursions on the antenna boom, and the amplitude matching accuracy requirements, this would appear to be highly undesirable.

Using Tunnel Detectors, the dynamic range of the receiver is approximately 24-27 dB which has been shown in Reference 1 to be marginally adequate. If it were necessary to increase the dynamic range, this could easily be accomplished by using hot carrier diode detectors and adding a third segment to the two-segment linear amplifier which would be adjusted to operate in the linear portion of the detector characteristic.

3.2.1.4.3 Calculation of Receiver 50% Detection Sensitivity

The detection sensitivity for the TOA, Pulse Width and Omni Video measurements will be calculated in this section. These measurements are made on the summed detected outputs of all seven channels (6 DF + 1 Inhibit). The detected noise voltage will be the sum of all seven uncorrelated channel noise sources.

*-58 dBm is higher than normally would be used in this band (based on data rate considerations). However, it will be shown in Section 5.1 that the net antenna gain in this band is -6.5 dB on boresight.

The AC component of the detected output rms noise voltage, σ_n, is given by

$$\sigma_n = \sqrt{n}\ KTF\sqrt{2BB_v - B_v^2} \tag{3.12}$$

where

n = number of uncorrelated rf channels added after detection

K = Boltzmans constant

T = 273°K

F = Receiver noise figure

$\propto$ = detector square low rectification efficiency.

For $B \gg B_v$, it can be assumed that the noise has a Gaussian amplitude distribution. Therefore, for a false alarm rate of 1 FAS, a video bandwidth of 5 MHz, and a signal pulse width equal to the reciprocal video bandwidth (0.2 μsec.), the input signal power required, S_i, for a single pulse 50% probability of detection is

$$S_i = 5.1\sqrt{n}\ \ KTF\sqrt{2BB_v}. \tag{3.13}$$

For this receiver,

n = 7 (6 DF + 1 Inhibit Channel)

Therefore

$$S_i = -114\ \text{dBm} + 10\log_{10}(4.1\sqrt{7}) + 10\log_{10}\sqrt{2\text{x}2000\text{x}5} + F$$

$$S_i = -81.2\ \text{dBm} + F \tag{3.14}$$

Using the equivalent noise figures shown in Table I, this results in an available 50% detection sensitivity referred to the receiver input of -65.2 dBm in S-Band, -70.9 dBm in C-Band and -73 dBm in X-Band.

3.2.1.5 Summary of Critical Microwave Components

Since the microwave channels require rather critical gain matching and, as will be shown later, make up a large portion of the total payload weight, it was necessary to verify the availability of all of the critical components as given below. These data were based on discussions with the various vendors, however, firm commitments were not obtained since the component would not be procured at this time and would be unnecessarily burdening the vendors.

TDA/Mixer Specifications - Suggested Vendor - Aertech

		C-Band	X-Band
A.	TDA Specifications		
1.	Frequency Range	4 to 8 GHz	8 to 12 GHz
2.	Gain	10 dB Min	15 dB Min
3.	Noise Figure	5 dB Max	5 dB Max
4.	Output Saturation Level	-15 dBm	-15 dBm
5.	Input VSWR	1.3 Max	1.3 Max
6.	Temperature Range	$-20^{o}C$ to $+ 60^{o}C$	$-20^{o}C$ to $+ 60^{o}C$
7.	Size(typ)	2" x 4" x 1"	5" x 4 3/8" x 1 3/8"
8.	Weight	16 Oz.	16 Oz. Max
9.	Power Requirements	20 ma @ 10V	20 ma @ 10V
B.	Double Balanced Mixer Specifications		
1.	RF Frequency Range	4 to 8 GHz	8 to 12 GHz
2.	IF Frequency Range	1.5 to 3.5 GHz	2 to 4 GHz
3.	LO Frequency Range	7.5 to 9.5 GHz	12 - 14 GHz
4.	Conversion Loss	8 dB Max	9 dB Max
5.	Noise Figure	8 dB Max	9 dB Max
6.	L0 Power	5 mw	5 mw
7.	Size	0.63" x 0.5" x 0.6"	.63" x .5" x.6"
8.	Weight	1 oz.	1 oz.
C.	Combined Matched Specifications - Set of 7 ($T = -20^{o}C$ to $+ 60^{o}C$)		
1.	Gain Flatness	$\pm$1.5 dB Max	$\pm$1.5 dB Max
2.	Relative Gain Match (6 amplifier/mixer sets to be matched to a reference set)	$\pm$0.75 dB Max	$\pm$0.75 dB Max

Local Oscillators - Suggested Vendors - Varian and Monsanto

1.	Type	Gunn Oscillators
2.	Output Frequencies	7.5, 9.5, 12 and 14 GHz
3.	Minimum Output Power	50 MW
4.	Temperature Stability (INVAR Cavity)	50 KHz/°C Max
5.	Weight	3 Oz.
6.	Power Requirements	400 ma at 9V

Transistor IF Amplifier - Suggested Vendors - Avantek and Aertech

Matched set of 7 amplifiers

1.	Frequency Range	1.5 to 4.0 GHz
2.	Gain	28 dB Min
3.	Noise Figure	8 dB Max
4.	Temperature Range	-20 to + 60°C
5.	Gain Flatness	± 1 dB
6.	Relative Gain Track (6 amplifiers to be matched to a reference amplifier within ±0.5 dB	± 0.5 dB
7.	VSWR, Input and Output	1.5
8.	Power Output at the 1 dB Gain Compression Point	+ 7 dBm
9.	Size	12 - 16 cu.in.
10.	Weight	9 Oz.
11.	Power Requirements	80 ma at 15V

NOTE: The Avantek AWM-4000N does not quite meet the above specifications as a standard model, however, at some additional cost for aligning and testing, these specifications should be attainable. Aertech has a balanced transistor amplifier under development that should exceed all of these specifications. The amplifier will be larger (4" x 4" x 1") compared to the Avantek AWM-4000N (2" x 2" x 3") and weigh about 12 Oz. as compared to the AWM-4000N (9 Oz.)

TDA Limiter (used in Frequency Measurement Channel)

Suggested Vendor - Aertech

1.	Frequency Range	5.0 - 7.0
2.	Small Signal Gain	35 dB Min
3.	Noise Figure	8 dB Max
4.	Gain Variation	± 2 dB Max
5.	Temperature Range	-20 to + 60°C
6.	Limiting Characteristics	Limiting to occur at -50 dBm input. The output will be between -15 and -11 dBm. After onset of limiting, output variation will not exceed ±1 dB for input signal levels to -15 dBm.
7.	Weight	32 Oz.
8.	Power Requirements	40 ma @ 10V

3.2.1.6 Channel Gain Tracking

For good DF accuracy it is extremely important that great care be taken in matching the amplitude characteristic of the six DF channels. It is recommended that the five channels connected to the antennas on the periphery of the cluster each be matched to the boresight channel.

In order to assess an attainable rf channel match, a tolerance was obtained for each of the components effecting the overall channel gain. These estimates were all based on discussions with various manufacturers and by also referring to published data. These data are given in Table 2. The advertised data are given in the first column in the form of a worst case matching specification. If it is assumed that the match between the boresight channel and any of the other channels varies from 0 dB to this maximum value in a normal fashion (Gaussian distribution) and that the mean value is zero; then, the worst case tolerance is approximately equal to the 2.6σ value which is given in Column 2. The 1σ value can now be determined and all 1σ values summed in rss form to give an overall 1σ value of 0.4 dB in C and X bands and 0.3 dB in S band. This also corresponds to a 2.6σ of 1 dB in C and X bands and 0.75 dB in S band.

3.2.2 Frequency Measurement Channel

3.2.2.1 Up-Converter-Limiter-Discriminator Description

Instantaneous broadband frequency measurements are made on a pulse-by-pulse basis with two broadband delay-line frequency discriminators preceeded by a broadband TDA limiter, Figure 3-6. The output of the boresight channel IF amplifier is up-converted from either 1.5 - 3.5 GHz or 2.0 - 4.0 GHz to 5.0 - 7.0 GHz in the input mixer using either the 8.5 GHz or the 9.0 GHz local oscillator respectively. The difference frequency IF output is selected with the 5.0 - 7.0 GHz band-pass filter and amplified in the TDA limiter. The output of the limiter is then divided into two paths to simultaneously drive the coarse and fine frequency discriminators. The

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TABLE 2

RF CHANNEL GAIN MATCH

COMPONENT	ESTIMATED TOLERANCES dB			S-BAND	C&X-BANDS
	TOL	2.6σ	1σ	σ^2	σ^2
1. Triplexer	±0.2	0.2	.077	0.0059	.0059
2. TDA/Mixer	±0.75	0.75	0.288	-	.083
3. Bandpass Filter	±0.2	0.2	0.077	0.0059	.0059
4. Microwave Switch	±0.2	0.2	0.077	0.0059	.0059
5. IF Amplifier	±0.5	0.5	0.192	0.0368	0.0368
6. Detector	±0.2	0.2	0.077	.0059	.0059
7. Attenuator	±0.4	0.4	0.154	0.0237	-
				.0841	0.1434
Overall Channel 1σ				0.29 dB	0.38 dB
Overall Channel 2.6σ				0.75 dB	1.0 dB

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detected outputs of the two discriminators are then combined in pairs using four differential amplifiers to obtain the four output voltages shown. These outputs are then entered into the frequency measurement video processor which is discussed in Section 3.4.

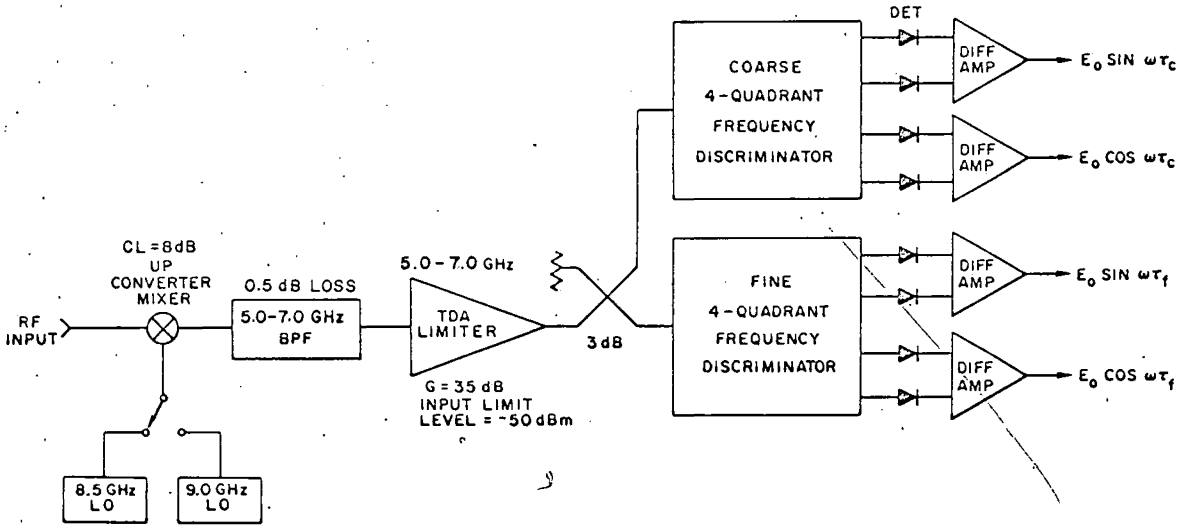


FIGURE 3-6 FREQUENCY MEASUREMENT RF CHANNEL

3.2.2.2 TDA Limiter Characteristics and Small Signal Suppression Measurements

The TDA Limiter serves two purposes. First, it provides dynamic range compression thereby reducing the range of power levels over which the video processing circuits must perform. Second, and most important, it provides suppression (up to 6 dB) to the lower of two simultaneous signal frequencies. This is highly desirable since the frequency discriminator can give erroneous frequency measurements to simultaneous signals of approximately equal level and the limiter reduces the relative power range over which this may occur to a negligible amount. This will be discussed later in Section 3.2.2.4 and the characteristics of the limiter will be given here.

Figure 3-7 shows the measured transfer characteristic of two limiters. The dashed curve with the vertical scale to the right is

data taken on a 2-4 GHz TDA amplifier used in the SAMPAN receiver. The solid curve and the left vertical axis is data taken on a 100 Hz to 15 MHz broadband video limiter. The reason for showing both sets of data is that the TDA was not available to perform small signal suppression measurements on, therefore, frequency scaled data was taken on the 15 MHz limiter and both transfer curves were shown for comparison. Very similar performance can be expected from the limiter since they both perform as nearly ideal limiters.

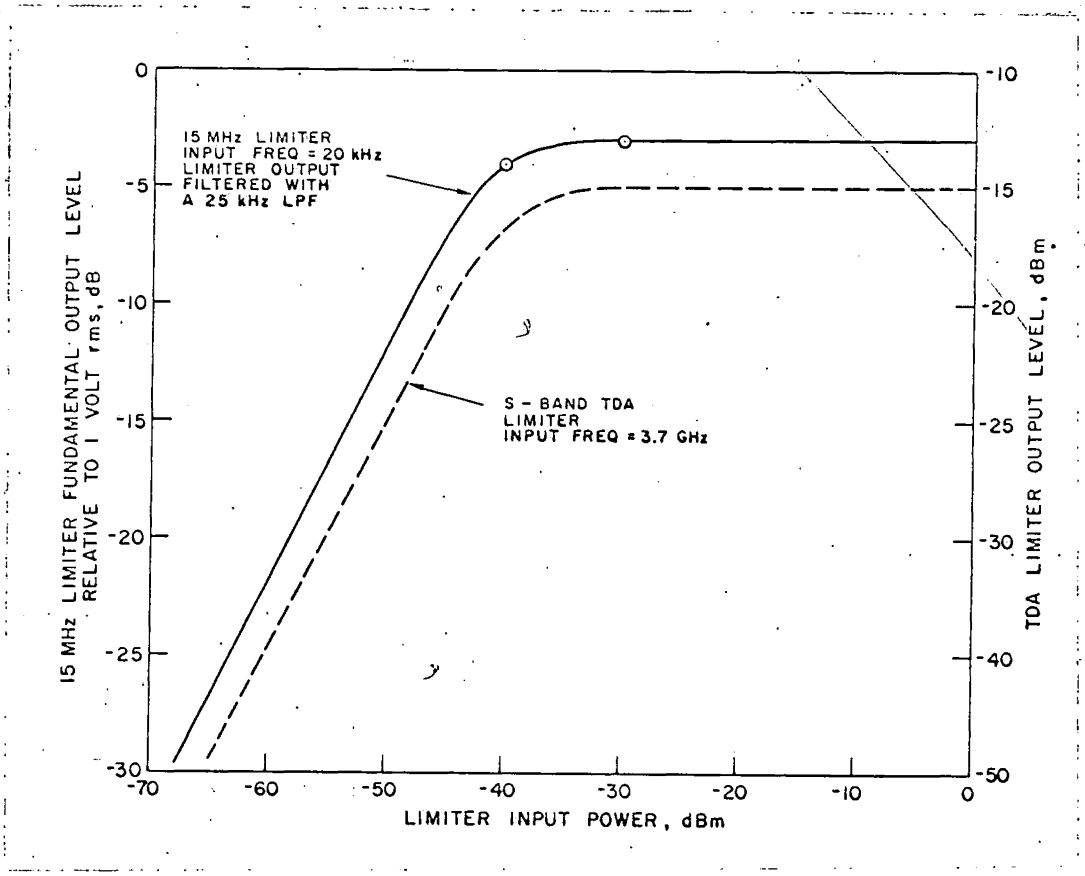


FIGURE 3-7 LIMITER MEASURED TRANSFER CHARACTERISTICS

The small signal suppression characteristics of the video limiter are shown in Figure 3-8. Data were taken for two points on the transfer characteristic. The dash curve is for the case when one signal was held constant at the knee of the curve, P_1 = -40 dBm, and the other signal, P_2 was varied from 10 dB below to 10 dB above this

point, -50 to -30 dBm. The solid curve is for the case when P_1 = -30 dBm (10 dB above the knee) and P_2 again varied about this point ± 10 dB. Similar signal suppression performance can be expected over the entire limiting range of the limiter. In Section 3.2.2.4, this suppression data will be applied for the simultaneous signal response of a discriminator to show the improvement gained by the use of the limiter.

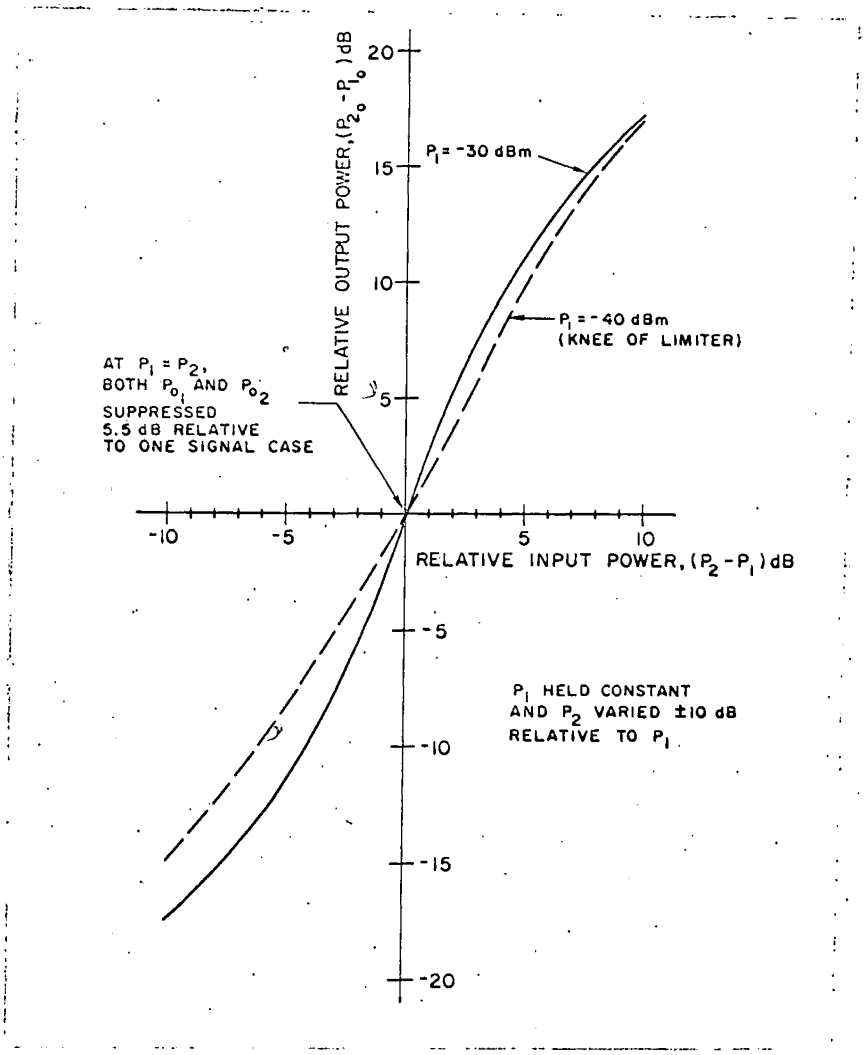


FIGURE 3-8 15 MHz LIMITER MEASURED SMALL SIGNAL SUPPRESSION DATA

3.2.2.3 Four-Quadrant Frequency Discriminator

The four-quadrant discriminator is shown in Figure 3-9. This version consists of 7 each 3 dB quarter wave couplers, a delay line of length τ, and four matched detectors. The equations for the four detected output voltages, E_{01_D} through E_{04_D} are developed in Appendix A and also given below.

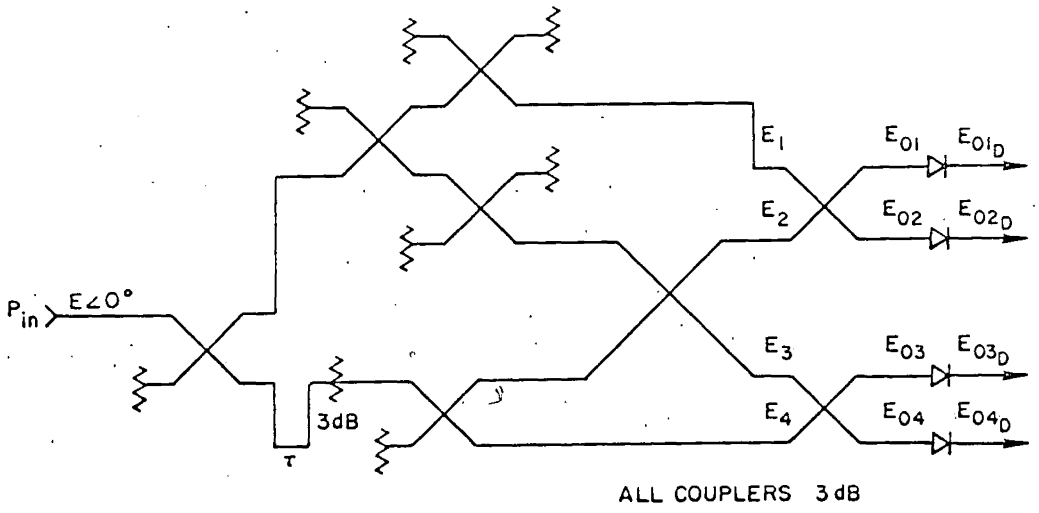


FIGURE 3-9 FOUR QUADRANT FREQUENCY DISCRIMINATOR

$$E_{01_D} = A_1 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{\sin^2\theta} + \frac{K^4\sin^2\theta}{1-K^2\cos^2\theta} - 2CK^2\left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}}\sin\omega\tau\right] \quad (3.15)$$

$$E_{02_D} = A_2 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[C^2K^2 + \frac{K^2(1-K^2)}{1-K^2\cos^2\theta} + 2CK^2\left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}}\sin\omega\tau\right] \quad (3.16)$$

$$E_{03_D} = A_3 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{K^2\sin^4\theta} + \frac{K^4\sin^2\theta}{(1-K^2\cos^2\theta)} - \frac{2CK(1-K^2)}{\sin\theta(1-K^2\cos^2\theta)^{\frac{1}{2}}}\cos\omega\tau\right] \quad (3.17)$$

$$E_{04_D} = A_4 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{\sin^2\theta} + \frac{K^2(1-K^2)}{(1-K^2\cos^2\theta)} + \frac{2KC(1-K^2)}{\sin\theta(1-K^2\cos^2\theta)^{\frac{1}{2}}}\cos\omega\tau\right] \quad (3.18)$$

and

$$\theta = \frac{\Pi f}{2f_o} \quad (3.19)$$

where:

f is the rf frequency.

f_o is the midband rf frequency.

P_{in} is the discriminator input power.

A_1, A_2, A_3, A_4 are the detector open circuit voltage coefficients (units of $\mu V/\mu W$).

K is the directional coupler voltage coupling coefficient at mid-band.

C is voltage attenuation added to the delayed path to appropriately balance the output powers (3 dB or 0.707 for the discriminator shown).

τ is the delay which determines the overall frequency sensitivity of the discriminator.

The difference voltages $(E_{02_D} - E_{01_D})$ and $(E_{04_D} - E_{03})$ are present at the outputs of the two differential amplifiers. The angle formed by the arc tangent of $(E_{02_D} - E_{01_D})/(E_{04_D} - E_{05_D})$ varies linearly with frequency. Hence, the processing of the output requires a method for preserving this angle, β, which is given below in eq. 3.20.

$$\beta = \text{Tan}^{-1}\frac{E_{02_D} - E_{01_D}}{E_{04_D} - E_{03_D}} \quad (3.20)$$

One method that is used with operator oriented equipment is the use of the polar display where the two difference voltages are applied to the vertical and horizontal plates of a CRT. This display indicates ...

frequency as the polar angle relative to a reference and the signal amplitude as the length of the radial vector. A method will be described later in this section for digitally processing this output and preserving the angle β as a digital word.

The length of the delay line, τ, determines the unambiguous frequency range over which a given discriminator measures frequency, the frequency range being inversely proportional to delay. In this application it is suggested that two discriminators be used; one with a relatively fine frequency resolution (typically 250 MHz per 360^{o}) and a second coarse discriminator with a 2 GHz or greater frequency coverage to resolve the ambiguity of the fine discriminator.

The steps to design a discriminator for a given frequency range include: 1) Adjusting the length of delay τ, and 2) designing a quarter wave coupler to be approximately centered within the desired frequency range and having the appropriate coupling coefficient. The two relationships that must simultaneously be satisfied are:

$$\tau = \frac{n}{2f_c} \tag{3.21}$$

where n is an odd interger, 1, 3, 5 ...., and when f_c is the center frequency of the band covered by one cycle of the discriminator. This insures that $\beta = 180^{o}$ at f_c. Second, to insure there are no ambiguties over the frequency band, Δf, $1/\tau > /\Delta f$ and preferably as close to equality as possible.

The design parameter for the discriminator used in this study is as follows:

a) Coarse Discriminator

The center frequency, f_c, is 6 GHz, the frequency coverage, Δf, is 2 GHz min. Therefore from the relationship above, $\tau \leq 0.5$ nsec and from eq. 3.21 n max = 6. Since n must be odd, let n = 5, then $\tau = n/2f_c = 0.417$ nsec and Δf = 2400 MHz. Also for a 3 dB coupler,

K = 0.74 and for a 3 dB attenuator, C = 0.707.

b) Fine Discriminator

It is desired that the fine discriminator repeat approximately 8 times across the 5.0 - 7.0 GHz band. Letting τ = 4 n sec, then Δf = 250 MHz and β will be 0^{o} degrees at 5.0, 5.25,.... 7.0 GHz and 180^{o} at 5.125, 5.375....6.875 GHz. Also the corresponding values of n will be 51, 53 .... 69.

Equations 3.12 through 3.15 were programmed onto a computer and solutions for the four detected output voltages E_{01_D} through E_{04_D}, the polar phase angle, β, (eq. 3.21) and the variation of β from an ideal linear discriminator were obtained. Using the parameters above for both coarse and fine discriminators, the polar angle as a function of frequency is plotted in Figure 3-10. In this case 37.5^{o} of

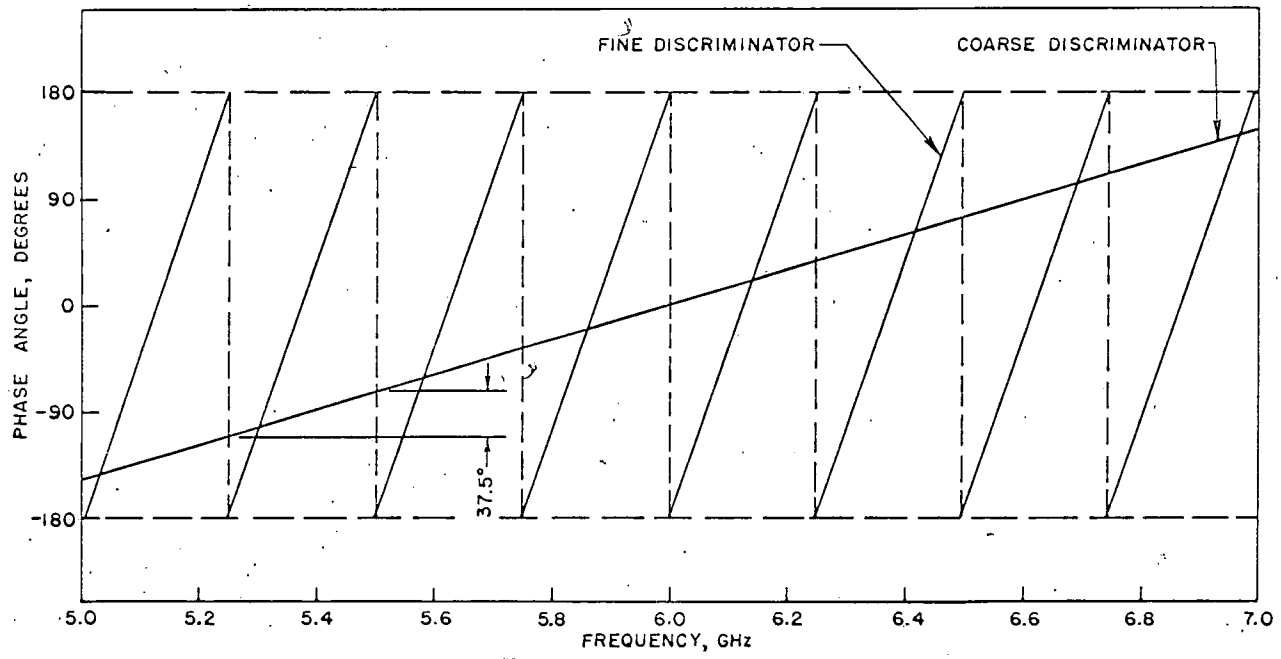


FIGURE 3-10 FREQUENCY DISCRIMINATOR CHARACTERISTICS

the coarse discriminator corresponds to 360^{o} of the fine discriminator. The angular sensitivity of the coarse discriminator is 6.6 MHz per degree and that of the fine discriminator 0.695 MHz per degree. Since

the quarter wave couplers do not have perfectly flat coupling versus frequency, the polar angle, β, deviates from the ideal linear response slightly. The variation of the frequency discriminators output polar angle from the ideal linear response is shown in Figure 3.11. The maximum peak-to-peak deviation is $\pm$ 2.3° for the coarse discriminator and $\pm$ 3.3° for the fine discriminator. This corresponds to $\pm$ 15.3 MHz and $\pm$ 2.3 MHz frequency deviation for the coarse and fine discriminators respectively.

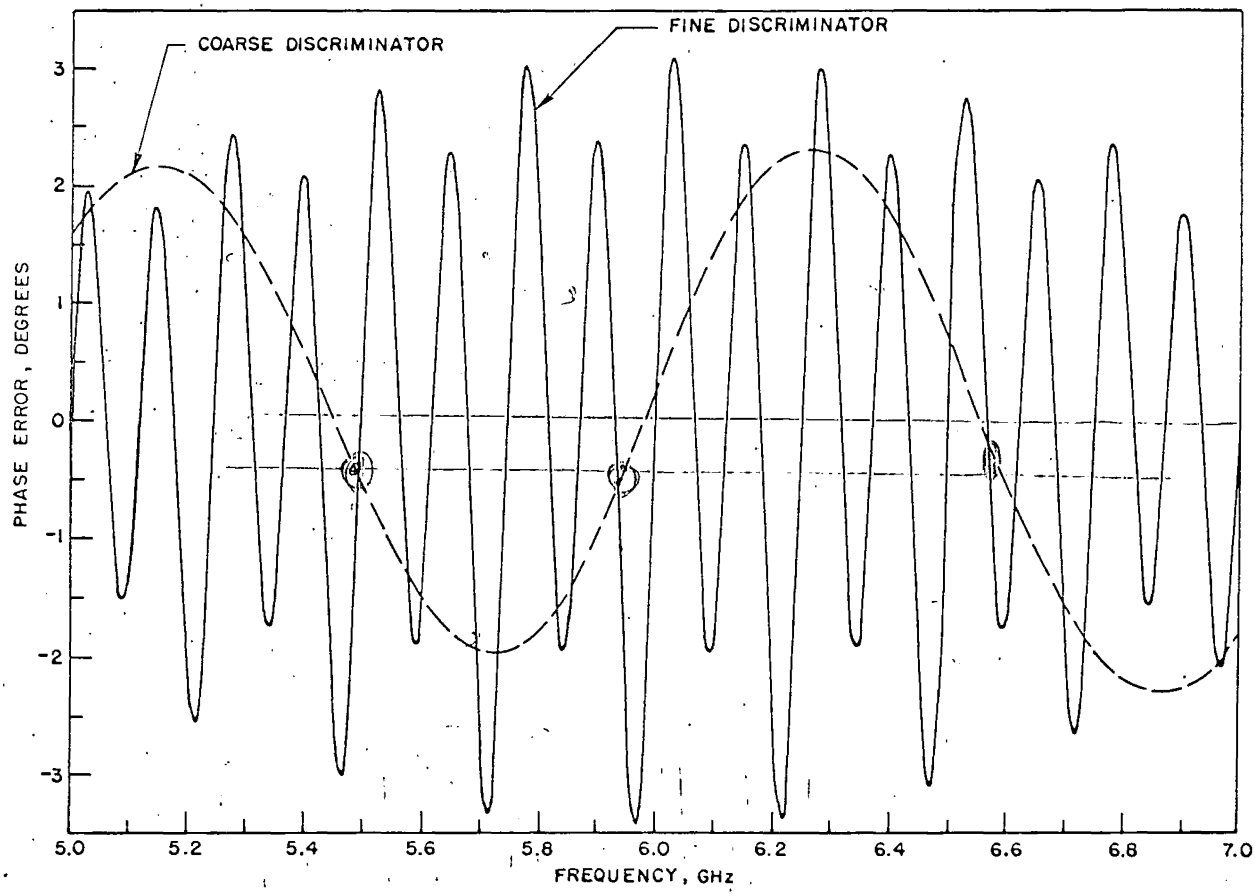


FIGURE 3-11 FREQUENCY DISCRIMINATOR POLAR ANGLE DEVIATION FROM THE IDEAL LINEAR RESPONSE

The above analysis does not include errors due to internal impedence mismatching, imperfect detector matching and temperature effects in realizing the discriminator. Experience has shown that $\pm 6^{\circ}$ deviation from linearity can be expected in an actual discriminator. Both Aertech and Anaren market this type of discriminator with angular deviations less than $\pm 6^{\circ}$. Using the above angular sensitivities, this corresponds to $\pm$ 40 MHz for the coarse discriminator and $\pm$ 4.1 MHz for the fine discriminator.

In designing the frequency measurement video processing circuitry, an attempt has been made to preserve typically $\pm 5^{\circ}$ polar angle accuracy on through to the digital output.

3.2.2.4 Frequency Measurement Errors due to Simultaneous Signals

The response of the frequency discriminator to simultaneous pulsed signals is the vector sum of the two signals. The Limiter-Discriminator shown in Figure 3-6 will generally read out the frequency of the stronger of two simultaneous signals and ignore the weaker. If the relative power level of the two signals is, however, within 3dB, there can be an error in the measured frequency, the amount of error being related to both the frequency separation of the two signals and their relative power levels. The significant point to be made here is that in a Main Beam Collection application, one signal will generally be stronger by several dB and only while flying through the crossover point between two emitter beams could erronious measurements occur. Data are given in Figure 3-12 from which the amount of error can be assessed. These data were taken on the SR-1966 S-band polar display receiver. This receiver has two discriminators, one covers a 1 GHz segment in S-band (2.4-3.4GHz) and a second sub-band discriminator covering 250 MHz. The data shown in Figure 3-12 were taken on the discriminator covering 1 GHz. Two signals separated by 100 MHz at 3000 MHz and 3100 MHz respectively were simultaneously applied to the receiver input. The data were taken both with and without a rf limiter in front of the receiver. Without the limiter it required approximately a 9dB difference in power level for a reliable frequency measurement of the stronger of the two signals.

As can be observed, with a broadband TDA limiter in front of the receiver, only a 3dB difference in power level was required for a reliable mesurement of the higher level signal. As a cross check, the measured suppression characteristics of the 15 MHz limiter given in Figure 3-8 were applied to the no limiter case and are shown as the dashed curve of Figure 3-12. The close agreement of the two curves tends to indicate that the improvement with the limiter is primarily due to the small signal suppression effects.

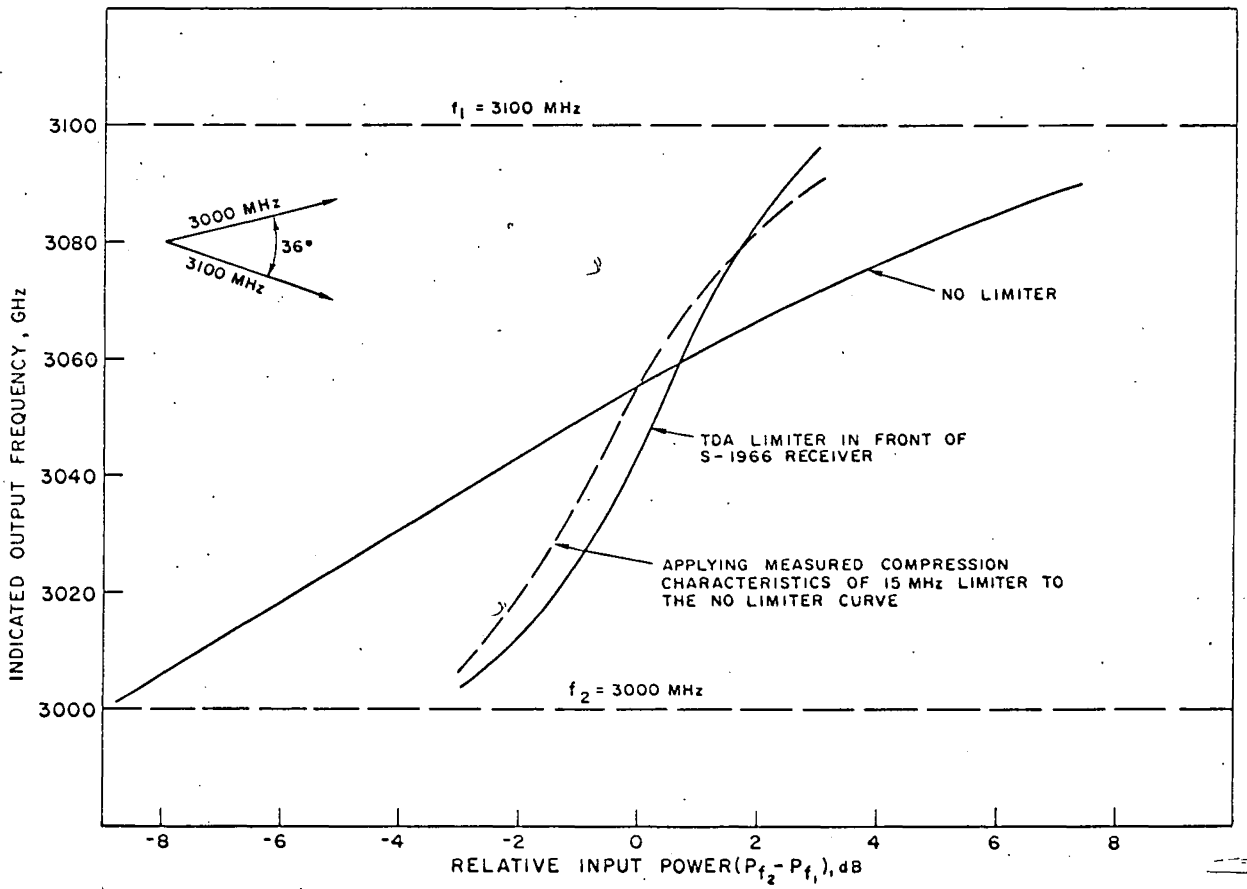


FIGURE 3-12 EFFECTS OF TDA LIMITER ON SIMULTANEOUS FREQUENCY MEASUREMENT WITH S-1966 RECEIVER

3.2.2.5 Signal to Noise Limitations on Frequency Measurement Accuracy

In C and X band, the sensitivity of the frequency measurement channel will be limited by the thermal noise generated at the receiver front end. In reference 3, it was shown that the measurement errors due to thermal noise are invariant with frequency (angular position on the polar display) and an expression was developed, (equation 3.78 of reference 3) which predicts the rms frequency error as a function of input signal-to-noise ratio and other receiver parameters. The applicable equations from reference 3 are shown below in the noise contributed Frequency Measurement Error Calculation. This development assumed both a gaussian shaped rf and video bandpass; however, it has been experimentally established that eq. 3.23 is also valid for the more conventional shaped passbands if corrections are used to relate the rms and 3 dB bandwidth (eq. 3.24 and 3.25 below).

As can be observed from either eq. 3.22 or eq. 3.26, the rms frequency error is a function of the rf frequency range covered by one cycle of the discriminator. Since the ultimate accuracy of the frequency measurement is established by the fine discriminator, the delay line length, τ, was used for the fine discriminator in the example.

Ref. 3 - Bill B May, "A Statistical Analysis of Multichannel Systems with Applications to Broadband, Microwave Frequency Discriminators (U) SEL TR No. 1962/1966-1 March 1966 Contract Nos. Nonr-235(59) and AF33(657)-11144, Stanford Electronics Laboratories, Stanford, California (Report Unclassified)

Noise Contributed Frequency Measurement Calculation

$$\Delta f = \frac{1}{2\Pi\tau W_n}\left[\left(\frac{1}{W_n^2 + W^2}\right)^{\frac{1}{2}} \frac{W W_n^2}{(S/N)_{in}}\right. \tag{3.22}$$

$$\left.\left\{1 - \exp\left[-\frac{(2\Pi\tau W_n W)^2}{2(W_n^2+W^2)}\right]\right\} + \frac{1}{(S/N)_{in}^2} \frac{W W_n^2}{2(W^2+2W_n^2)^{\frac{1}{2}}} \left\{1 - \exp.\left[-(2\Pi\tau W_n)^2\right]\right\}\right]^{\frac{1}{2}}$$

where

$$(S/N)_{in} = \frac{P_s}{\sqrt{8\Pi}\, P_n W_n F} \tag{3.23}$$

and

τ is the discriminator rf delay.

P_s is the input rf power.

P_n is the thermal noise power (-114 dBm per 1 MHz).

F is the equivalent input noise figure.

W_n is the rms rf bandwidth and is related to the rf bandwidth, B, by

$$W_n = \frac{B}{(2)(1.18)} \tag{3.24}$$

and

W is the rms video bandwidth and is related to the video bandwidth, b, by

$$W = \frac{b}{1.18}\,. \tag{3.25}$$

For

$W_n \gg W$ eq. 3.22 simplifies to

$$\Delta f = \frac{1}{2\Pi\tau W_n}\left[\frac{WW_n}{(S/N)_{in}}\left\{1-\exp\left[-\frac{(2\Pi\tau W)^2}{2}\right]\right\}+\frac{1}{(S/N)_{in}^2}\frac{WW_n}{2\sqrt{2}}\left\{1-\exp\left[-(2\Pi\tau W_n)^2\right]\right\}\right]^{\frac{1}{2}} \quad (3.26)$$

For the vernier discriminator which repeats every 250 MHz over a 2000 MHz input rf bandwidth,

$B = 2000$ MHz

$b = 5$ MHz

$\tau = 4$ nsec

$F = 9.3$ dB (8.4) in C-band and 7.2 dB (5.3) in X-band

Therefore

$W_n = 850$ MHz

$W = 4.23$ MHz

and

eq. 3.26 reduces to

$$\Delta f = \frac{0.218 \times 10^6}{\sqrt{(S/N)_{in}}}\left(1+\frac{60}{(S/N)_{in}}\right)^{\frac{1}{2}} \quad (3.27)$$

It can be observed from eq. 3.27 that the rms frequency deviation varies inversely as the input S/N ratio for small signal-to-noise ratios and inversely as the $\sqrt{(S/N)_{in}}$ for large input signal-to-noise ratios. Using the equivalent noise figures calculated in Section 3.2.1.2, and assuming 1 dB input triplexer losses, the rms frequency deviation as a function of receiver input power is given in Figure 3-13.

From Figure 3-13 it can be observed that the receiver will have a frequency measurement sensitivity of -70 dBm in C-band and -72 dBm in X-band for a 1σ frequency error due to thermal noise of 3 MHz.

The maximum signal level in this channel is determined by the saturation level of the TDA preamplifiers (-15 dBm output level). This results in a maximum receiver input level of -24 dBm in C-band and -29 dBm in X-band. This further results in an input frequency measurement dynamic range of 46 dB in C-band and 43 dB in X-band.

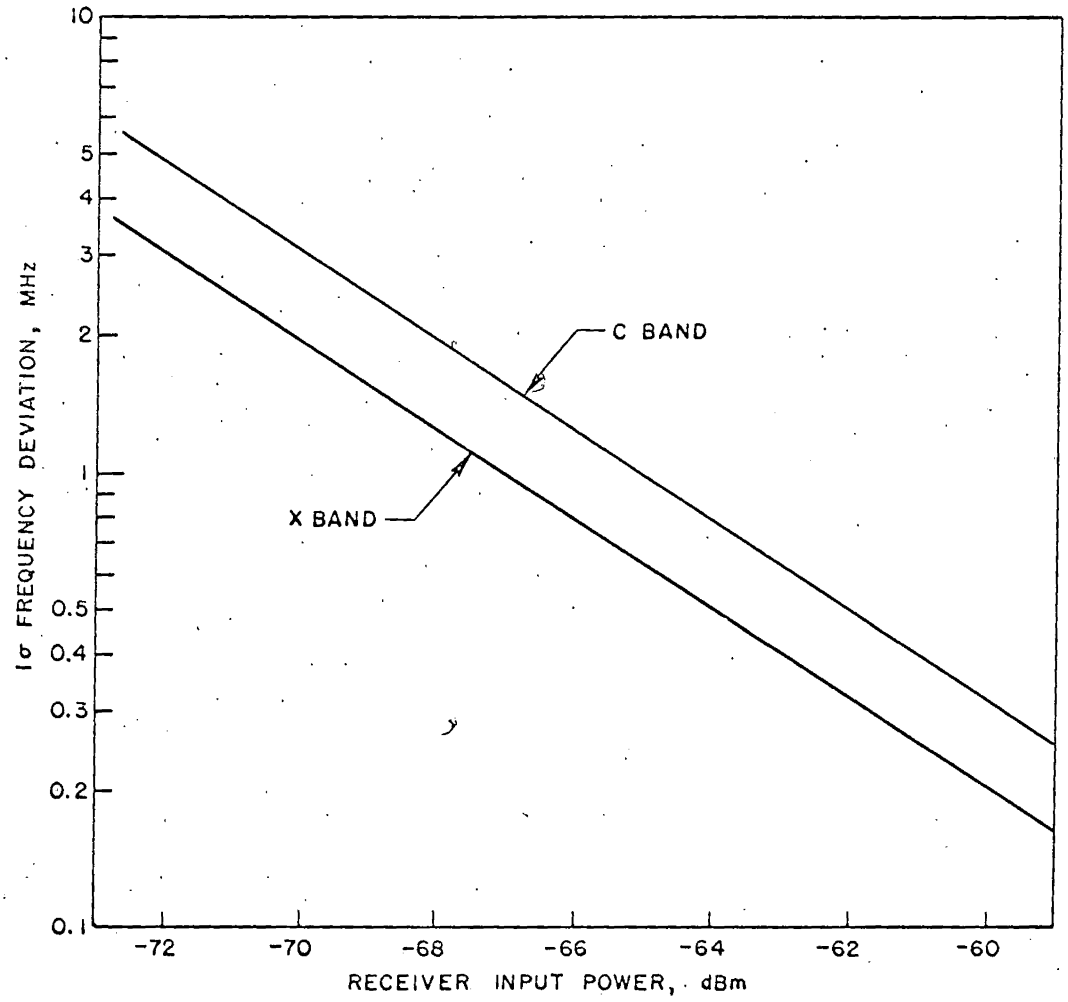


FIGURE 3-13 CALCULATED RMS FREQUENCY MEASUREMENT ERROR DUE TO THERMAL NOISE AS A FUNCTION OF RECEIVER INPUT POWER

The frequency measurement sensitivity analysis was based on a linear rf channel. That is, it assumes that the knee of the rf TDA limiter is above the level for minimum signal measurement. The limiter has been specified to have knee in its transfer characteristic at -50 dBm referred to its input (See Section 3.2.1.5).

The net rf gain from the receiver input to the TDA Limiter input is 13 dB in C-band and 17 dB in X-band. Hence, the minimum signal levels referred to the TDA Limiter input are -55 dBm in C-band and -57 dBm in X-band which are 5 and 7 dB below the knee of the limiter respectively.

3.2.3 Test Signal Generator Description

The suggested on-board Test Signal Generator is shown in Figure 3-14. Two rf oscillators at 2.1 and 3.9 GHz are alternately pulse modulated and their outputs combined and multiplied in a broadband multiplier. The output of the multiplier is then low pass filtered to pass the output frequencies given in the table of Figure 3-14. The multiplied output is divided in an 8-way power divider and coupled into the receiver using capactivily coupling T's which have a loose coupling

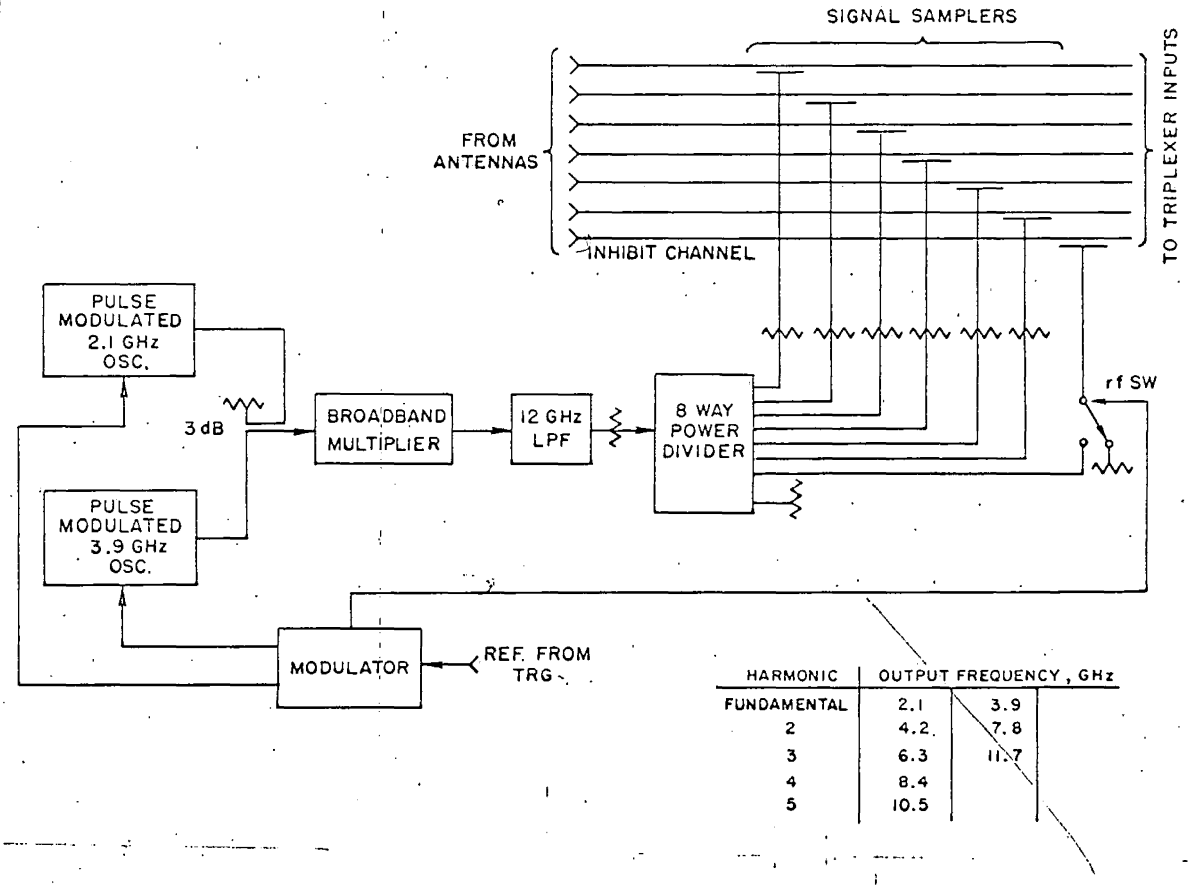


FIGURE 3-14 TEST SIGNAL GENERATOR

coefficient (> 20 dB). The response of this type of coupler through the capactive path increases with frequency approximately 6 dB per octave. Since the broadband multipliers output drops off at higher frequencies,

the amplitude response of the two tend to compensate for each other. It should be pointed out that the intent here is not to provide a precise relative power calibration but rather a precise PRI, Pulse Duration, and two point Frequency calibration in most of the bands. A more elaborate on-board calibration which would calibrate the gain match of the six rf channels was considered. However, due to the large complexity of precisely dividing the power 8 ways and then coupling it into the rf inputs over a frequency range of greater than 5:1 discouraged this type of calibration. It is suggested that on-orbit ground based calibrations perform this function.

The timing of the modulator which controls both oscillators and the rf switch in the inhibit channel is shown in Figure 3-15. The basic pulse rate is 1 KHz which is in sync with the TRG. The 2.1 GHz and 3.9 GHz oscillators are pulsed by alternate groups of two pulses. By closing the switch to the inhibit channel at a 500 pps rate, half the pulses from

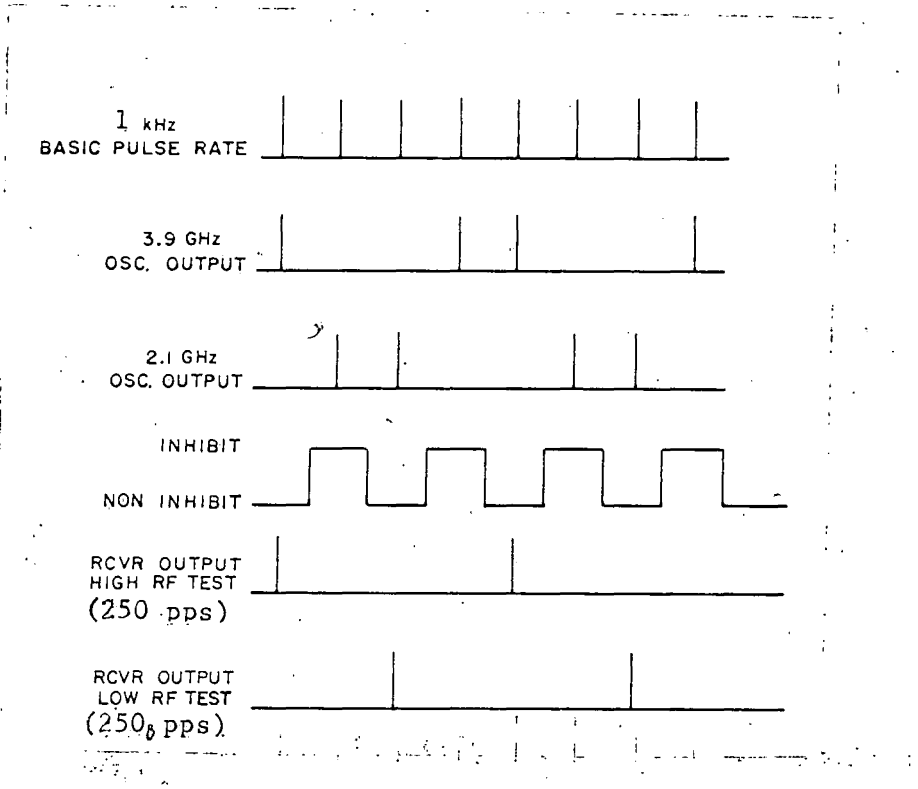


FIGURE 3-15 TEST SIGNAL GENERATOR TIMING WAVEFORMS

each of the oscillators will be inhibited and the resulting output will be two 250 pps pulse trains staggered one-half interpulse interval. During Read-In the Test Signal Generator is excited for a 360 ms interval once per minute again controlled by the system TRG.

The relative power level of the TSG should be tapered slightly to give ratio measurements other than zero. Since only the three highest channels will be read out (see Section 3.3), it may also be desirable to insert a two level attenuator in the power divider associated with three of the channels and switch its level on alternate TSG bursts. This will allow all channels to be checked on two TSG bursts by alternately measuring sets of three.

3.3 DF VIDEO PROCESSING TECHNIQUE

3.3.1 Description of Inputs and Outputs

Figure 3-16 is a functional diagram of the DF VIDEO PROCESSOR Section of the receiver.

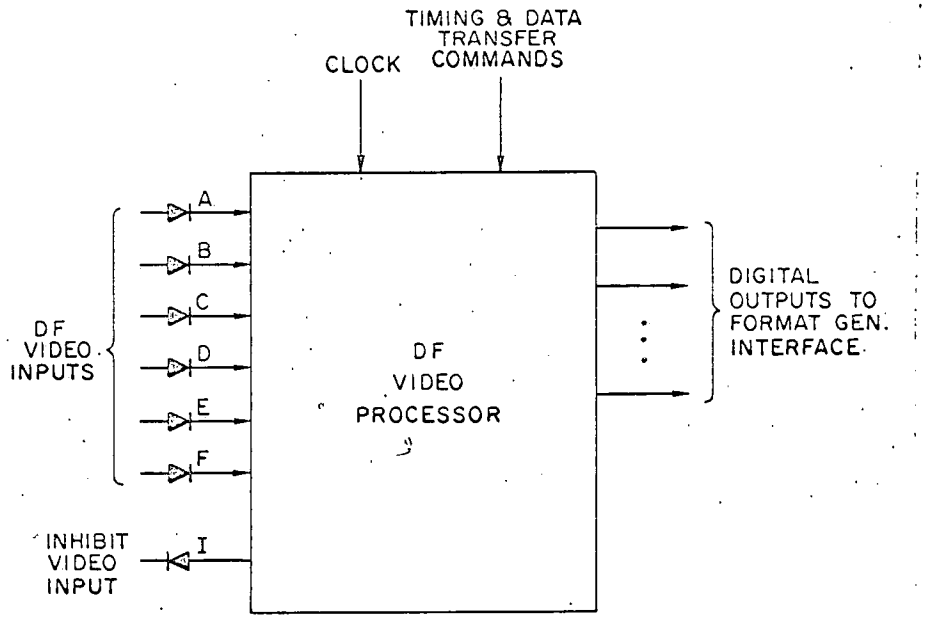


FIGURE 3-16 DF VIDEO PROCESSOR FUNCTIONAL DIAGRAM

Inputs

The inputs to this section of the receiver are detected video signals from the six DF antenna RF/IF channels and the detected video signal from the INHIBIT antenna RF/IF channel.

Other inputs are the various clock waveforms and data timing and transfer commands.

Operation

The basic function of the DF VIDEO PROCESSOR is the processing of the six DF VIDEO inputs to provide a digital DF WORD on a pulse by pulse basis. The PROCESSOR determines which three of the six DF VIDEO inputs are highest in amplitude and stores the absolute amplitude of the highest channel and the amplitudes relative to the highest of the

second and third highest channels. Also stored is which channel (A B C D E or F) is highest, which is second and which is third. As described in Section 2.1 above, this is the information required for the amplitude monopulse DF measurement.

Outputs

The output of the DF VIDEO PROCESSOR is a sequence of binary bits containing the amplitude power ratios and orders described above. Upon command, this data is transferred to the DATA FORMAT GENERATOR to make up part of the OUTPUT PCM WORD.

The DF VIDEO PROCESSOR/FORMAT GENERATOR interface logic operates on the DF PROCESSOR output to optimize the number of bits required for the DF information and provides the serial format required by the FORMAT GENERATOR.

3.3.2 DF Ratio Taking Technique

Implementation of the DF amplitude monopulse measurement requires taking amplitude ratios between several channels; this is commonly done using logarithmic video amplifiers in each channel and forming the output $\log A - \log B = \log \frac{A}{B}$. This method of ratio taking is susceptable to errors resulting from non-ideal log transfer functions and transfer function variation with temperature. The exponential ratio taking technique described below is offered as an alternative to the use of log amplifiers and has several advantages which should allow realization of higher accuracy in a practical system. Linear amplifiers are used in the exponential approach, and with sufficient feedback excellent gain stability and linearity can be maintained over large temperature ranges. Also, the nonlinear function required (i.e. a decaying exponential sweep) is generated by a passive R-C network and can be made very stable with temperature. Finally, the dynamic range of the output is compressed after stretching (which is accomplished at the linear amplifier output), resulting in minimum errors resulting from non-ideal pulse stretchers.

The basic technique chosen for taking the DF channel power ratios is illustrated in Figure 3-17. The square-law detected videos are amplified linearly so that the various channel output voltage levels are directly proportional to input power. For example, the voltage (rf power) levels corresponding to a particular direction-of-arrival might be distributed as indicated in the illustration (Figure 3-17). The power level differences are converted to time differences by applying each video output to a comparator and comparing it with a decaying exponential sweep which starts at a pre-determined reference level P_{ref}. Because the sweep is exponential

$$t_1 - t_0 \propto \log \frac{P_{ref}}{P_A}$$

$$t_2 - t_0 \propto \log \frac{P_{ref}}{P_B}$$

$$t_3 - t_0 \propto \log \frac{P_{ref}}{P_C}$$

} refer to Figure 3-17

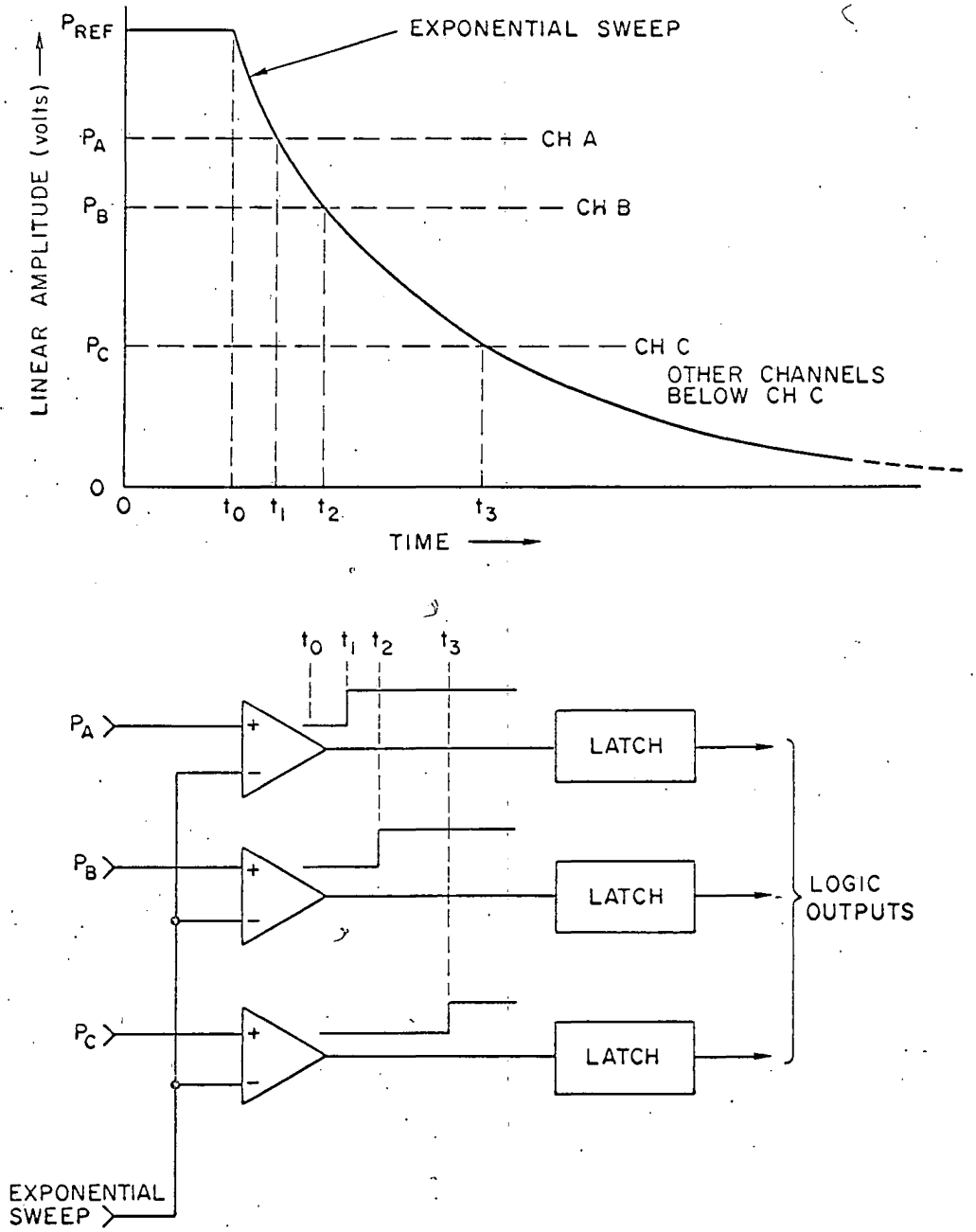


FIGURE 3-17 EXPONENTIAL SWEEP RATIO-TAKING TECHNIQUE

Since the sweep time constant is known, a constant k (dB/μs) may be determined such that

$$\frac{P_{ref}}{P_A} = k\,(t_1 - t_0)\ \text{dB, etc.}$$

By gating on simple binary clock pulse counters during the times $t_0 \rightarrow t_1$, $t_1 \rightarrow t_2$ and $t_2 \rightarrow t_3$, the channel power levels may be easily converted to a digital format.

3.3.3 DF Video Processing Requirements

Dynamic Range and Sensitivity

The dynamic range is limited on the low-signal end by the sensitivity of the detectors and the receiver front end noise level. To approximately determine the lower signal level the front end noise can be neglected. Further assuming the use of tunnel diode detectors and a video bandwidth of B_v = 5 MHz, calculations and measurements verify that for a (S/N) out = 14 dB, the required IF power to the detector input is -47 dBm. Assuming a Gaussian amplitude distribution for the noise at the video output, (see Figure 3-18) the measured power level will be within 2σ of the mean value 95% of the time; thus 95% of the time, for a -47 dBm signal, the measured level will be between -49.2 dBm and -45.5 dBm, with a maximum error of 2.2 dB. This number has been chosen as the minimum signal level for which a DF measurement will be accepted; thus, -47 dBm is the lower limit of the measurement dynamic range. It should be noted that this error is computed for the matched bandwidth case; for pulses longer than $\frac{1}{2(BW)}$ sec., the S/N could be improved by signal integration or averaging.

The tunnel detector response changes from square-law to linear at higher power levels; typically, deviation from square-law is 1 dB at an input power level of -12 dBm. If it is desired that the system operate only over the square-law range of the detector, the upper limit on dynamic range is approximately -12 dBm, giving an overall range of 35 dB.

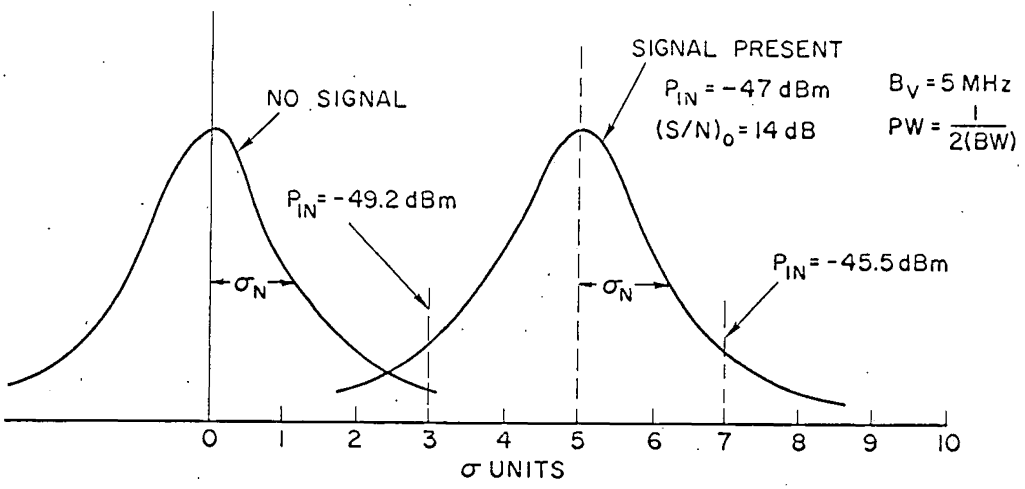


FIGURE 3-18 ASSUMED VIDEO NOISE AMPLITUDE DISTRIBUTIONS (IN ABSENCE OF FRONT END NOISE)

There is no fundamental reason to prevent using the detector above the square-law region (i.e. in the linear region). If this were done, the dynamic range could be considerably extended on the high signal end; in this case, Schottky barrier detectors would probably be employed since they have a larger overall dynamic range than tunnel diode detectors. One possibility would be to add a third segment to the linear amplifiers which could then be used for measurements on signals in the linear range of the detector characteristic.

Accuracy

The fundamental limit on measurement accuracy of the detected video signals is the S/N of the pulses being measured. Other errors will result from deviation from ideal response in the PROCESSOR electronics; these errors will be discussed in more detail in Section 3.3.5.5.

Processor Speed

The time it takes to make a measurement, the measurement resolution and accuracy, and the complexity and cost of the PROCESSOR are all interrelated. Since the overall receiver system must make

several measurements besides the DF measurement, and eventually report all of these in the form of a long serial word, speed is not of over-riding importance; other measurements can be made and read out while the DF measurement is in progress. This technique is reasonably fast (20 - 30 μs measurement and conversion time) and provides high resolution and accuracy with moderate complexity.

Digital Output

The eventual receiver output is a PCM serial word; as mentioned above the conversion of power ratios to time differences by the PROCESSOR lends to simple A/D conversion with the use of a gated counter.

3.3.4 DF Video Processor Block Diagram

Figure 3-19 is a block diagram of the DF VIDEO PROCESSOR; the general block diagram will be examined first with more detailed discussion and diagrams to follow in subsequent sections.

The seven detected IF signals (DF channels A through F plus inhibit) are first amplified by low-noise Post Detection Amplifiers (PDA's) and then the DF signals are amplified by two-segment, limiting, linear video amplifiers. The outputs of the PDA's including the inhibit channel, are summed into a bipolar logarithmic video amplifier (LVA) to provide the inhibit video.

Two-Segment Limiting Video Amplifiers

The two-segment video amplifiers each have two outputs at different gain levels; the use of two segments, rather than a single linear output, allows the following circuits (pulse stretchers, etc.) to operate over a limited dynamic range to obtain high accuracy. The output of each segment is used over an RF input range of approximately 17 dB, to cover the range of input powers from -47 dBm to -12 dBm.

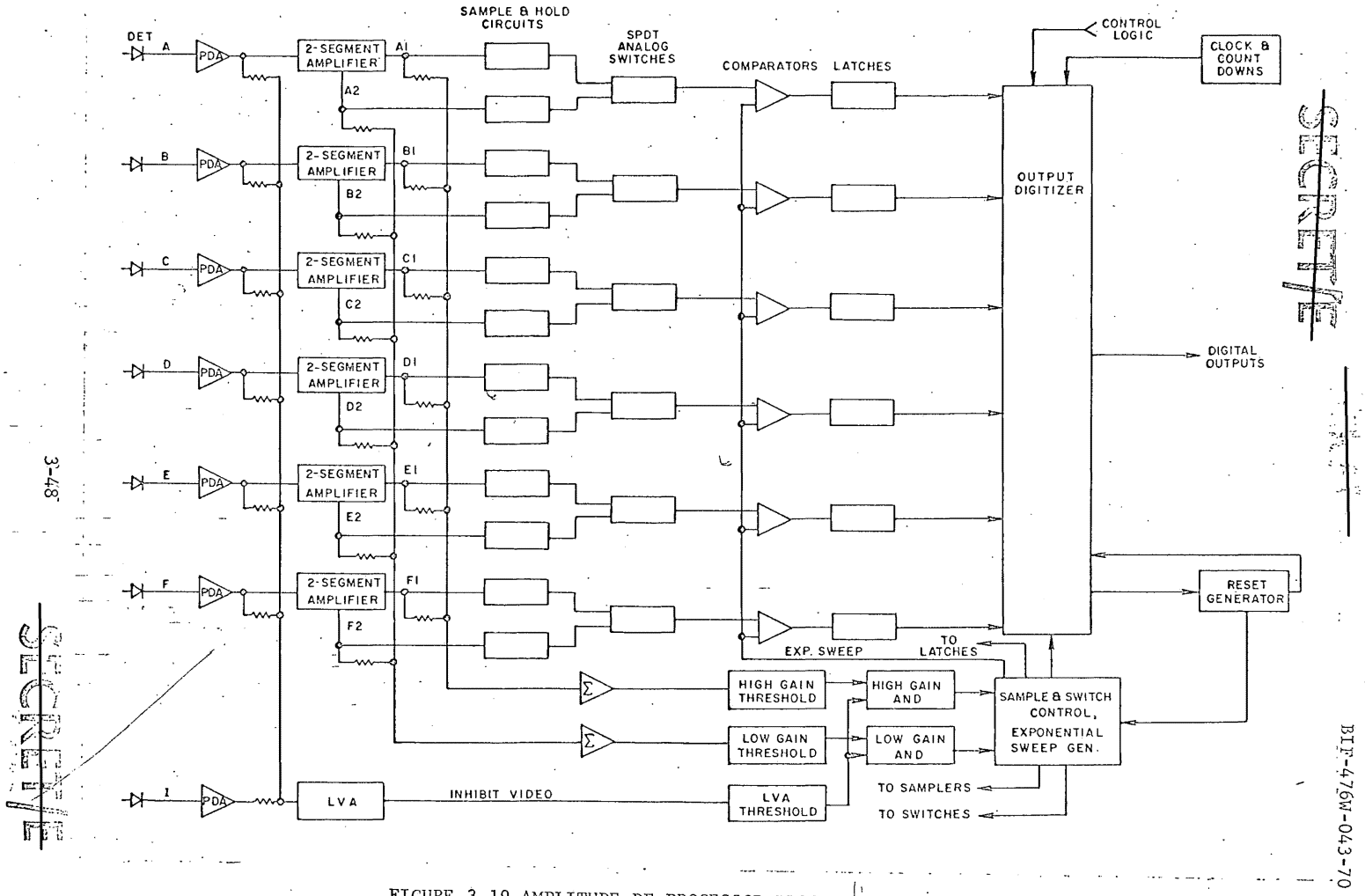


FIGURE 3-19 AMPLITUDE DF PROCESSOR BLOCK DIAGRAM

Measurement Thresholds

Both the high and low gain outputs (A1 through F1 and A2 through F2) are summed to provide both high and low gain sum video. These sum videos plus the inhibit video are used to decide if a signal is present and to initiate the proper measurement sequence.

Measurement Control Logic

If a valid signal pulse appears, either the high gain or both the high and low gain video outputs are sampled and held for processing. The analog switches select either the High Gain (HG) or Low Gain (LG) video for processing (the same segment on all channels) and the switch positions are controlled by the signal power level range as determined by the high and low gain threshold gates. Once the proper sampled levels have been applied to the comparator inputs through the analog switches, the exponential sweep starts and, as the various comparators change state, they set their respective latches (refer again to Figure 3-17).

In actual operation, the sweep continues only until three latches are set (since only the highest three channels are of interest). If the input signal is low-power, the analog switches will be set so that the high-gain segments are swept first and the sweep will continue into the noise if necessary to pick up a third channel. For high level signals, the low-gain segments will be swept first; if three channels are measured during this sweep, the answer is read out and the PROCESSOR is reset; if, however, three channels are not measured, the switches will switch to the high segment, the sweep will be reset and started again, and will continue until the third channel is measured.

A/D Conversion

The output digitizer converts the analog time information, which contains the channel power levels, into digital format and stores the channel power level order information. The power levels are coded by starting and stopping counters at the appropriate times as determined by the sweep start and comparator output times. The channel order information

can be stored in many ways, one of which is discussed below in Appendix C.

Format Generator Interface

The output digitizer formats the power level and channel order information into a digital serial word and clocks this word to the output DATA FORMAT GENERATOR on command.

3.3.5 Five Channel Breadboard

A five channel (4 DF Channels plus inhibit) breadboard was designed and constructed to verify feasibility of the critical circuits and to make performance measurements on the DF VIDEO PROCESSOR. Except for the number of channels and the digital output format, this breadboard operates in the same manner as the 7 channel system described in Section 3.3.4 above. The breadboard circuit schematics are presented in Appendix B.

Amplifiers and Exponential Sweep

The transfer curve for the two-segment video amplifier is shown in Figure 3-20 and the exponential sweep start voltage is indicated on the figure at a voltage corresponding to P_{in} = -12 dBm. Depending on the time constant of the sweep, the sweep voltage will decay k dB/μs.

From the figure, it can be seen that the sweep start voltage determines the start power level, either -12 dBm on the low gain segment or -29 dBm on the high gain segment. Since in some cases both segments must be swept to measure the three signals desired, the stop power (voltage) level on the low gain segment should correspond to the start power level on the high gain segment. The stop power level is determined by the sweep period (T) and the sweep k from the relationship

$$P_{stop} = P_{start} - k\ (dB/\mu s)\ T\ (\mu s)$$

Normally T would be chosen based on other considerations (i.e. resolution, comparator BW, etc.) and k (the sweep time constant) would be adjusted to give the desired tracking between the two segments.

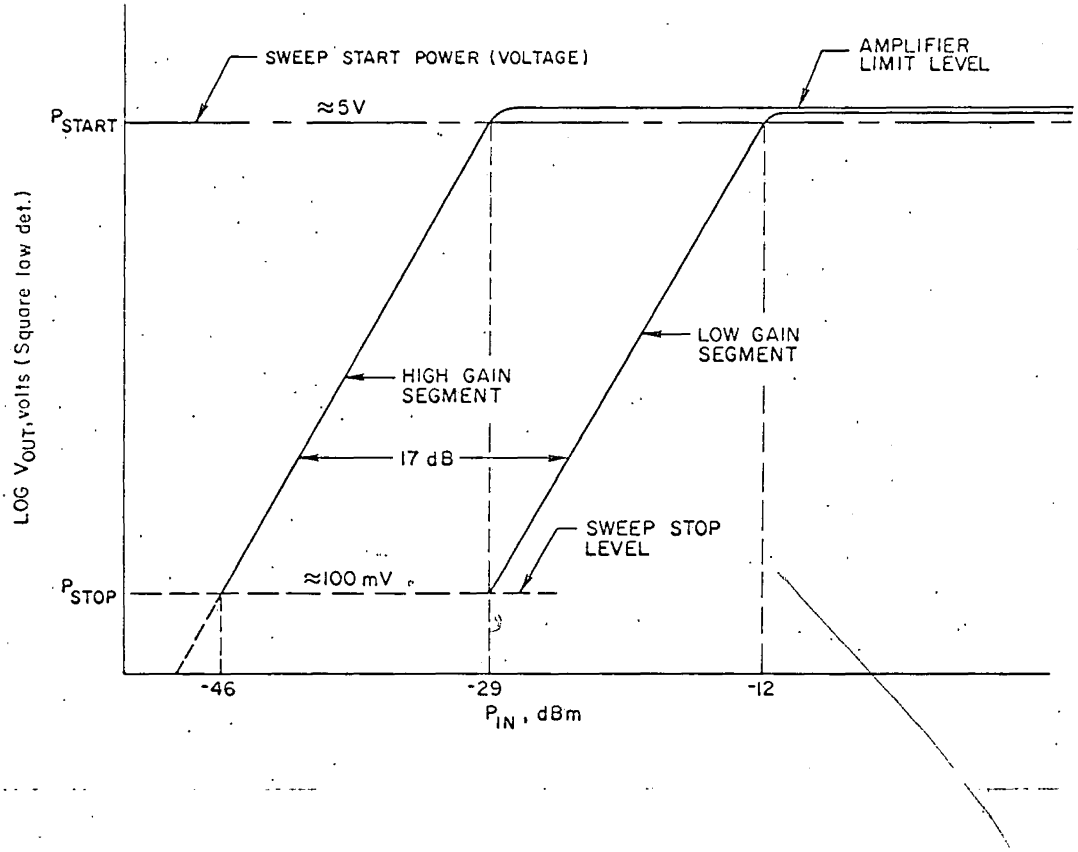


FIGURE 3-20 TWO SEGMENT VIDEO AMPLIFIER TRANSFER CURVES

Thus when sweeping the low gain segment, the sweep stops at P_{stop} = -29 dBm; however, when sweeping the high gain segment, the sweep is allowed to go into the noise if necessary to measure the lowest level signal. A more detailed diagram of the measurement and sweep control logic is shown in Figure 3-21 and is discussed below.

Measurement Logic and Waveforms

The high gain and low gain thresholds are combined in AND gates with the LVA (inhibit) threshold one-shot (≈2.5 μs period). The sample and hold circuits are activated by the trailing edge of the AND outputs; thus for pulses shorter than the LVA/one-shot period the sampling will occur just prior to the trailing edge. For longer pulses the sample will be taken at the end of the LVA one-shot period.

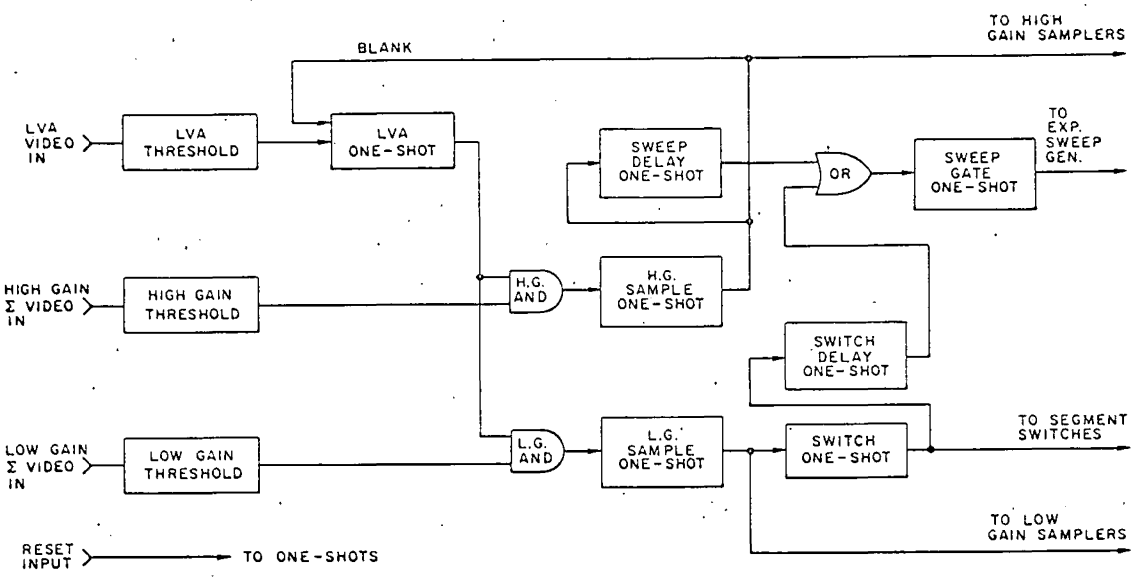


FIGURE 3-21 DF VIDEO PROCESSOR CONTROL LOGIC

For low level signals, only the high gain AND will have an output, which will cause the high gain samples to be held and the sweep delay one-shot to be triggered (see example waveforms of Figure 3-22). At the end of the sweep delay one-shot period (≈ 2 μs), the sweep gate starts the exponential sweep. When three signals are measured by the comparators, a reset is generated and the cycle is over.

For high power signals, both the high gain AND and the low gain AND will have outputs, triggering the HG and LG samplers and the sweep delay and switch one shots. When the sweep starts, the low gain segment will be swept first because of the state of the switch one-shot. If three signals are collected, a reset will be generated. If three are not collected, the sweep will run out its natural period (to -29 dBm) and then fly back; the switch one-shot natural period is slightly longer and when it ends the switch delay one shot is triggered which restarts the sweep approximately 2 μs later. The sweep now sweeps the high gain

segment until a total of three channels have been measured. (See the waveforms of Figure 3-22).

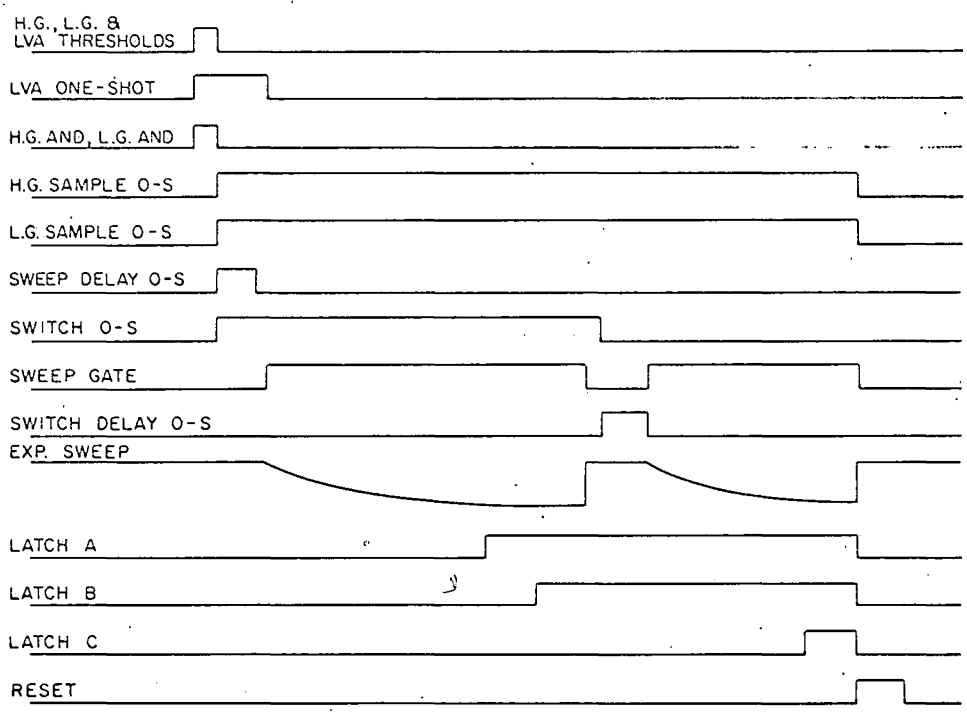


FIGURE 3-22 DF VIDEO PROCESSOR WAVEFORMS

Digital Outputs

For the breadboard system a parallel BCD output format was adopted for convenience in manual data reduction. The diagram of Appendix B, Figure A4, shows the A/D conversion section of the breadboard. In a system where a binary serial word output was desirable, the decade counters would be replaced by binary counters and the storage latches by parallel-to-serial converters for clocking to the formatting logic. A binary output format, including a method for generating the channel order word, is discussed in Appendix C.

In the breadboard DF PROCESSOR system, the digital outputs are parallel BCD with a separate order readout code.

The power received in each channel is read out as a BCD count stored in a memory latch which drives a BCD light display. The transfer curve relating the digital count to input power level is shown in Figure 3-23. The two curves of Figure 3-23 correspond to measurements made on the high gain (approx. -29 to -45 dBm) and low gain (approx. -13 to -29 dBm) amplifier segments. A single extra bit is used to indicate which segment was swept first (i.e. the reference power level).

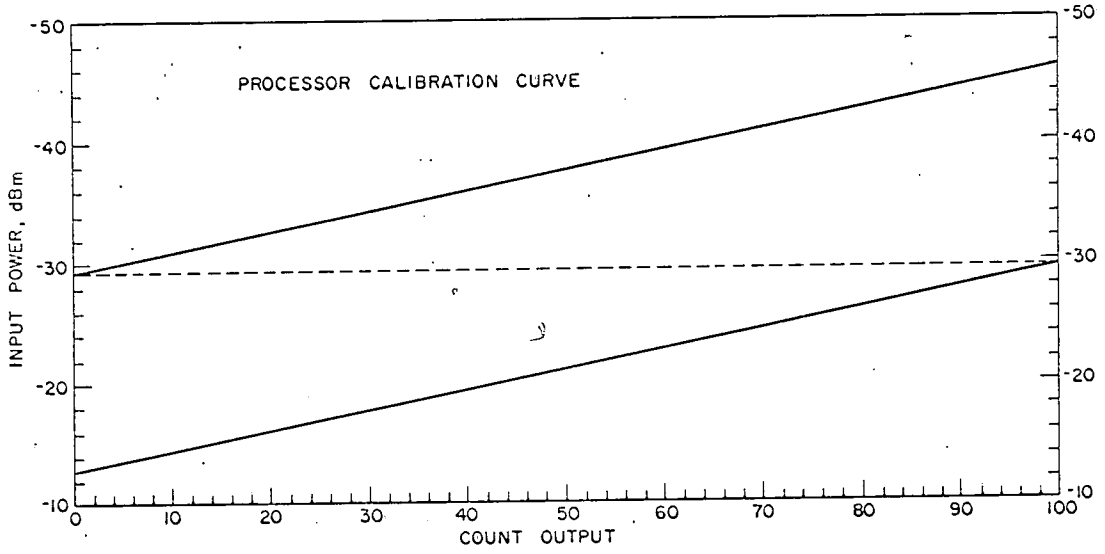


FIGURE 3-23 DF VIDEO PROCESSOR CALIBRATION CURVE

The order information is encoded with binary bits (and appropriate lights) to indicate the highest, second and third channels.

3.3.5.1 Output Calibration Data and Channel Tracking Measurements Calibration Data

The digital power readout consists of three counts; the first count corresponds to the absolute power level of the highest channel which can be determined directly from the calibration curve of Figure 3-23. For example, a count of 41 plus a high-gain segment indication indicates a power level of -36 dBm. The second count indicates the power level relative to the highest channel (i.e. a first count of 41 and second count of 19 would indicate first and second channel power

levels of -36 dBm and -39.1 dBm). The third count gives power relative to the second channel.

Channel Tracking Measurements

Data were taken with the three highest channels separated 3 dB in power level and the absolute power level (high channel) was varied from -49 dBm to -10 dBm (low channel-46 dBm to -16 dBm). A plot of the data is shown in Figure 3-24.

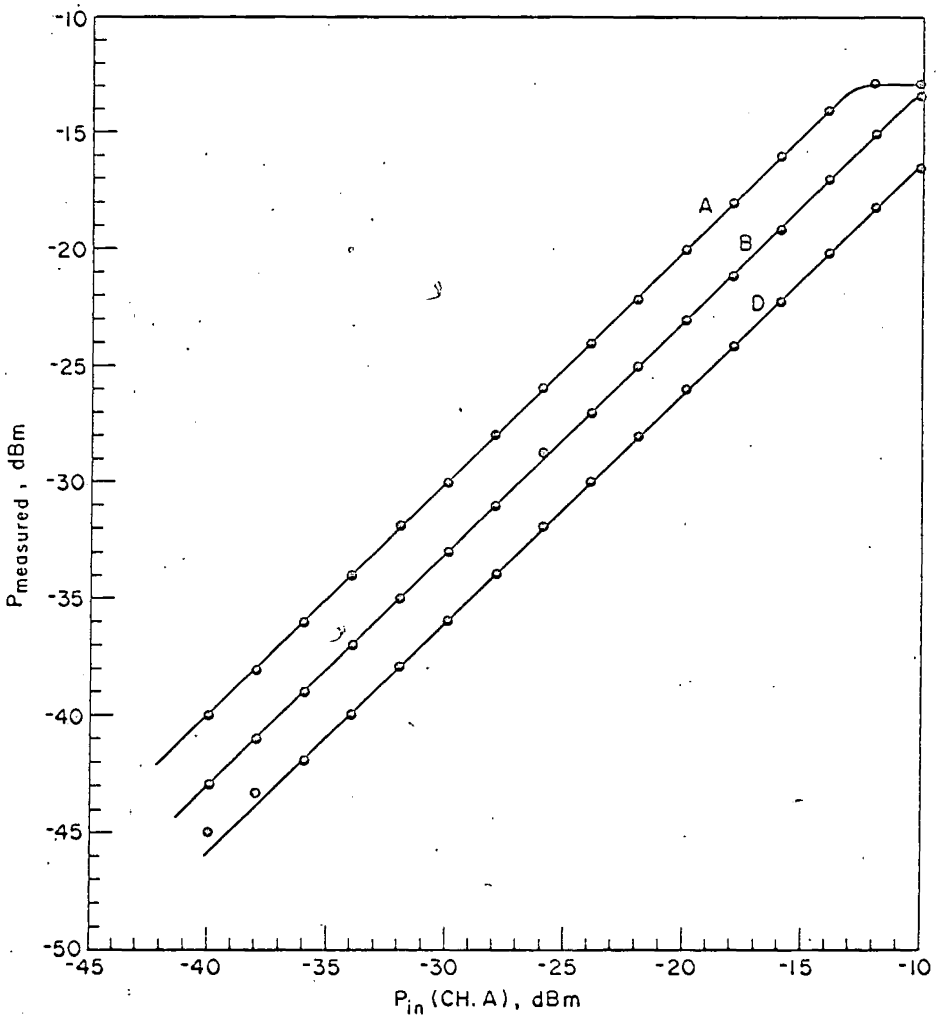


FIGURE 3-24 DF PROCESSOR CHANNEL-TRACKING

It should be mentioned that these are not averaged data but rather measurements of a single pulse; this accounts for the large errors in the measurement of Ch. D at -44 dBm and -46 dBm. These same data which were used in plotting Figure 3-24 are presented in Figure 3-25, where the difference in measured power level from the expected value is plotted versus the power level of Channel A.

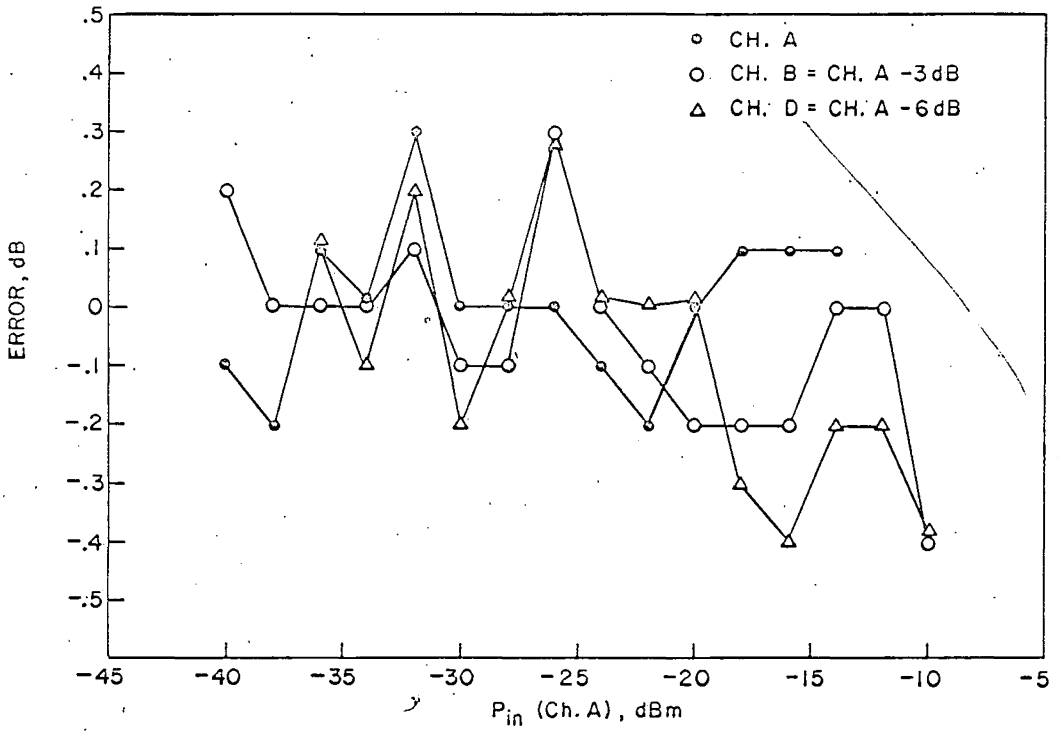


FIGURE 3-25 DEVIATION OF MEASURED POWER FROM TRUE INPUT

To determine the performance of the ratio taking circuit at very low S/N, a number of measurements were made on Channel D, with the input power to Channel D set at -45 dBm, -47 dBm and -49 dBm.

In each case, at least 20 pulses were measured; Figure 3-26 presents amplitude histograms of the data points, plotted versus deviation in dB from the expected values of -45, -47 and -49 dBm. The average of the measurements is also indicated for each of the three

cases. The deviation of 0.6 dB for Pin = -49 dBm is attributed to processor errors (i.e.d.c. drifts and non-linearities).

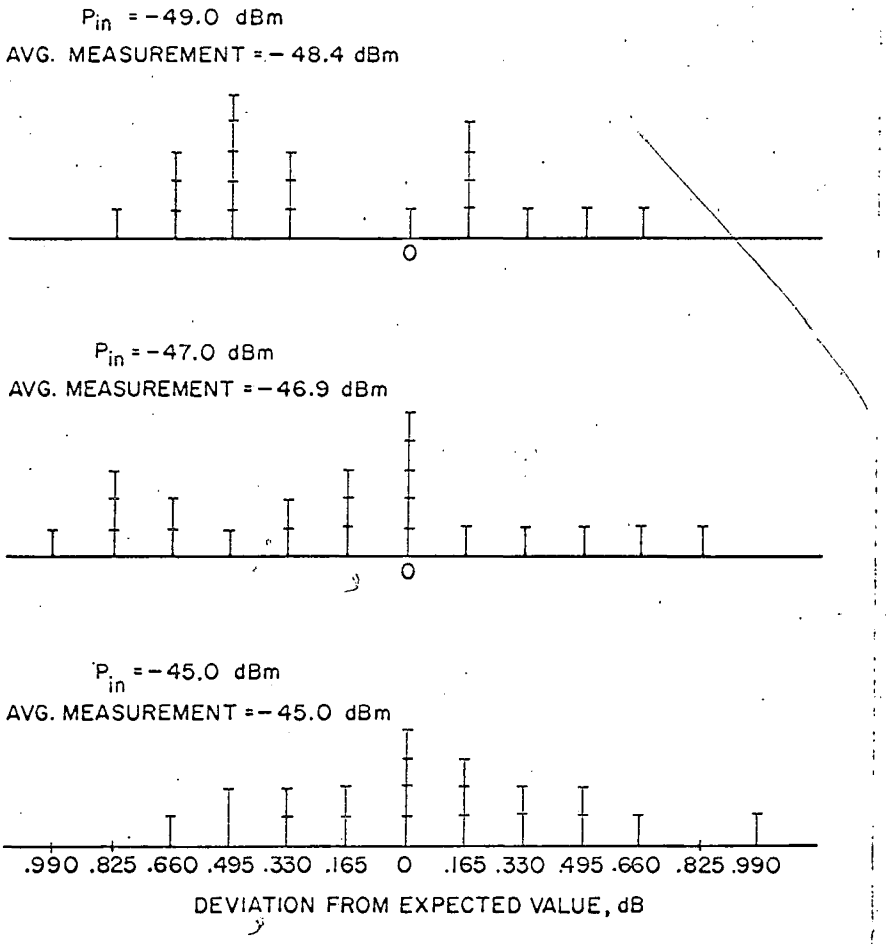


FIGURE 3-26 LOW S/N AMPLITUDE HISTOGRAMS

From the data collected the 1σ video processor error is estimated as 0.14 dB at high $S/_N$ and 0.82 dB at $S/_N$ = 14 dB.

3.4 FREQUENCY MEASUREMENT VIDEO PROCESSING TECHNIQUE

3.4.1 Interpreting the Broadband Frequency Discriminator Output

The outputs of the frequency discriminator, after subtracting and amplification, are two voltages of the form

$$V_x = A \sin 2\Pi f\tau$$

and

$$V_y = A \cos 2\Pi f\tau,$$

where A is proportional to signal amplitude, f is the signal r.f. (or i.f.) frequency, and τ is a constant associated with the discriminator. The amplitude A can be eliminated from the relationship between V_x, V_y and f by dividing V_x by V_y to form the equation

$$\frac{V_x}{V_y} = \frac{A \sin 2\Pi f\tau}{A \cos 2\Pi f\tau} = \tan 2\Pi f\tau,$$

thus

$$2\Pi f\tau = \tan^{-1} \frac{V_x}{V_y},$$

or

$$f = \frac{1}{2\Pi\tau} \tan^{-1} \frac{V_x}{V_y}.$$

If V_x and V_y are considered vectors in the X-Y plane, then the frequency f can be considered proportional to the angle β as indicated in the diagram of Figure 3-27.

The second relationship is the basis for the polar instantaneous frequency display, where V_x and V_y are applied to the X and Y deflection plates of a CRT.

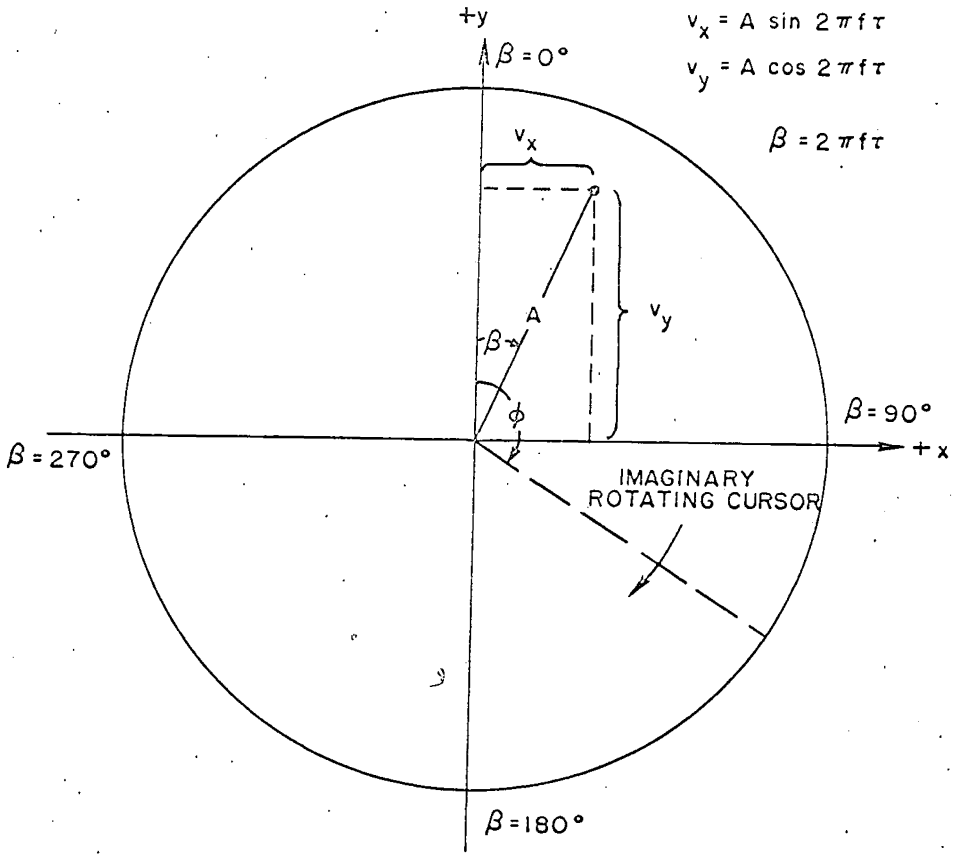


FIGURE 3-27 POLAR FREQUENCY DISPLAY

3.4.2 Possible Readout Techniques

Several methods, which are discussed below, may be used to preserve the discriminator output in digital form.

Digitization of V_x and V_y

The most straightforward method of reading out the discriminator is to digitize V_x and V_y; this, however, would require more bits than necessary to define the frequency and would necessitate the recombination of these two voltages to determine f.

Digitize Tangent of $\frac{V_x}{V_y}$ ~~or~~ of $\frac{V_y}{V_x}$

The tangent function relates to the frequency, but the disadvantages in digitizing tangent $\frac{V_x}{V_y}$ are the large dynamic range required and the necessity of performing a division of V_x by V_y and the conversion from tangent β to f.

Digitize β (or frequency) directly

If a digital output which is a direct measurement of the angle β can be generated, this output will be directly related to frequency so that the number of bits required for the measurment will be minimized and the output can be interpreted directly in terms of frequency.

A technique for digitizing β directly has been devised and is described in the following section. This method appears to offer several advantages over the previously discussed approaches; these include direct digitization of frequency and a reasonably straightforward processing approach which should be capable of yielding high-accuracy measurements.

3.4.3 Analog Multiplication A/D Conversion Technique

Basic Approach

Consider the polar frequency display of Figure 3-27 where the signal components V_x and V_y indicate the presence of a signal at frequency $f = \frac{1}{2\Pi\tau}\beta$, where $\beta = \tan^{-1}\frac{V_x}{V_y}$. If the signal components are multiplied by two sine waves, B sin $\emptyset$ and B cos $\emptyset$, two voltages result:

$$V_1 = (A \sin 2\Pi f\tau \; B \cos \emptyset) \tag{3.28}$$

and

$$V_2 = (A \cos 2\Pi f\tau \; B \sin \emptyset). \tag{3.29}$$

These equations may be rewritten as,

$$V_1 = \frac{AB}{2}\left[\sin(2\Pi f\tau + \emptyset) - \sin(\emptyset - 2\Pi f\tau)\right] \tag{3.30}$$

and

$$V_2 = \frac{AB}{2}\left[\sin(2\Pi f\tau + \emptyset) + \sin(\emptyset - 2\Pi f\tau)\right]. \tag{3.31}$$

Subtracting V_1 from V_2 we obtain:

$$V_2 - V_1 = AB \sin(\emptyset - 2\Pi f\tau), \tag{3.32}$$

or since $\beta = 2\Pi f\tau$,

$$V_2 - V_1 = AB \sin(\emptyset - \beta). \tag{3.33}$$

The angle $\emptyset$ is actually a function of time; in fact, the voltages B sin $\emptyset$ and B cos $\emptyset$ can be visualized as producing on a polar display a rotating cursor making an angle $\emptyset$ with respect to the 0 deg. reference and making one revolution per cycle of the sine wave Bsin $\emptyset$. The key to digitizing β is the observation that $(V_2 - V_1)$ changes sign when $\beta = \emptyset$ (β is constant for a given signal and $\emptyset$ is rotating at some fixed angular velocity). If a counter is started when $\emptyset = 0$ degrees (some reference position) and stopped when $V_2 - V_1$ changes sign (when $\beta = \emptyset$), the count accumulated will be a direct measurement of the angle β, and therefore frequency.

Circuit Implementation

A diagram of the circuits required to generate a digital frequency readout from a broadband instantaneous frequency discriminator is shown in Figure 3-28.

The outputs of the frequency discriminator are sampled and held and applied to analog multipliers. Also, two reference waves 90° out of phase are generated (B sin $\emptyset$ and B cos $\emptyset$) at a frequency

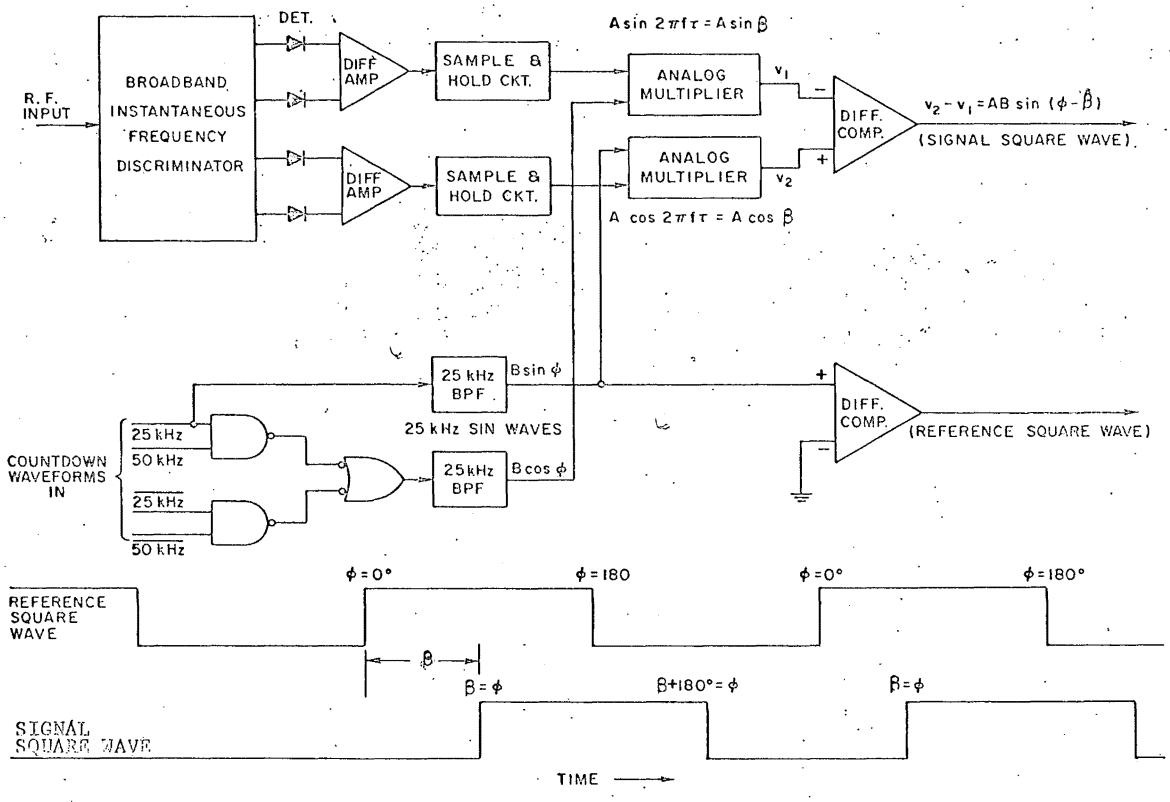


FIGURE 3-28 FREQUENCY MEASUREMENT ANALOG PROCESSOR

of 25 kHz. The multiplier outputs are differenced to provide the voltage $V_2 - V_1$ discussed above. A reference square wave is generated by squaring up the B sin Ø waveform with a comparator.

The reference square wave is available continuously, changing state each time the imaginary rotating cursor generated by B sin Ø and B cos Ø passes the 0^o and 180^o points on the polar display.

Until a signal appears and is sampled, the analog multiplier outputs are zero; when a signal is sampled, the output $V_2 - V_1$ becomes a square wave with the same period as the reference square wave, but with a phase difference determined by the frequency (angle β) of the r.f. input.

The digital processing circuit is shown in Figure 3-29. The inputs to this circuit are the signal square wave (SSW), the reference square wave (RSW) and a command input used to initiate the readout cycle.

When no signals are present, the counter starts each time $Ø = 360^o$ (0^o), is reset and starts again. The total number of counts is 3.2×10^6 counts/sec. $\times$ 40×10^{-6} sec. = 128 counts.

When a valid signal appears (as determined by the receiver measurement thresholds) it is sampled and applied to the multiplier inputs; after a short delay to allow settling of any transients at the multiplier outputs, a command to initiate the digital measurement is given to the processor; this command is synchronous with the clock waveform. At the time the process command appears, the reference square wave phase is arbitrary and the accumulated count may be anywhere between zero and 127. The counter will be stopped at the next change-of-state of the signal square wave. It is estimated that the relative phase between the SSW and the RSW can be determined with an accuracy of $\pm$ 2% (2.6τ). This corresponds to a 1σ frequency error introduced by the processor of 1.9 MHz.

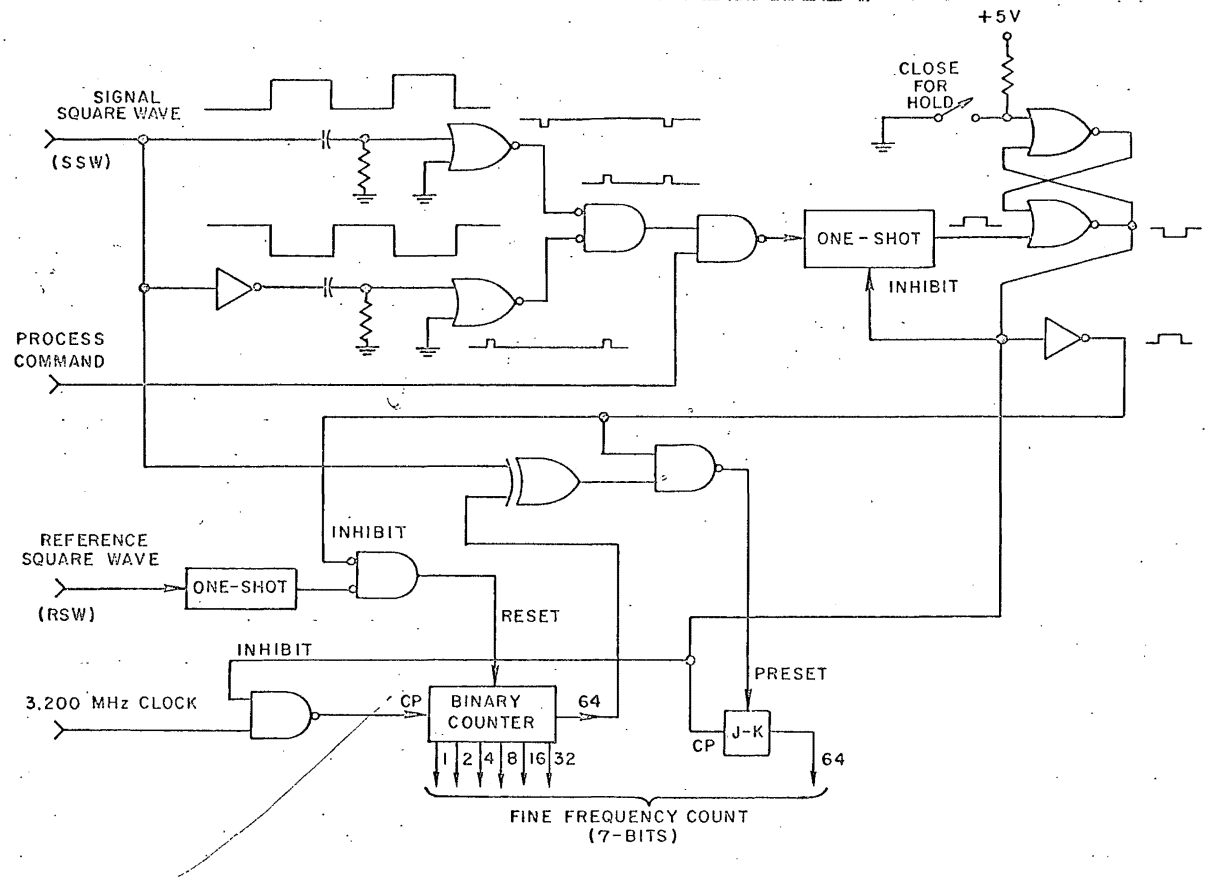


FIGURE 3-29 FREQUENCY MEASUREMENT DIGITAL PROCESSOR

If a counter were used without any other logic, the count at this time could represent either the angle from $\emptyset$ = 0 deg to the signal (counter turned off on positive transition of SSW) or the angle from $\emptyset$ = 0 deg to the signal plus 180 deg (turned off on negative SSW transition). This ambiguity is resolved by generating an "artificial" bit by comparing the counter output with the state of the SSW immediately after the transition which turned off the counter.

3.4.4 Digital Output Format

The output of the digital frequency processor will be a parallel binary word (count proportional to frequency). This word will be converted to serial format when clocked to the format generator.

In the receiver system two discriminators are to be used, one fine frequency discriminator with eight cycles over the band (i.e., 250 MHz/cycle) and one coarse discriminator with one cycle over the band. If 128 counts are used for one polar revolution of the fine discriminator, the frequency resolution will be 1.95 MHz. However, a given count out of the fine discriminator specifies any one of 8 different frequencies separated by 250 MHz; the coarse discriminator must resolve this ambiguity.

It is necessary to have more than eight resolution cells in the coarse frequency discriminator (CFD) output since perfect tracking between the discriminators will not be possible, and even if it were, there could still be a logic or quantization error of one resolution cell for frequencies near the fine frequency discriminator (FFD) crossover points. However, if the CFD output is quantized into 16 resolution cells, this problem can be avoided. The scheme for quantizing the FFD and CFD outputs is illustrated in Figure 3-30. Although the count numbers are listed in decimal form, it should be kept in mind that the actual system will operate in the binary number system; this is the reason for choosing eight revolutions of the FFD to

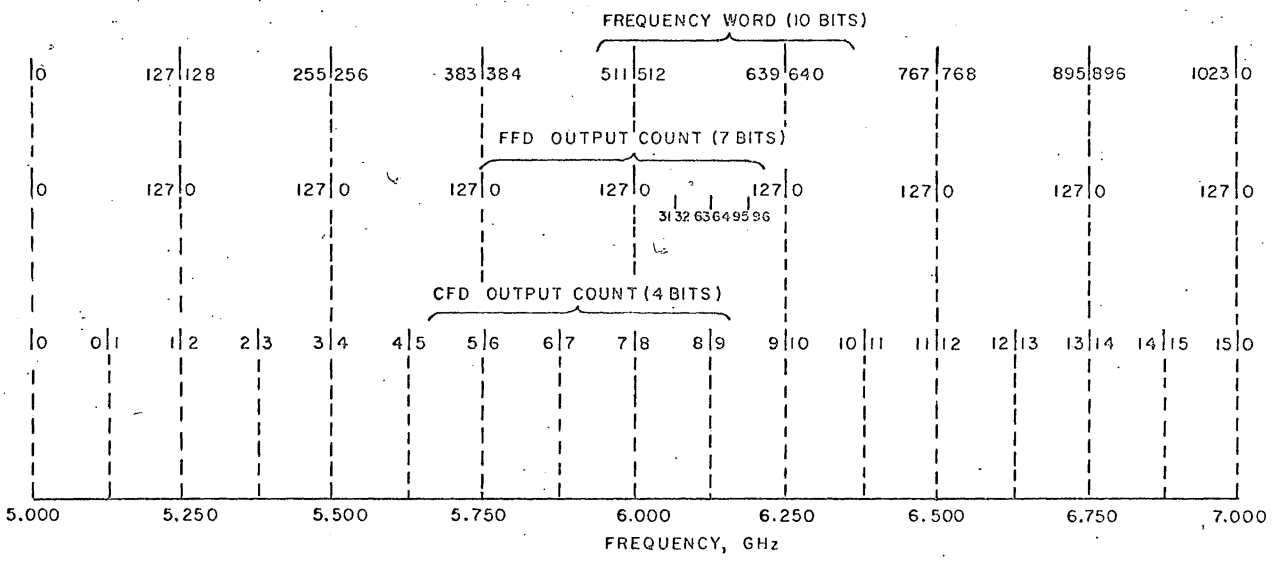


FIGURE 3-30 FREQUENCY MEASUREMENT QUANTIZATION SCHEME

BIF-476W-043-70

cover the band. By picking the proper arrangement for the counts, the hardware required to generate the frequency word can be kept simple.

From Figure 3-30 note that the FFD repeats every 250 MHz and the desired output frequency word starts at zero (0000000000) and increases to 1,023 (1111111111) as the frequency changes from 5.000 GHz to 7.000 GHz. Since the FFD output will be used as the frequency measurement criteria and the CFD only to resolve the FFD ambiguities, the 7 least significant bits of the frequency word (FW) will be identical to the FFD output count. The task then is to form the three most significant bits of the FW; this can be accomplished by using knowledge of both the CFD and FFD output.

Notice that in Figure 3-30, the FFD output in the frequency range from 6.000 MHz to 6.250 MHz has been divided into four sub-divisions (0-31, 32-63, 64-95, 95-127). Ideally, for FFD = 0-63, CFD = 8 and for FFD = 64-127, CFD = 9; this, however, will not be the case because of quantization error and discriminator non-linearities and drift.

Suppose we assume that if FFD equals 0-31, CFD = 7 or 8; for this assumption not to hold, the error in the CFD would have to be at least 62.5 MHz which is several times larger than the errors expected from the CFD. Thus, we also conclude that if FFD = 32-63, CFD = 8 or 9; if FFD - 64-95, CFD = 8 or 9; and if FFD = 96-127, CFD = 9 or 10.

If the overall frequency range is examined the relationships shown in Table 3 become evident, where the frequency sub-word (FSW) is the three most significant bits of the FW:

$$\underbrace{\overbrace{X\ X\ X}^{\text{FSW}}\ \overbrace{X\ X\ X\ X\ X\ X\ X}^{\text{FFD}}}_{\text{FW}} \quad (10\text{-bits})$$

TABLE 3

RELATION OF FSW TO FFD AND CFD OUTPUTS

FFD	CFD	FREQ SUB WORD (FSW)
(0) 0 0 0 0 0 0 0	15 or 0	0 0 0
to	1 or 2	0 0 1
Region 1	3 or 4	0 1 0
	5 or 6	0 1 1
	7 or 8	1 0 0
	9 or 10	1 0 1
(31) 0 0 1 1 1 1 1	11 or 12	1 1 0
	13 or 14	1 1 1
(32) 0 1 0 0 0 0 0	0 or 1	0 0 0
to	2 or 3	0 0 1
	4 or 5	0 1 0
Region 2	6 or 7	0 1 1
	8 or 9	1 0 0
	10 or 11	1 0 1
	12 or 13	1 1 0
	14 or 15	1 1 1
(95) 1 0 1 1 1 1 1		
(96) 1 1 0 0 0 0 0		
	1 or 2	0 0 0
	3 or 4	0 0 1
to	5 or 6	0 1 0
	7 or 8	0 1 1
	9 or 10	1 0 0
Region 3	11 or 12	1 0 1
	13 or 14	1 1 0
(127) 1 1 1 1 1 1 1	15 or 0	1 1 1

The FFD is already available; the FSW must be generated. This could be accomplished by performing logical combinations of the FFD and the CFD outputs directly. However, several steps may be taken to significantly reduce the complexity of the required logic. Note that in Table 3 the FFD output has been divided into three regions, where in each separate region the relation of the FSW to the CFD output is constant. The region may be determined by examining only the two most significant bits of the FFD output as follows:

FFD (two most sig. bits)	Region
0 0	1
0 1	2
1 0	2
1 1	3

The FSW may be generated for each of the three regions by simply generating appropriate countdown waveforms from the CFD counter output as illustrated in Figure 3-31. The top four waveforms represent the four bits of the CFD counter versus time. Examining the three most significant bits of this counter output revelas that they are identical to the FSW required in Region 2. By using some straightforward countdown logic operating from the CFD counter output, the FSW's required in Regions 1 and 3 can also be generated, as indicated in Figure 3-31. The three FSW's will, of course, all be generated simultaneously and the proper one selected to be placed into the FW on the basis of the region determination. The base logic scheme is illustrated in Figure 3-32. Examination of Figure 3-32 reveals that the output of the FFD counter is placed directly into the frequency-word to make up the 7 least significant bits. The three possible frequency subwords are available at the countdown circuit outputs CD1, CD2 and CD3. The proper FSW is selected on the basis of the region determination and is put into the 3 most significant bit positions of the now complete frequency word.

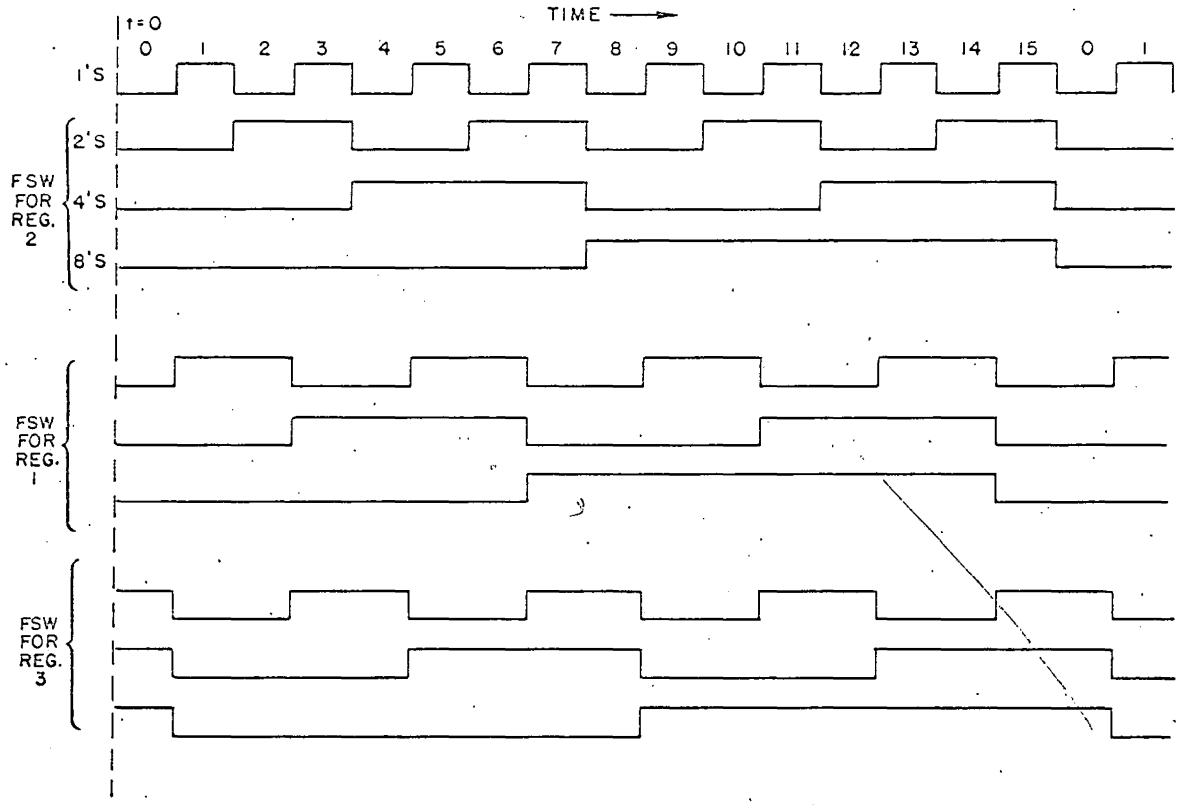


FIGURE 3-31 GENERATION OF FREQUENCY SUB-WORDS

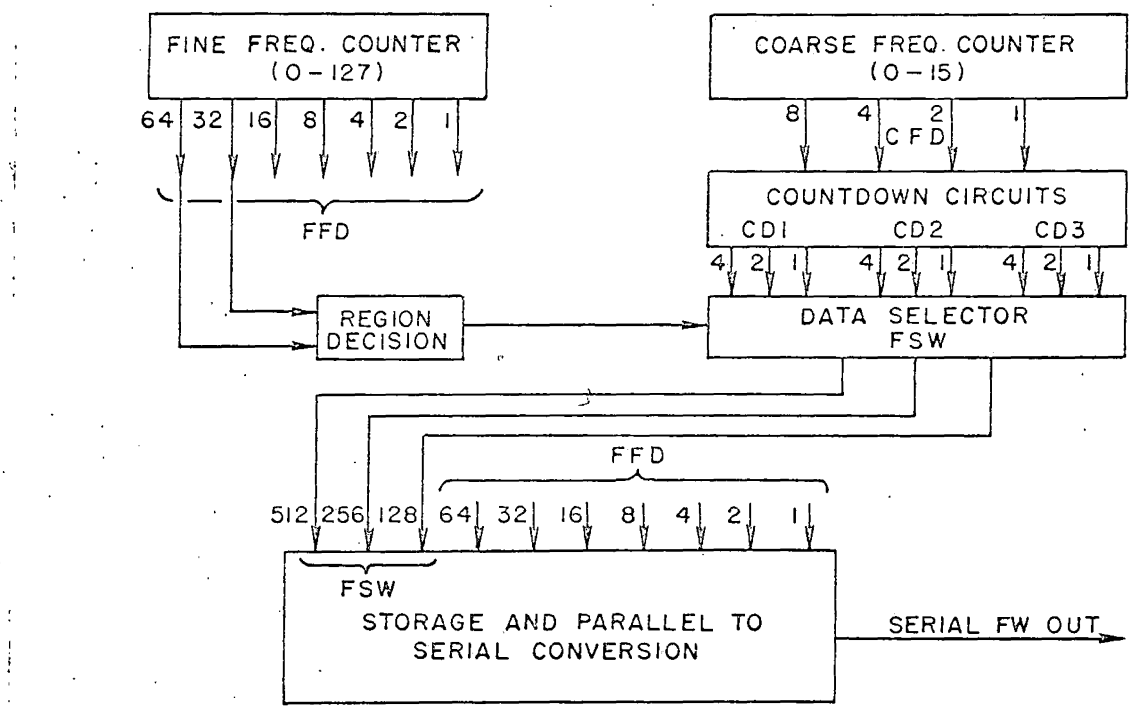


FIGURE 3-32 FSW GENERATION LOGIC BLOCK DIAGRAM

3.5 DETAILED PAYLOAD BLOCK DIAGRAM

The detailed block diagram of the payload is given in Figure 3-33 (foldout at end of report). This diagram shows all of the payload sub-assemblies and their functional interconnections. The simplified block diagram was discussed in Section 3.1 which identified the primary payload measurements. The receiver RF front end including the basic rf channel, the choice of local oscillator frequencies , the frequency measurement channel and the test signal generator were discussed in detail in Section 3.2. The DF Video Processing including a description of the techniques used to perform the DF power ratio measurement and output digital logic necessary to generate the DF word is given in Section 3.3. Last, the Frequency Measurement Video Processing technique was discussed in Section 3.4. The remaining measurements which have not been discussed in detail are the Pulse Width and TOA Measurements.

The TOA Measurement is clocked at a 1 MHz rate and is a measure of the time between the leading edge of the data pulse to the next half frame increment in the PCM output (two data pulses can be transmitted each frame, see Section 3.6.1).

The Pulse Width Measurement is a measure of the time between the crossing of a fixed threshold on the leading edge of the pulse and a fixed voltage increment below the peak of the logarithmeticly compressed pulse. It has previously been established that this combination of thresholds provides an accurate measurement of pulse width. This measurement is digitized at a 16 MHz rate and is read out with .0625 μsec resolution for pulse widths up to 5 μsec, and 0.125 μsec resolution from 5.125 to 10 μsec.

The remaining portions of the payload include the Timing Circuits, the Output Buffer Memory, the Format Generator, and other miscellaneous outputs such as the TRG, Horizon Sensor, Status, etc.

The Timing Circuits generate coherent timing waveforms from a master 16 MHz oscillator which has been synchronized to the TRG. Provision should also be provided to allow the timing circuits to be synchronized to a secondary internal reference as a backup to the TRG.

The output Buffer Memory can store up to two data bits. If data pulses occur at intervals less than 250 μsec the measured parameter will be stored in the buffer memory. Both the TOA and Pulse Width measurements are available immediately at the time of the input pulse trailing edge, however, it requires a finite time to perform the DF, Power Level, and Frequency measurements. If a second data pulse appears while either of these measurements are being processed it will be lost; however, if it appears after they are completed the first will be stored in the buffer memory and the second also measured. The average time to perform both the DF and frequency measurements is 20 μsec. The maximum possible measurement time is 30 μsec for the DF and 40 μsec for the frequency measurement.

The Output Format Generator combines the pulse data bits with other data such as TRG, Horizon Sensor, Status, etc. to generate the output PCM word that can be made compatible with the SGLS ground station equipment.

3.6 OUTPUT FORMAT

3.6.1 PCM Data

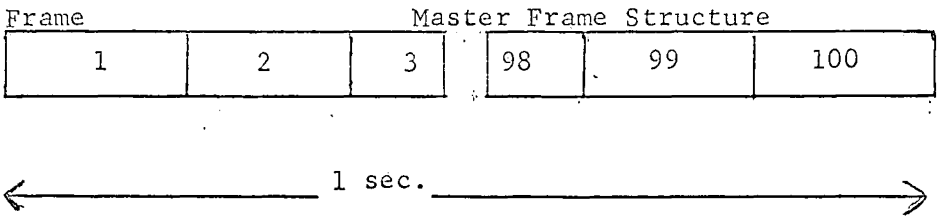
The output format of the PCM bit stream is similar to that of the URSALA payload which is compatible with the SGLS ground station equipment. A bi-phase mark PCM code recorded at 256 K bits per second and readout at 1024K bits per second is recommended. The PCM format is divided into a MASTER FRAME, FRAME, LINE and WORD structure as shown in Figure 3-34. The data parameters, their range, their resolution, and number of bits needed to transmit are shown in Table 4. Eight words are needed to transmit the measured parameters of a single data pulse, hence, two data pulses are transmitted on each line. Lines two through 20, in the frame structure,are identical and each contain two data pulses The first 8 words on Line 1 in the frame are used to transmit a 32 bit Barker code frame sync every 10 ms plus other sub-commutated data. With 8 words available for each frame this results in a total of 3200 bits available for the sub-commutated data also listed in Table 4.

3.6.2 Other Data Channels

In addition to the PCM data, other analog data channels are frequency multiplexed on to the data link. These include 1) the Omni Video data on a Ch E VCO, 2) the GSQ-53 time word TRG on a Ch 16 VCO, 3) either the Sun Sensor or Horizon Sensor command selectable on Ch 15 VCO, and 4) a 50 KHz reference tone.

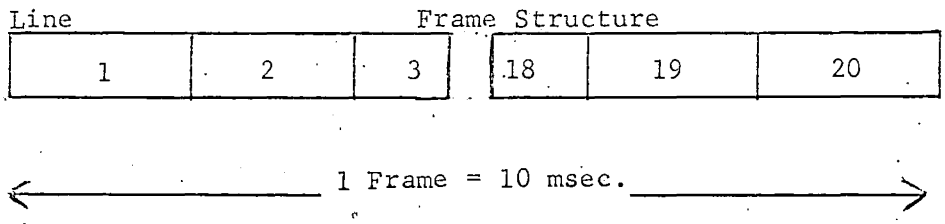
The analog data are to be transmitted on a 1.7 MHz sub-carrier channel with the PCM data in the base band of the single 2 MHz bandwidth down link. Since the flight recorder has only 1 MHz bandwidth, it is necessary to record these data on two tracks and then frequency multiplex the two tracks on playback (see Figure 3-35). The spectrum of the record and down link data channels are shown in Figure 3-36. There is room for one additional 5 KHz data channel in the baseband of the 1.7 MHz FM channel. This could be used for reading out an additional measurement such as a cw detection if desired.

SGLS



256 KBPS

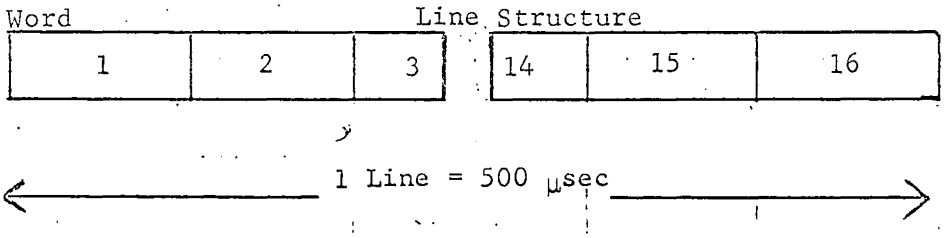
100 Frames per second



20 Lines per Frame

2560 bits per Frame

256 bits per msec.



16 Words per Line

128 Bits per Line

8 Bits per Word

PCM FORMAT

FIGURE 3-34

PCM DATA PARAMETERS

PARAMETER	RANGE	RESOLUTION	# BITS
TOA	0-250 μsec	1 μsec	8
PW	0.0625-5 μsec 5.125-10 μsec	0.0625 μsec 0.125 μsec	7
FREQ	0 - 2 GHZ	2 MHz	10
HIGH Channel Power Level	0 - 38.4 dB	0.3 dB	7
2nd Channel Rel Power Level	0 - 9.6 dB	0.3 dB	5
3rd Channel Rel Power Level	0 - 9.6 dB	0.3 dB	5
Channel Power Level Order	3 of 216		9
Buffer Pulse Count	0 - 2 plus overflow		2
H/S Pulse	Yes/No		1
S/S Pulse	Yes/No		1
CAL	Yes/No		1
SPARE			8
Total Bits per 1/2 Line (8 words)			64

OTHER PCM DATA

Frame Sync 26 bits every 10 ms

Sub Commulated Data

a. Time Word: 23 hours, 59 min., 59 sec. 20 bits every second

b. Sun Sensor Angle: ± 32° with 0.5° resolution, 7 bits every 200 msec

c. Command Matrix: as required once per second

d. Payload Status: as required once per second

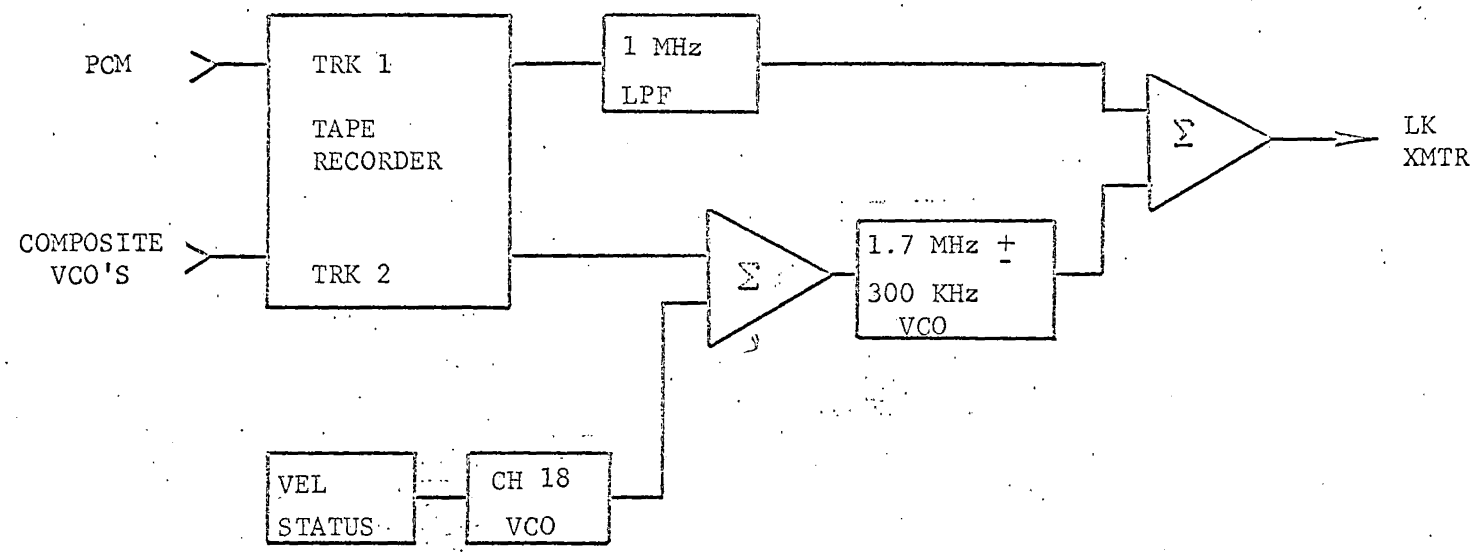


FIGURE 3-35 TAPE RECORDER READOUT (R/O)

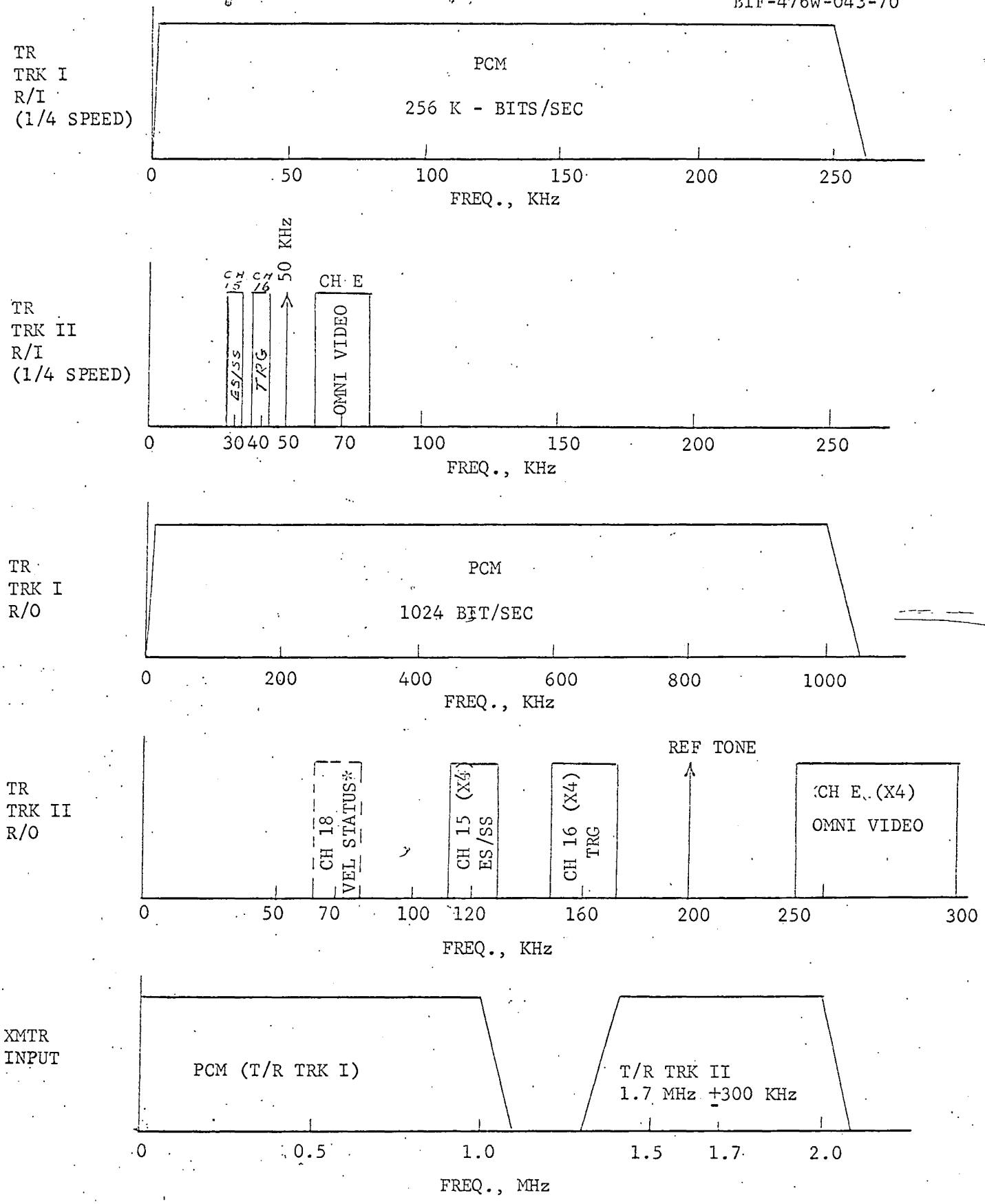


FIGURE 3-36 R/I, R/O AND DOWN LINK FREQUENCY SPECTRUM

*Vel Status summed with recorded data at 1.7 MHz VCO input

It should be noted that a 1/4 speed, 250 KHz R/I bandwidth is suggested. This is to allow for 24 min read-in time intervals. With a Main Beam Collection System it is desirable to turn-on and turn-off below the horizon both approaching and leaving the desired area of coverage. This necessitates that the payload be turned on from below the equator to past the North Pole.

4.0 ANTENNAS

The antennas best suited for this wide-aperture amplitude-monopulse DF application are broadband flat spirals; the general characteristics of these antennas are discussed in Section 2.0 above and a typical idealized pattern is presented in Figure 2-2 of that section.

Measured patterns on an antenna of this type are available along with summarized data on axial ratios, boresight shift and 3 dB beamwidth measured every 100 MHz from 2.0 GHz to 12.0 GHz.

These patterns were of the antenna only and did not include the effects of the vehicle. The vehicle can be expected to have some influence upon the patterns, however this should be minimized and patterns should be taken with the antennas mounted on a vehicle.

From the patterns, typical monopulse error curves were generated for a cut in the plane of two boresights; in this plot, identical patterns for the two antennas were assumed (see Figure 4-1).

The slope of the error curve is considerably less at f = 2.0 GHz because of the broadening of the antennas beamwidth at the extreme low end of the band; however, above 4.0 GHz, the slope becomes reasonably constant and actually oscillates since the beamwidth possess ripples which are a function of frequency. A plot of 3 dB beamwidth vs frequency for a constant linear polarization is presented in Figure 4-2, and Figure 4-3 shows the gain relative to boresight at 32 degrees and 64 degrees.

The error curves of Figure 4-1 all pass through the origin because identical patterns were assumed for the two antennas; in practice, the curves will not always intersect the origin because of pattern variations between the antennas. The antenna beamwidth (or gain off boresight) will vary as a function of azimuth (at constant frequency) in approximately the same manner as it varies with frequency at constant azimuth.

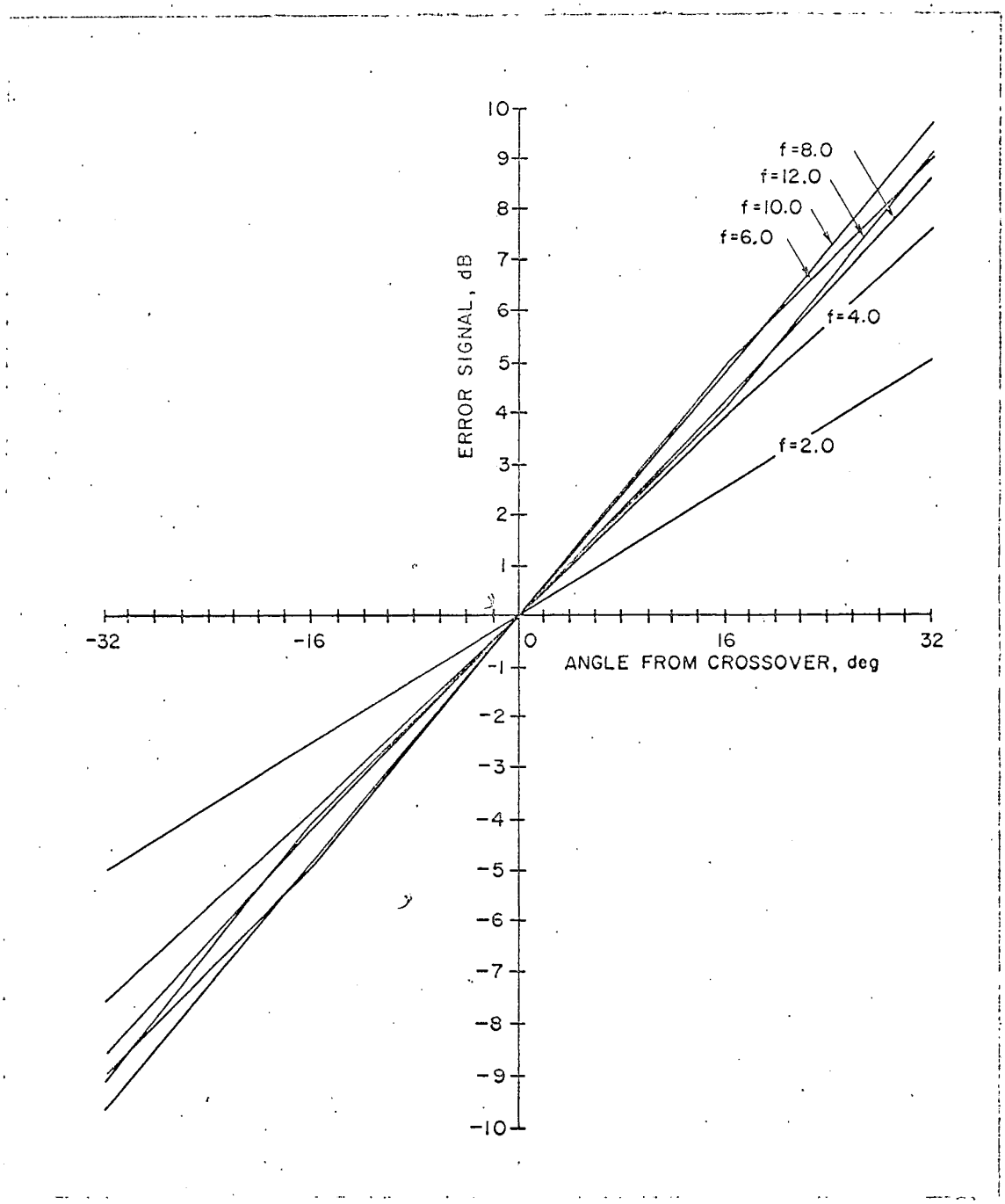


FIGURE 4-1 TYPICAL MONOPULSE DF ERROR CURVES

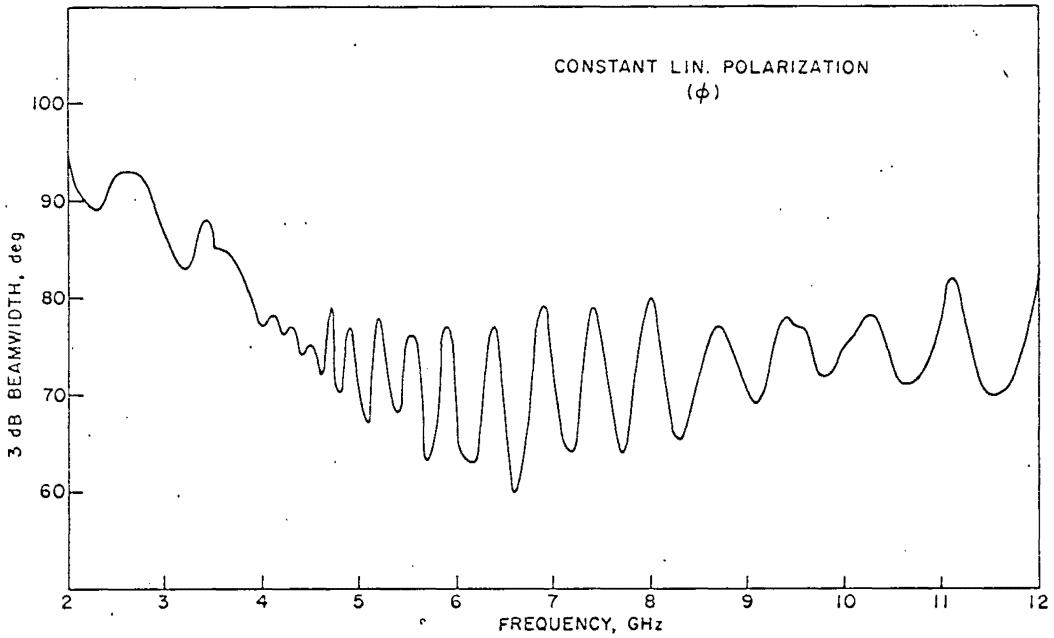


FIGURE 4-2 VARIATION OF ANTENNA BEAMWIDTH WITH FREQUENCY

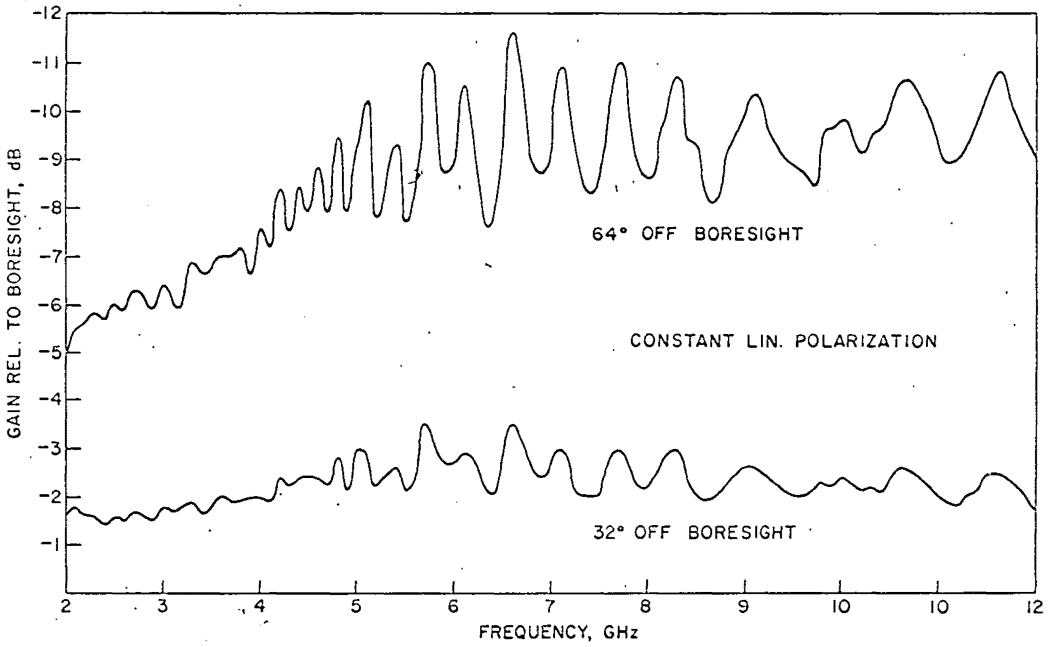


FIGURE 4-3 VARIATION OF OFF-BORESIGHT GAIN WITH FREQUENCY

The expected error in the DF measurement can be estimated from Figure 4-3; for example, in the 6.0 to 8.0 GHz band, the average error curve can be drawn and is shown in Figure 4-4. This error curve was plotted assuming antenna patterns corresponding to the average values of the oscillating gain functions shown in Figure 4-3. From the peak-to-peak amplitude of the gain variations indicated in Figure 4-3, the rms angular error due to pattern variations may be estimated and is indicated as a band on either side of the average error curve shown in Figure 4-4. This error band has a minimum width at the pattern crossover and increases toward the antenna boresight. Figure 4-4 indicates that the rms error 32 degrees from crossover is 3 degrees and the error decreases to about 2.3 degrees at crossover.

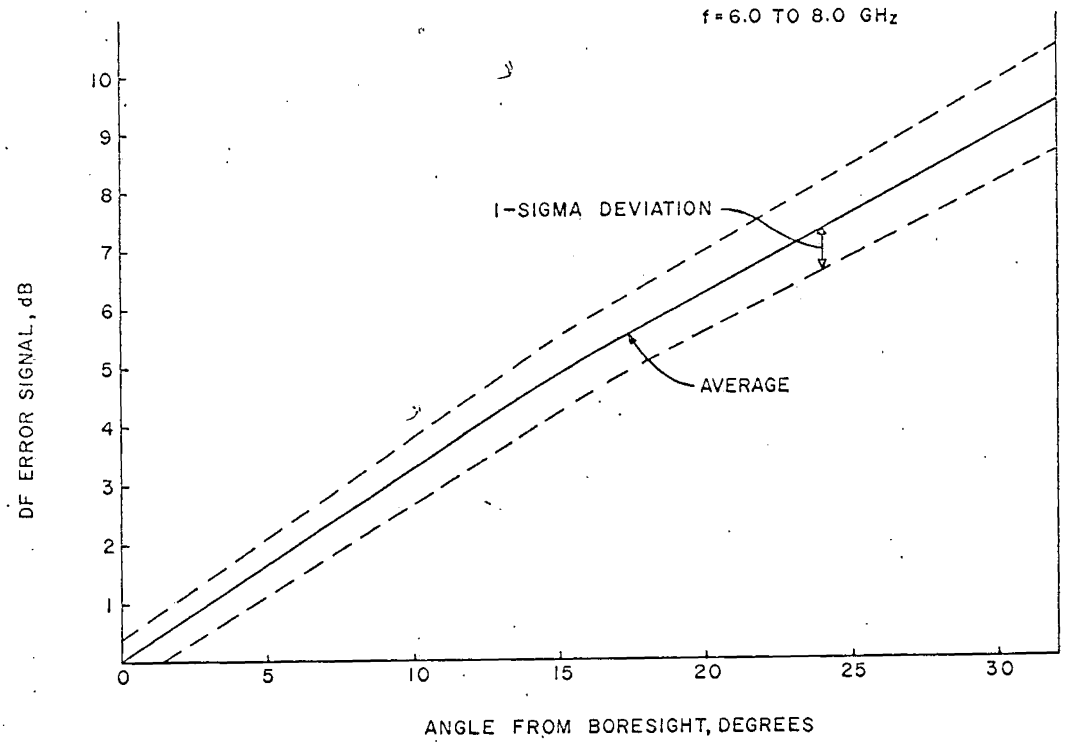


FIGURE 4-4 ANTENNA DF ERROR SIGNAL VS ANGLE OFF BORESIGHT

Polarization mismatch will also contribute to the DF error; the expected value of the axial ratio is about 0.5 dB at crossover and 0.7 dB at 32 degrees from crossover. These numbers correspond to angular errors of 2 degrees and 2.8 degrees respectively. Adding these errors (as rms values) the total 1 σ error is estimated as 3.1 degrees at crossover and 4.0 degrees 32 degrees from crossover.

The variations in beamwidth (Figure 4-3) indicate that somewhat improved accuracy might be obtained in the 2-5 GHz region and possibly in the 8-12 region; however, the axial ratio will be somewhat greater at the band edges and will tend to offset any improvement in beamwidth matching.

5.0 PHYSICAL DESCRIPTION

The payload described would require the majority of the space, weight and power capability of both wings of a P-11 vehicle. Estimates were made on both weight and power consumption and are given below in Tables 5 and 6. These estimates were based on conventional packaging techniques. For example, as estimated, the microwave components are all individually packaged and then assembled as a sub-assembly and the video and digital circuits were estimated using conventional printed circuit board construction techniques. Significant weight could be saved by initially packaging the microwave components as integrated sub-assemblies and using thick film circuit fabrication techniques. This is particularly appropriate for the repeated video and digital circuits.

The overall weight of both boxes was estimated as 74 lbs, 9 oz. and is summarized in detail in Table 5. It was originally anticipated that it would be possible to later include either or both a CW measurement capability and a polarization measurement in the system. This is not out of the question even with this high estimated weight because of 1) the possibility of weight savings over that estimated, 2) the antennas used in this system are quite small and simple thereby saving more weight for the payloads and, 3) in the case of the polarization measurement, it may be possible to time share rf channels with the DF measurement. For example, the DF aperature could be reduced while operating in the polarization measurement mode of operation.

The power requirements were estimated to be 87 watts (3.4 amperes at 26V) and are summarized in Table 6.

TABLE 5

PAYLOAD WEIGHT ESTIMATES

	Weight, Oz
1. RF Component Weight Estimates (using comercially available miniature coax packages)	
a. Typical RF Channel	
1. Input Triplexer	6
2. 2 each, Band Pass Filters (3 oz. ea.)	6
3. 4-8 GHz TDA	16
4. 8-12 GHz TDA	16
5. 2 each Mixers (1 oz. ea.)	2
6. Transistor IF Amplifier	9
7. Microwave Switch	4
8. Detector	0.5
9. 2 each Attenuators (1/4 oz. ea.)	0.5
10. Signal Sampler	1
11. 14 each, rf Cables (1/2 oz. ea.)	7
Total	68.0 Oz
	(4 lbs. - 4 Oz.)
b. Frequency Measurement Channel	
1. TDA Limiter	32
2. 6 dB Directional Coupler	2
3. 3 dB Directional Coupler	2
4. 10 dB Directional Coupler	2
5. Mixer	1
6. Band Pass Filter	3
7. 2 each, Discriminators (include detectors) (8 oz. ea.)	16
8. 2 each, rf Oscillators (3 oz. ea.)	6
9. Microwave Switch	3
10. 10 each, rf Cables (1/2 oz. ea.)	5
Total	72 Oz
	(4 lbs. - 8 Oz.)
c. Local Oscillators	
1. 4 each Gunn Oscillators (3 oz. ea.)	12
2. 2 each, 2-way Power Divider (0.5 oz. ea.)	1
3. 2 each, 4-way Power Divider (1 oz. ea.)	2
4. Microwave Switch	3
5. 12 each, rf Cables, (0.5 oz. ea.)	6
Total	24 Oz.
	(1 lb. - 8 Oz.)

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TABLE 5 (continued)

	Weight, Oz
d. Test Signal Generator	
1. 2 each, rf Oscillators (3 oz. ea.)	6
2. 3 dB Coupler	1.5
3. Multiplexer	4
4. 12 GHz Low Pass Filter	2
5. 2-Way Power Divider	0.5
6. 4-Way Power Divider	1
7. Microwave Switch	3
8. 12 each, rf Cables (0.5 oz. ea.)	6
Total	24 Oz (1 lb. - 8 Oz.)
e. Summary of rf Section Wt. Estimate	
1. 7 RF Channels (68 oz. ea.)	476
2. Local Oscillators	24
3. Test Signal Generator	24
4. Frequency Measurement Channel	72
5. Miscellaneous Mounting Hardware	32
Total	628 Oz.
TOTAL MICROWAVE SECTION	39 lbs. - 4 Oz.
2. Video Circuits Weight Estimate (Using conventional PC card construction)	
a. DF Processing Circuits	80
b. Frequency Measurement Processing Circuits	40
c. Timing Count Down Circuits	10
d. Omni Video Circuits	11
e. Pulse Width and TOA Measurement Circuits	16
f. Buffer Memory and Output Format Generator	12
g. TSG Modulator	6
h. Video Mounting Hardware	32
TOTAL VIDEO CIRCUITS	207 Oz. (12 lbs. - 15 Oz.)
3. Overall Weight Estimates	
a. Microwave Components & Mounting Hardware and RF Cables	41 lbs. - 4 Oz.
b. Video Circuits and Mounting Hardware	12 lbs. - 15 Oz.
c. 2 each, Boxes (120 oz. per box)	15 lbs. - 0 Oz.
d. Wire	1 lb. - 0 Oz.
e. TRG	0 lb. - 12 Oz.
f. Power Supplies	3 lbs. - 0 Oz.
g. 3 each VCO's	6 Oz.
h. Command Relays	8 Oz.
TOTAL [illegible]	72 lbs. - 41 Oz.
TOTAL PAYLOAD	74 lbs. - 9 Oz.

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TABLE 6
ESTIMATED POWER REQUIREMENTS

	LOAD CURRENTS, ma				
	+5V	+10V	+15V	-15V	+26V Unreg.
1. Microwave Components					
a. RF Channels 40 ma @ 10V ea./80 ma @ 15V ea.		280	560		
b. Gun Oscillator		450			
c. UP Converters			100		
d. Pulse Modulator			10		
e. TDA Limiter		40			
Sub-Totals, Microwave Components	0	770	670	0	0
2. Video and Digital Circuits					
a. DF Video Processing	880		650	520	
b. Frequency Video Processing	170		160	180	
c. Timing Countdown Circuits	150				
e. TOA & PW Measuring Circuits	200				
f. Omni Video Channel			45	550	
g. Buffer Memory & Output Format Generator	40		80	80	
h. VCO's					30
i. TRG, ES, SS Processor	90		40		
Sub-Totals, Video & Digital Circuits	530		975	1370	30

3. Total Power

Regulator Voltage	Current ma	Power Watts
+5V	1530	7.65
+10V	770	7.7
+15V	1645	24.6
-15V	1370	20.7
+26 Unreg.	(30)	(0.78)
Total Regulated Power		60.65 watts

Assume 70% efficiency of converter/regulator

TOTAL PRIMARY POWER = (1.43 x 60.6 + .8) = 87.8 watts (3.4A. at 26V)

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6.0 SYSTEM SENSITIVITY AND ACCURACY SUMMARY

The receiver sensitivity and parameter measurement accuracy was investigated in Section 3. The antenna characteristics were reviewed in Section 4. The overall system, receiver plus antenna, sensitivity and parameter measurement accuracy will be summarized in this section.

6.1 RECEIVING SYSTEM MEASUREMENT SENSITIVITY SUMMARY

The overall system sensitivity is summarized in Table 7. The results are given for spot frequencies at the edges and center of the three bands, S, C and X. There are two calculations given at both 4 and 8 GHz, one for each of the adjacent sub-band rf channels.

The first six items summarize the antenna gain characteristics. Since any given antenna will be used over a 128° aperature, the gain is summarized both on boresight and 64° off boresight. The antenna cable was assumed to be 1/4" semi-rigid coax with a foam dialectric for minimum loss.

The sensitivity at the receiver input for a DF measurement, a frequency measurement and for 50% probability of detection is summarized in Item 7. The figures shown for S-band are not the maximum attainable, but rather that necessary for the measurements based on expected emitter power, data rates, and receiving antenna gain (loss in this case). The figures shown for C and X bands are the maximum attainable based on the noise figures specified for these two bands. The figures shown in Item 7 for the DF measurement do not include the necessary DF measurement dynamic range but rather indicates the minimum power level of the lowest of the three channels used for a given DF measurement.

Preceeding the receiver with the antenna characteristics, the various measurement sensitivities referred to the receiving antenna input are given in Item 8. Since a single threshold set on the summed video from all 6 DF channels is used in the video processing circuits to establish if there is adequate S/N to perform a DF measurement, the DF measurement sensitivity will be constant over the entire aperature. This threshold is set based on the minimum acceptable S/N ratio when

TABLE 7

SYSTEM SENSITIVITY SUMMARY

		S-BAND			C-BAND			X-BAND		
Frequency	GHz	2	3	4	4	6	8	8	10	12
1. Antenna Gain (boresight)	dB	-3	-1	+3	+3	+3	+4	+4	+4	+4
2. Antenna Gain (64% off boresight)	dB	-8	-5	-5	-5	-5	-5	-5	-5	-5
3. Antenna Cable Loss (5' FXA 14-40)	dB	-0.5	-0.6	-0.8	-0.8	-1	-1.1	-1.1	-1.3	-1.5
4. Polarization Loss	dB	-3	-3	-3	-3	-3	-3	-3	-3	-3
5. Net Antenna Gain (boresight)	dB	-6.5	-4.6	-0.8	-0.8	0	-0.1	-0.1	-0.3	-0.5
6. Net Ant. Gain (64% off boresight)	dB	-11.5	-8.6	-8.8	-8.8	-9	-9.1	-9.1	-9.3	-9.5
7. Minimum Receiver Input Power for:										
a. DF Measurement	dBM	-63*	-63*	-63*	-72.3	-72.3	-72.3	-74.4	-74.4	-74.4
b. Freq. Measurement	dBm	-63*	-63*	-63*	-70	-70	-70	-72	-72	-72
c. 50% Detection	dBm	-63*	-63*	-63*	-70.9	-70.9	-70.9	-73	-73	-73
8. Minimum Receiver Power at Antenna Input for:										
a. DF Measurement (128^{o} cone of coverage)	dBm	-51.5	-54.5	-54.5	-63.5	-63.3	-63.2	-65.3	-65.1	-64.9
b. Freq. Measurement (on boresight)	dBm	-51.5	-54.5	-54.5	-69.2	-70	-69.9	-71.9	-71.7	-71.5
c. Freq. Measurement (64^{o} off boresight)	dBm	-51.5	-54.5	-54.2	-61.2	-61	-60.9	-62.9	-62.7	-62.5
d. 50% detection (360^{o} coverage)	dBm	-51.5	-54.4	-54.2	-70.1	-70.9	-70.8	-72.9	-72.7	-72.5
9. FSA 1200 nmi (4^{o} elevation)	dB	166	169.5	172	172	175.5	178	178	180	181.5
10. Minimum Power at Xmtr. Antenna output for:										
a. DF Measurement	dBm	114.5	115.0	117.8	108.5	112.2	114.8	112.7	114.9	116.6
b. Freq. Measurement (on boresight)	dBm	114.5	115.0	117.8	102.8	105.5	108.1	110.7	108.3	110.0
c. Freq. Measurement (64^{o} off boresight)	dBm	114.5	115.0	117.8	110.8	114.5	117.1	107.1	117.3	119.0
d. 50% Detection	dBm	114.5	115.0	117.8	101.9	104.6	107.2	105.1	105.3	109.0
11. Assumed Xmtr. Antenna gain at 3 dB point	dB	30	30	30	30	30	30	33	33	33
12. Xmtr. Power for:										
a. DF Measurement over 128^{o} cone of coverage	dBm	84.5	85	87.8	78.5	82.0	84.8	79.7	81.9	83.6
	KW	280	315	600	70	160	300	100	150	230
b. 50% Detection over 360^{o} coverage	dBm	84.5	85	87.8	71.9	74.6	77.2	75.1	75.3	79.0
	KW	280	315	600	16	30	55	33	35	80

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the signal is being received on boresight of one antenna, and 64° off boresight on one or more of the adjacent antennas (9 dB measurement dynamic range). By setting individual thresholds on each channel, and introducing additional logic, the sensitivity could be improved slightly over parts of the aperature. For instance, the best sensitivity for a DF measurement would occur where two patterns cross over. This is approximately 3 to 4 dB below the boresight antenna gain rather than 9 dB below as in the case either on boresight or on the periphery of the 128° aperature. The frequency measurement sensitivity, both on boresight and 64° off boresight, is given in Items 8b and 8c. Since the frequency measurement is made from the center antenna in the cluster, the sensitivity of this measurement will be maximum at the aperature boresight and minimum on edge of the aperature.

The 50% detection sensitivity is given in Item 8d. These figures assume a 0 dB antenna gain over the 360° spherical coverage. In calculating the 50% detection sensitivity (Section 3.2.1.4.1), the noise contribution from all 7 receiver channels was included. It can be shown that the sum of the detected signal voltages will provide a gain slightly greater than 0 dB, however 0 dB was used in this study. The free space attenuation (FSA) for a 1200 nmi slant range is given in Item 9. This corresponds to an intercept 4° in from the visual horizon. Using Items 8 and 9, the minimum power at the transmitter antenna output for the DF, frequency and 50% detection measurement is shown in Item 10. A transmitter antenna gain was assumed in Item 11 and used with Item 10 to estimate the minimum transmitter power required for the DF and 50% detection measurements.

6.2 SYSTEM DF MEASUREMENT ACCURACY

The overall DF measurement errors are due to 1) antenna errors, 2) RF channel gain mismatch, and 3) video processing circuit errors including those due to thermal noise. Each of these errors were developed in previous sections and are summarized in Table 8. The antenna error slope from Figure 4-1 (Item 5) is also given and used to reflect the

channel gain variations into angular variations (Item 6). The total 1σ DF measurement error of the entire system, antenna and receiver, is given in Item 7. The 0.3 dB quantization increment is also converted to angular quantization uncertainty in Item 8 for comparison purposes.

6.3 FREQUENCY MEASUREMENT ERRORS

The frequency measurement errors are summarized in Table 9. The overall 1σ error is 2.6 MHz for a very large signal-to-noise ratio and 4 MHz for an intercept just above the measurement threshold which is -70 dBm in C-band and -72 dBm in X-band referred to the receiver front end (see Section 3.2.2.5). The quantization increment for this measurement is 2 MHz per bit.

TABLE 8

SYSTEM DF MEASUREMENT ERROR STUDY

		1σ error
1.	Antenna Errors	
	a. Antenna crossover	3.1°
	b. 32° from crossover	4.0°
2.	RF Channel Match	
	a. S-band	0.29 dB
	b. C and X-bands	0.38 dB
3.	Video Processing Circuits	
	a. Ratio measurement, large S/N	0.14 dB
	b. Ratio error due to thermal noise, S/N = 14 dB	0.82 dB
4.	Combined RMS Error of RF + Video Channel	
	a. S-Band	
	Large S/N	0.32 dB
	S/N = 14 dB	0.87 dB
	b. C and X-bands	
	Large S/N	0.40 dB
	S/N = 14 dB	0.90 dB
5.	Antenna Error Slope	
	a. 2 GHz	6.4°/dB
	b. 4-12 GHz	4.2°/dB

6. Angle of Arrival Error due to Receiver Errors

	Large S/N	S/N = 14 dB
a. 2 GHz	2.0°	5.6°
b 4 GHz	1.3°	3.6°
c. 4-12 GHz	1.7°	3.8°

7. Total DF Measurement 1σ Errors (Antenna + Receiver)

	2 GHz	4 GHz	4-12 GHz
Antenna Crossover			
Large S/N	3.7°	3.4°	3.5°
14 dB S/N	6.4°	4.7°	4.9°
32° from Crossover			
Large S/N	4.5°	4.2°	4.3°
14 dB S/N	6.9°	5.4°	4.5°
0.3 dB Quantization Increment	1.9°	1.2°	1.1°

TABLE 9

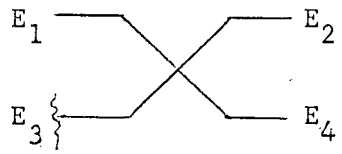
Frequency Measurement Error Summary		1σ
1. Frequency Discriminator Errors		1.6 MHz
2. Video Processing Circuits		1.9 MHz
3. Thermal Noise Errors		3 MHz
4. Overall RMS Frequency Measurement Errors	Large S/N	At Measurement Threshold
	2.5 MHz	3.9 Mhz
5. Quantization Increment	2 MHz	2 Mhz

APPENDIX A

DEVELOPMENT OF THE FOUR QUADRANT FREQUENCY DISCRIMINATOR TRANSFER CHARACTERISTIC

1. Quarter Wave Coupler Equations

Consider the quarter wave coupler below



For

$$E_1 = E \sin \omega t \tag{A.1}$$

then

$$E_2 = \frac{E_1 \, jK \sin \theta}{(1-K^2)^{\frac{1}{2}} \cos \theta + j \sin \theta} \tag{A.2}$$

$$E_3 = 0$$

$$E_4 = \frac{(1-K^2)^{\frac{1}{2}}}{(1-K^2)^{\frac{1}{2}} \cos \theta + j \sin \theta} \tag{A.3}$$

where

$$\theta = \frac{\Pi \omega}{2\omega_c} \tag{A.4}$$

ω_c = the quarter wave coupler center frequency

and =

K = the voltage coupling coefficient.

E_2 and E_4 can be expressed as

$$E_2 = E_1 \frac{K \sin\theta}{(1-K^2\cos^2\theta)^{\frac{1}{2}}} \angle \tan^{-1}(1-K^2)^{\frac{1}{2}} \operatorname{ctn}\theta \qquad (A.5)$$

$$E_4 = E_1 \left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}} \angle \tan^{-1}(1-K^2)^{\frac{1}{2}} \tan\theta \,. \qquad (A.6)$$

The angle of E_2 and E_4 remain 90° with respect to each other for all θ, hence, E_2 and E_4 can be simplified to

$$E_2 = E_1 \frac{K \sin\theta}{(1-K^2\cos^2\theta)^{\frac{1}{2}}} \angle 0^\circ \qquad (A.7)$$

$$E_4 = E_1 \left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}} \angle \pi/2 \,. \qquad (A.8)$$

2. Discriminator Equations

The discriminator shown in Figure 3-9 contains seven of these quarter wave couplers, a delay τ, and four matched detectors. The expressions for the four detected output voltages as a function of frequency will be developed below.

Assume that the input voltage, e(t), is

$$e(t) = E \sin \omega t.$$

Since the operation of the discriminator involves dividing and recombining of voltage vectors at various phase angles but all at the same radian frequency, it is convenient to express the input voltage

as a vector and use it as a reference throughout the development. Therefore let $E_{in} = E \angle 0^\circ$ and referring to Figure 3-9 and the expressions for the quarter wave coupler, equations A.7 and A.8, the voltages E_1 through E_4 in Figure 3-9 become

$$E_1 = E \frac{K^2 \sin^2\theta}{(1-K^2\cos^2\theta)} \angle 0^\circ \tag{A.9}$$

$$E_2 = E \frac{CK(1-K^2)^{\frac{1}{2}} \sin\theta}{(1-K^2\cos^2\theta)} \angle -(\Pi/2 + \omega\tau) \tag{A.10}$$

$$E_3 = E \frac{K^2(1-K^2)^{\frac{1}{2}} \sin\theta}{(1-K^2\cos^2\theta)^{3/2}} \angle -\Pi/2 \tag{A.11}$$

$$E_4 = E \frac{C(1-K^2)}{(1-K^2\cos^2\theta)} \angle -(\Pi + \omega\tau) . \tag{A.12}$$

Combining E_1 and E_2 in the output coupler, the expression for the output voltage, E_{01} is

$$E_{01} = E \frac{K^3(1-K^2)^{\frac{1}{2}} \sin^3\theta}{(1-K^2\cos^2\theta)^2} \angle -\Pi/2 + \frac{CK(1-K^2)\sin\theta}{(1-K^2\cos^2\theta)^{3/2}} \angle -(\Pi + \omega\tau) \tag{A.13}$$

$$E_{01} = E \cdot A \angle -\Pi/2 + B \angle -(\Pi + \omega\tau) \tag{A.14}$$

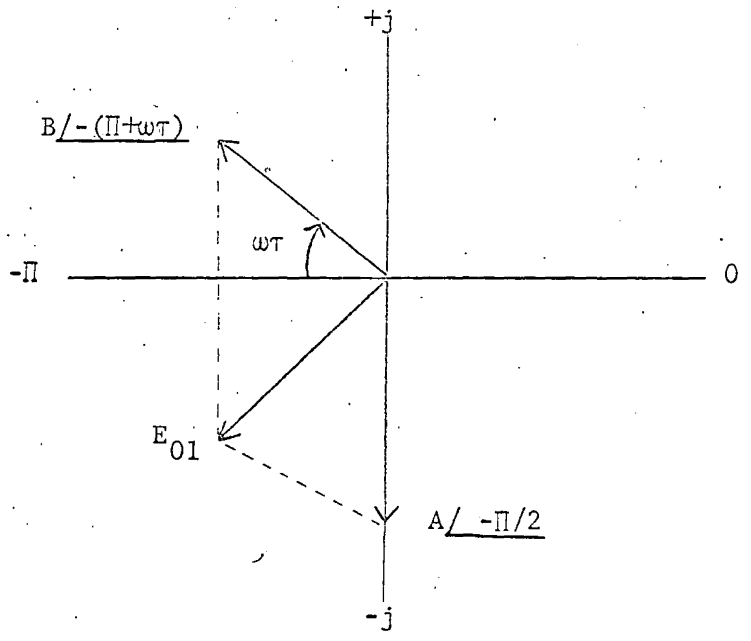
where

$$A = \frac{K^3(1-K^2)^{\frac{1}{2}} \sin^3 \theta}{(1-K^2\cos^2 \theta)^2} \qquad A.15$$

and

$$B = \frac{CK(1-K^2) \sin \theta}{(1-K^2\cos^2 \theta)^{3/2}} . \qquad A.16$$

To determine the magnitude of E_{01}, consider the following sketch:



$$R_e E_{01} = -B \cos \omega\tau$$

$$I_m E_{01} = -j (A - B \sin \omega\tau)$$

and

$$|E_{01}| = \left[B^2\cos^2 \omega\tau + (A - B \sin \omega\tau)^2 \right]^{\frac{1}{2}}$$

$$|E_{01}| = \left[A^2 + B^2 - 2 AB \sin \omega\tau \right]^{\frac{1}{2}}. \qquad (A.17)$$

Substituting equations (A.15) and (A.16) into equation (A.17)

$\left|E_{01}\right|$ becomes

$$\left|E_{01}\right| = E\,\frac{K(1-K^2)^{\frac{1}{2}}\sin^2\theta}{(1-K^2\cos^2\theta)^{3/2}}\left[\frac{C^2(1-K^2)}{\sin^2\theta} + \frac{K^4\sin^2\theta}{(1-K^2\cos^2\theta)} - 2CK^2\left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}}\sin\,\omega\tau\right]^{\frac{1}{2}} \quad \text{(A.18)}$$

Assuming a square law detector with open circuit voltage coefficient A_1, the detected output voltage is

$$E_{01_D} = A_1 P_{01} \quad \text{(A.19)}$$

where P_{01} is the power incident on the detector.

Relative to the discriminator input power, P_{in}, E_{01_D} is

$$E_{01_D} = A_1 P_{in}\,\frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{\sin^2\theta} + \frac{K^4\sin^2\theta}{1-K^2\cos^2\theta} - 2CK^2\left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}}\sin\,\omega\tau\right] \quad \text{(A.20)}$$

and similarly the expressions for E_{02_D} through E_{04_D} are

$$E_{02_D} = A_2 P_{in}\,\frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[C^2K^2 + \frac{K^2(1-K^2)}{1-K^2\cos^2\theta} + 2CK^2\left(\frac{1-K^2}{1-K^2\cos^2\theta}\right)^{\frac{1}{2}}\sin\,\omega\tau\right] \quad \text{(A.21)}$$

$$E_{03_D} = A_3 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{K^2\sin^4\theta} + \frac{K^4\sin^2\theta}{(1-K^2\cos^2\theta)} - \frac{2CK(1-K^2)}{\sin\theta(1-K^2\cos^2\theta)^{\frac{1}{2}}}\cos\omega\tau\right]$$

(A.22)

$$E_{04_D} = A_4 P_{in} \frac{K^2(1-K^2)\sin^4\theta}{(1-K^2\cos^2\theta)^3}\left[\frac{C^2(1-K^2)}{\sin^2\theta} + \frac{K^2(1-K^2)}{(1-K^2\cos^2\theta)} + \frac{2KC(1-K^2)}{\sin\theta(1-K^2\cos^2\theta)^{\frac{1}{2}}}\cos\omega\tau\right]$$

(A.23)

APPENDIX B

DF PROCESSOR BREADBOARD CIRCUITS

The DF Processor breadboard circuit diagrams are presented in Figures A1 through A4.

1. Schematic Diagrams

Figure A1 is a schematic diagram for the 2-Segment, Limiting Video Amplifier. This is basically a 3-stage amplifier preceeded by a low-noise PDA, and with a reference amplifier and d.c. feedback loop. Each stage has considerable negative feedback to provide gain stability over a wide temperature range and the limiting is accomplished using hot-carrier diodes in a bridge connection.

Figure A2 is a diagram of the high and low gain summing amplifiers and thresholds, the LVA threshold, the exponential sweep generator and the measurement control logic, described in Section 3.3.2.

Figure A3 is a schematic diagram of the video sampling circuit used in the processor breadboard. This circuit retains the amplitude of the video pulse approximately 100 ns prior to the pulse trailing edge; this is accomplished by generating the sample command at the trailing edge and preceeding the sampling portion of the circuit with a 100 ns delay line. The trailing-edge triggered sampler was used to allow for signal integration during a pulse, although the integration was not implemented in this breadboard. This type of sampler would be undesirable in a minor-lobe system because of multipath caused trailing-edge distortion.

Figure A4 shows the A/D conversion portion of the processor where the time differences corresponding to channel power level differences are generated and converted to digital form. The inputs to this section of the processor are the clock, the exponential sweep and sweep gate and various waveforms from the measurement control logic, and the sampled video levels.

As each comparator (A, B, C, D) changes state (at a time proportional to the level of that channel), its latch is set; the latches remain set until a processor reset pulse is generated. The latch outputs are used to generate three logic signals (C1, C2 and C3) which indicate when one or more latches have been set, two or more, and three or more. These logic outputs and the sweep gate are used to generate counter gates G1, G2 and G3, which are up from the leading edge of the sweep gate to the setting of the first latch, from the first latch to the second latch and from the second latch to the third latch respectively. Logic waveforms C1, C2 and C3 also generate strobe pulses which store the latch states after each transition in three separate registers, thereby preserving the channel order information.

Although decade counters were used in the breadboard system for readout convenience, binary counters are shown in the diagram and would probably be used in an operational system. A discussion of the DF Processor output format, including the number of bits required and the coding of the channel order information is presented in Appendix C. This Appendix.

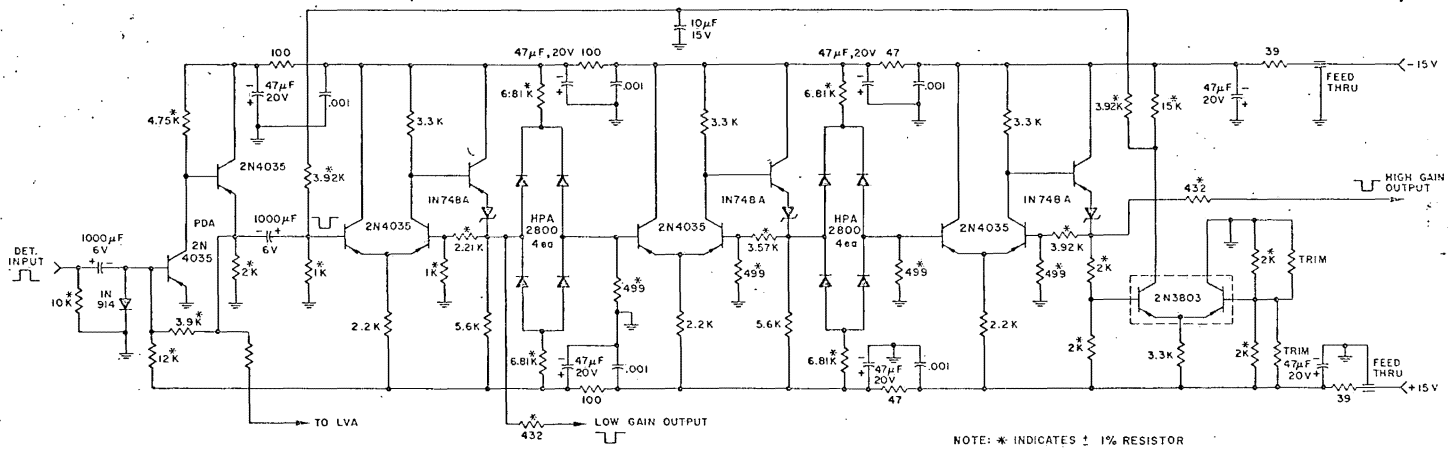


FIGURE A1 TWO-SEGMENT LIMITING AMPLIFIER SCHEMATIC DIAGRAM

A-9

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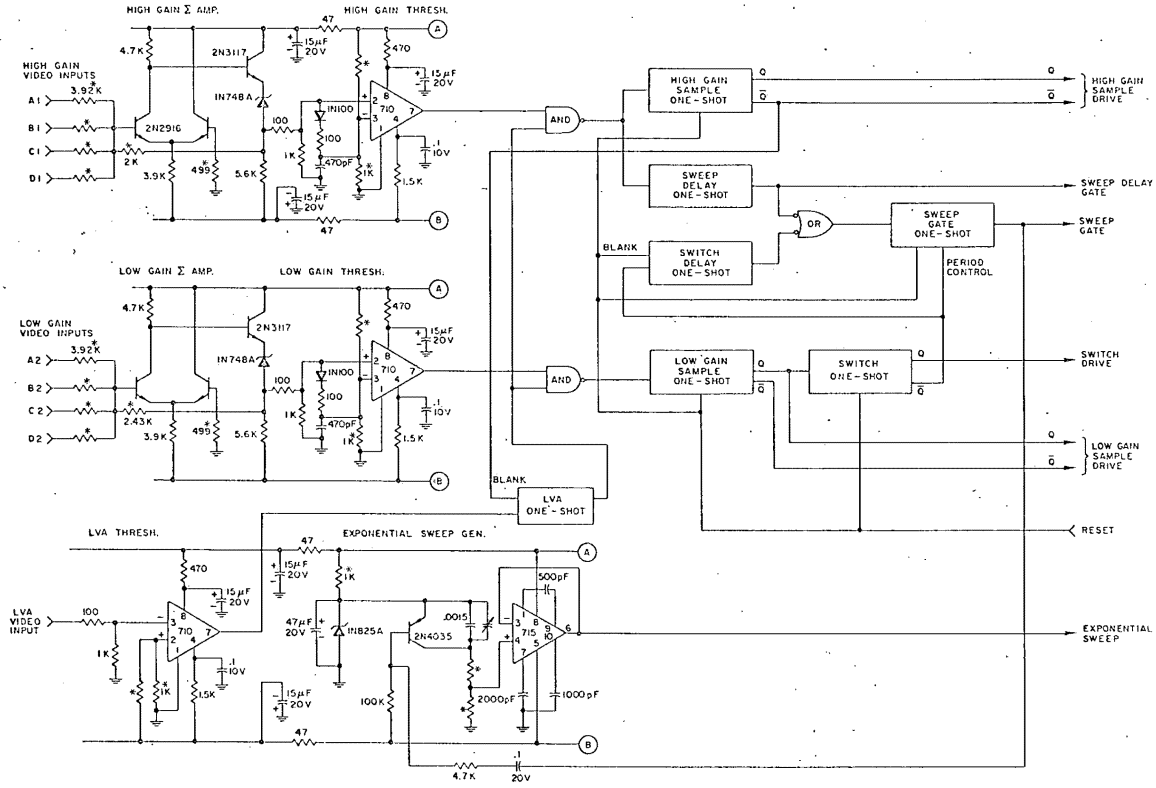

FIGURE A2 DF PROCESSOR THRESHOLDS AND CONTROL LOGIC

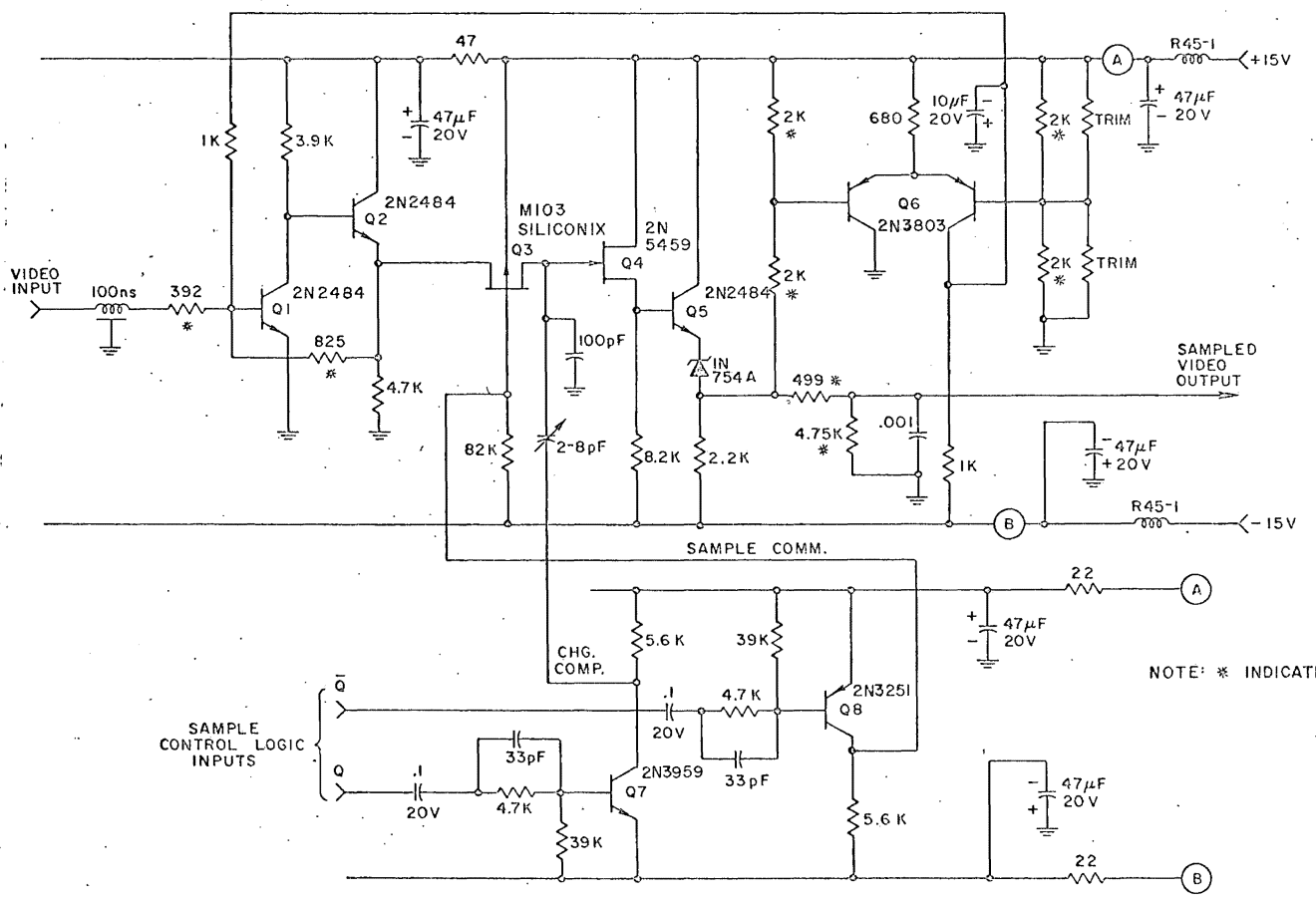

FIGURE A3 PULSE STRETCHER SCHEMATIC DIAGRAM

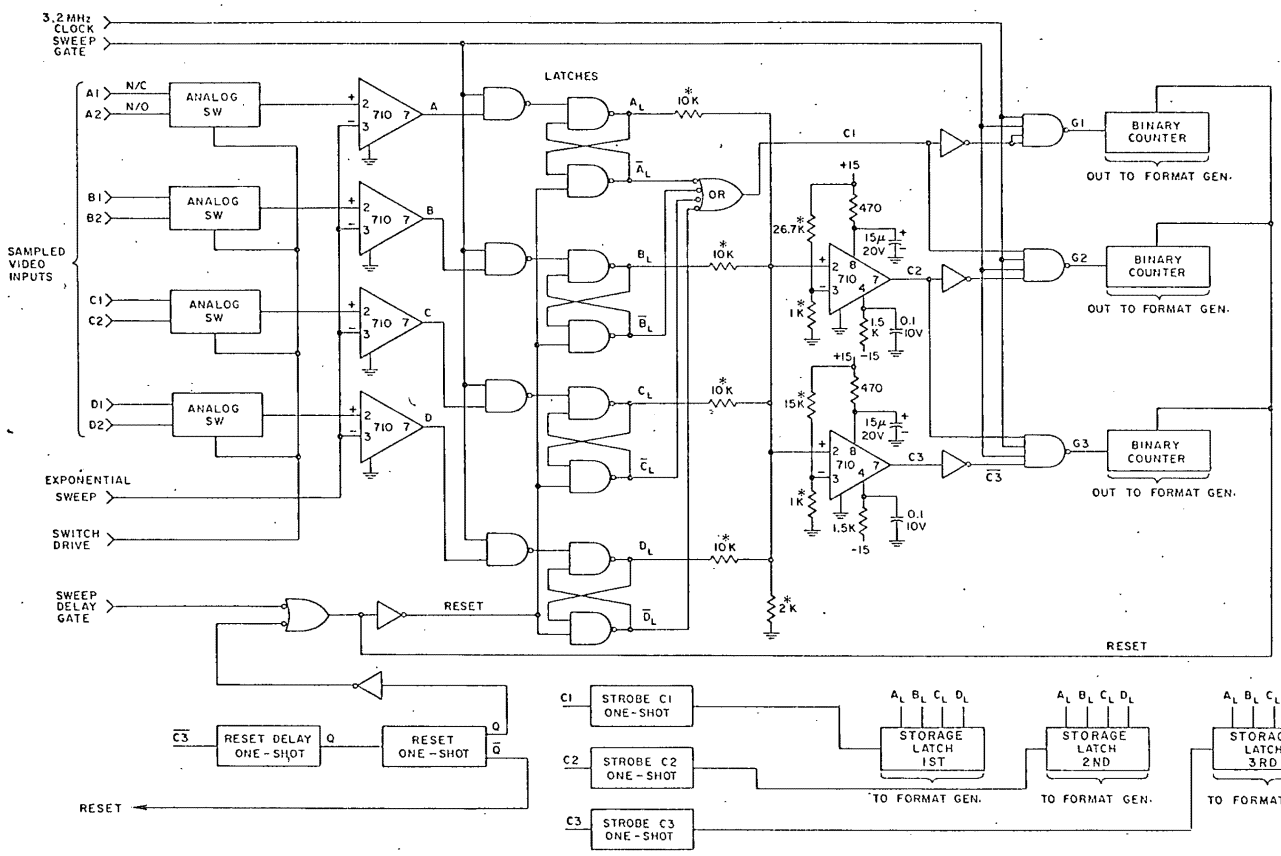

FIGURE A4 DF PROCESSOR A/D CONVERTER

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2. Two-Segment Amplifier and Pulse Stretcher Temp. Tests

The two segment linear amplifiers were tested at ambient temperatures of + 25°C, + 50°C and - 25°C. The transfer curves for both low-gain and high-gain outputs were taken at all three temperatures and are plotted in Figures A3 - 5. The low-gain output exhibited almost no change over the temperature range; the high gain channel changed gain by about 6% (0.5 dB) at - 25°C.

A pulse stretcher was also temperature cycled and the change in the output voltage at + 50°C is indicated in Figure A6.

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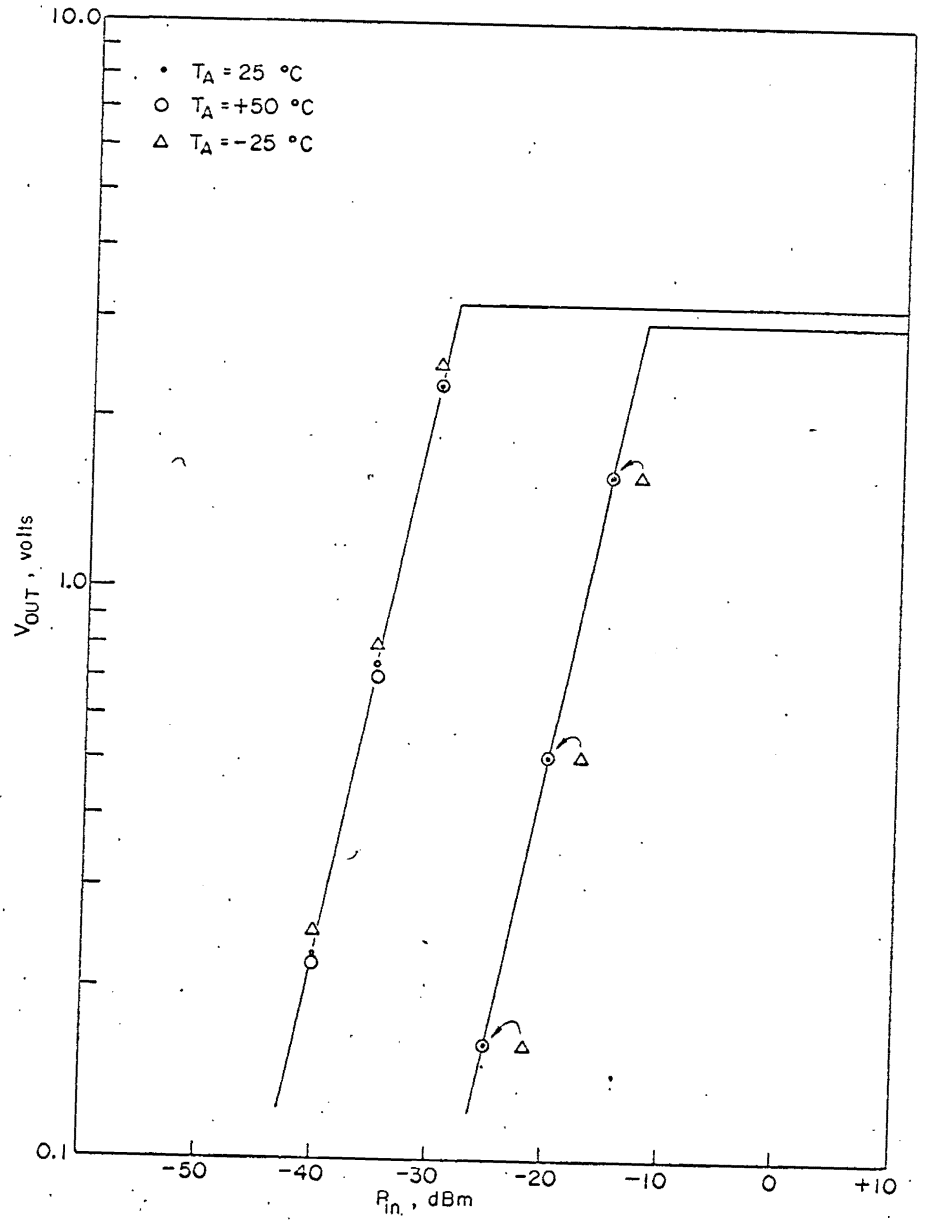

FIGURE A5 TWO-SEGMENT LIMITING AMPLIFIER TEMPERATURE CHARACTERISTIC

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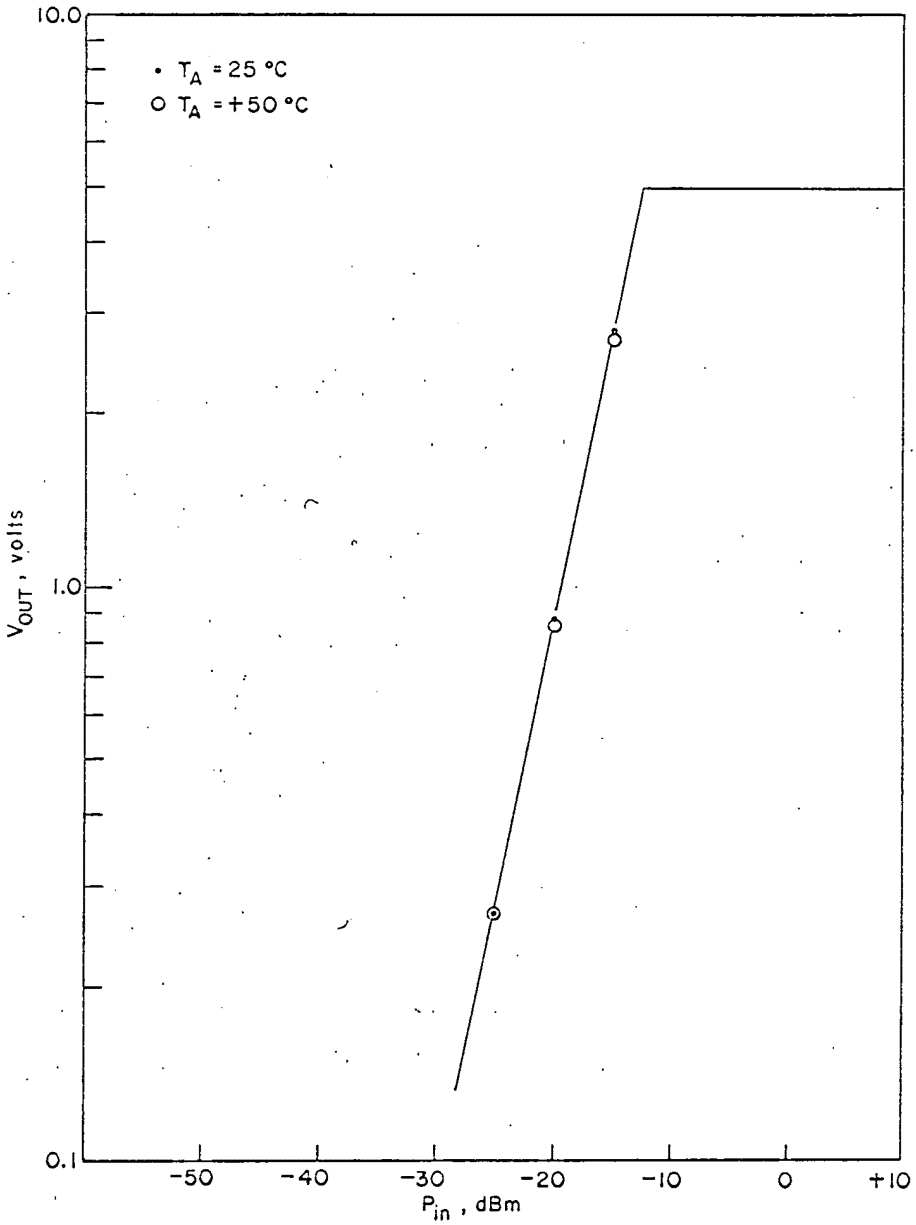

FIGURE A6 PULSE STRETCHER TEMPERATURE CHARACTERISTIC

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APPENDIX C

DF PROCESSOR OUTPUT FORMAT

The DF Processor output word format, which includes the absolute power reference, the power levels of the three highest channels, the identity of these three channels and their order in relative power is shown below:

Bit Number (readout order)

1	2 3 4 5 6 7	8 9 10 11 12 13	14 15 16 17 18 19	20 21 22	23 24 25	26 27 28
	High Channel Pwr. Level (6-bits)	2nd Channel Rel. Pwr. Level (6-bits)	3rd Channel Rel. Pwr. Level (6-bits)	High Ch. Ident. (3-bits)	2nd. Ch. Ident. (3-bits)	3rd Ch. Ident. (3-bits)

Reference Power Level (1-bit)

A total of 28 binary bits are required to transmit the necessary information. The power level count (bits 2 through 19) are available directly as outputs of binary counters; the power reference bit (bit-1) is generated from knowledge of which amplifier segment was being swept (high gain or low gain) when the first measurement was made. Some logic must be performed on the raw order information to generate the order code (bits 20 through 28). A logic diagram for generating the order codes is shown in Figure A7. The inputs are the six DF comparator/latch levels and the C1, C2 and C3 strobes which are generated when the first, second and third latches are set.

The six latches (A, B, C, D, E and F) drive three parallel in/serial out storage registers which are set at the strobe times C1, C2 and C3; during this time the storage registers are static. Thus, after strobe C3, register R1 contains 1's for all of the highest channels (normally a single 1 for the highest channel), register R2 contains 1's for the channels at the highest and second highest level and R3 contains 1's for the channels which are first, second and third highest in level.

These three registers are now clocked out in step with each other and a 3-bit binary counter,which indicates at each bit time (by a 3-bit code) which channel's history is being examined at the register outputs. When a "one" appears at the R1 output, the code for the channel being examined is stored in a 3-bit memory latch and is inserted in bits 20, 21 and 22 of the DF Processor output word. When a "one" appears at R2 simultaneously with a "zero" at R1 the code is stored in the "2nd level" memory and makes up bits 23, 24 and 25 of the output word; R3 operates in a similar manner. Since channels may have identical power levels (within the resolution limits of the system) the extra logic shown is required to handle these special cases; basically it allows R1 to control the first, second and third registers and R2 to control the second and third when necessary.

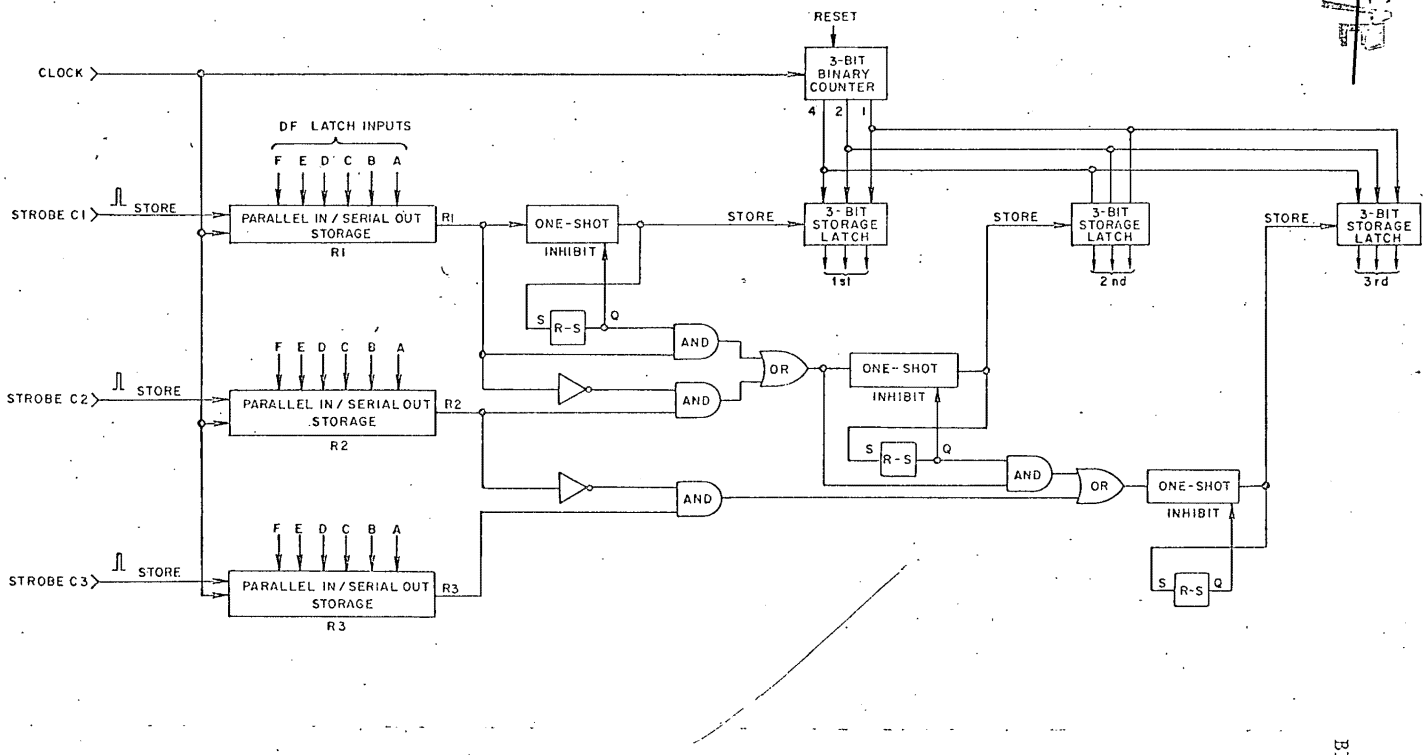

FIGURE A7 DF PROCESSOR CHANNEL ORDER STORAGE

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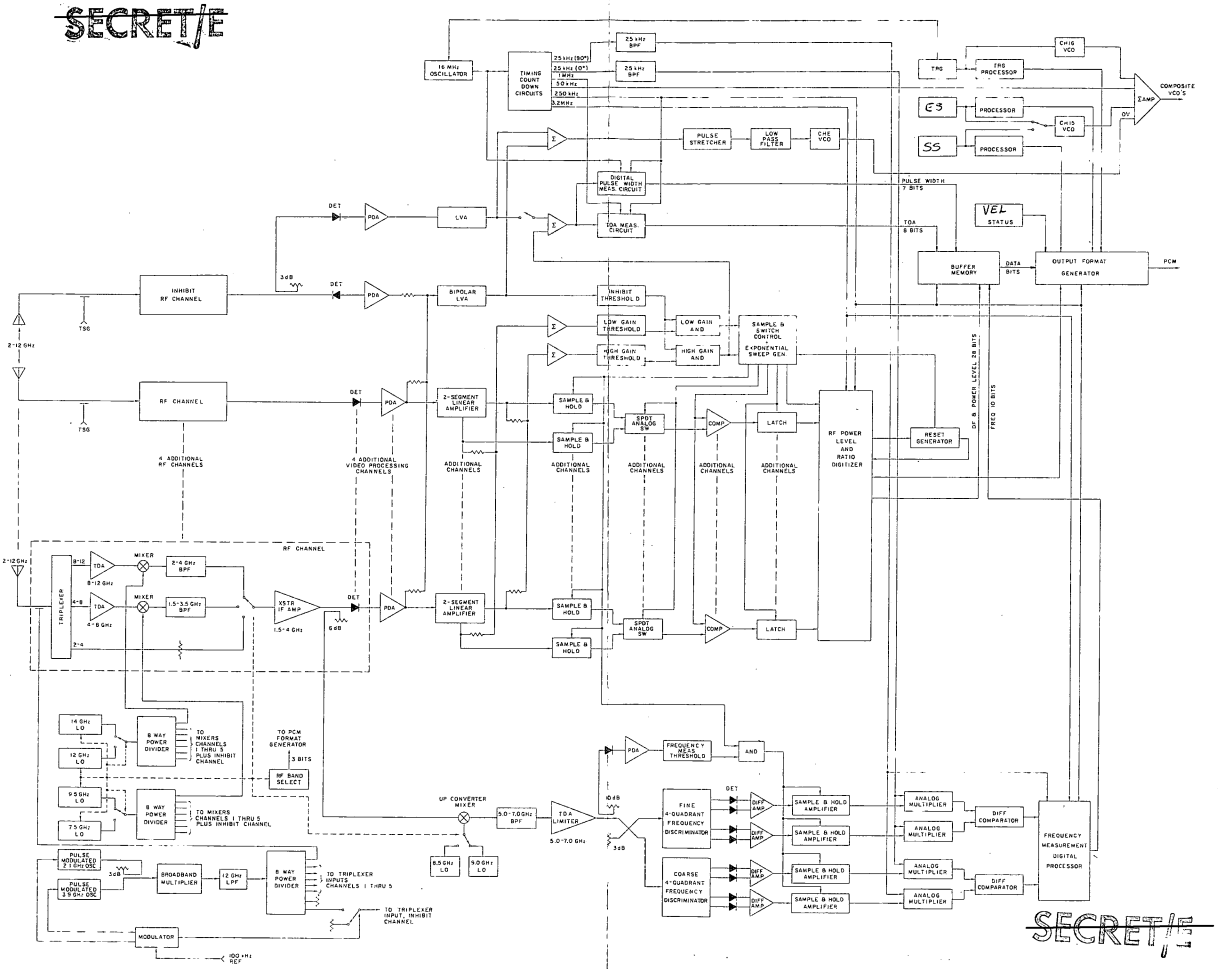

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FIGURE 3-33 DETAILED PAYLOAD BLOCK DIAGRAM