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COMPUTER SELECTION STATUS REPORT

6 February 1971

FRED V. HELLRICH

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Introduction

On 24 November, the second computer selection working group meeting was held in Room 200D, Bldg. 56, at NRL. Attendees at the meeting were: from NSA - [redacted] from NSG - [redacted]; from HRB-Singer - Joseph Riale; from NRL - Fred Hellrich and from NIC - Cdr. [redacted]

Since the first computer selection working group meeting, at which time the selection had been narrowed to three systems, a system had been tentatively selected as the optimum processor and configuration for the augmentation of the program. The system tentatively chosen is the System Engineering Laboratories Model 86 computer with associated peripheral equipment. This preliminary selection was primarily based on optimum performance of the system for the type of processing encountered in this program. Hardware and software support and training were also considered in the selection. Enclosure (1) summarizes the hardware characteristics and major performance characteristics of the Univac AN/UKY-7 and Xerox Sigma 5 and their relationship to the SEL 86. Software was not discussed in Enclosure (1) unless determined to be a serious deficiency.

where is Encl (2)

Enclosure (2) is a report of the technical discussion of the AN/UKY-7 held on 2 November 1970 at the Naval Ship Engineering Command between Fred Hellrich of NRL, [redacted] of NSG and [redacted] of NavSec.

Procurement schedule and methods

Because of the extreme difficulty of procuring a data processing system on a proprietary basis, the standard competitive method of procurement will be utilized. This will involve the following sequence of events: (1) writing specifications and evaluation criteria; (2) ADPESO approval of specifications and evaluation criteria; (3) synopsis and advertising of specifications by NRL Supply Division; (4) submission of proposals by manufacturers; (5) evaluation of proposals by NRL; (6) approval of proposals by ADPESO and GSA; (7) writing and awarding of contract. The anticipated completion of events for the procurement, delivery and deployment of the system remains as detailed in the enclosed schedule. Because of the intensive study undertaken for evaluating the computers available which would be capable of satisfying the anticipated processing requirements, no problems are anticipated in acquiring the best suited systems.

It should be noted that all agencies concerned will take part in evaluating the proposals submitted by vendors and that a final system selection will be based on the combined evaluation and agreement of NRL, NSA and NSG. Working group meetings will be scheduled as necessary for this.

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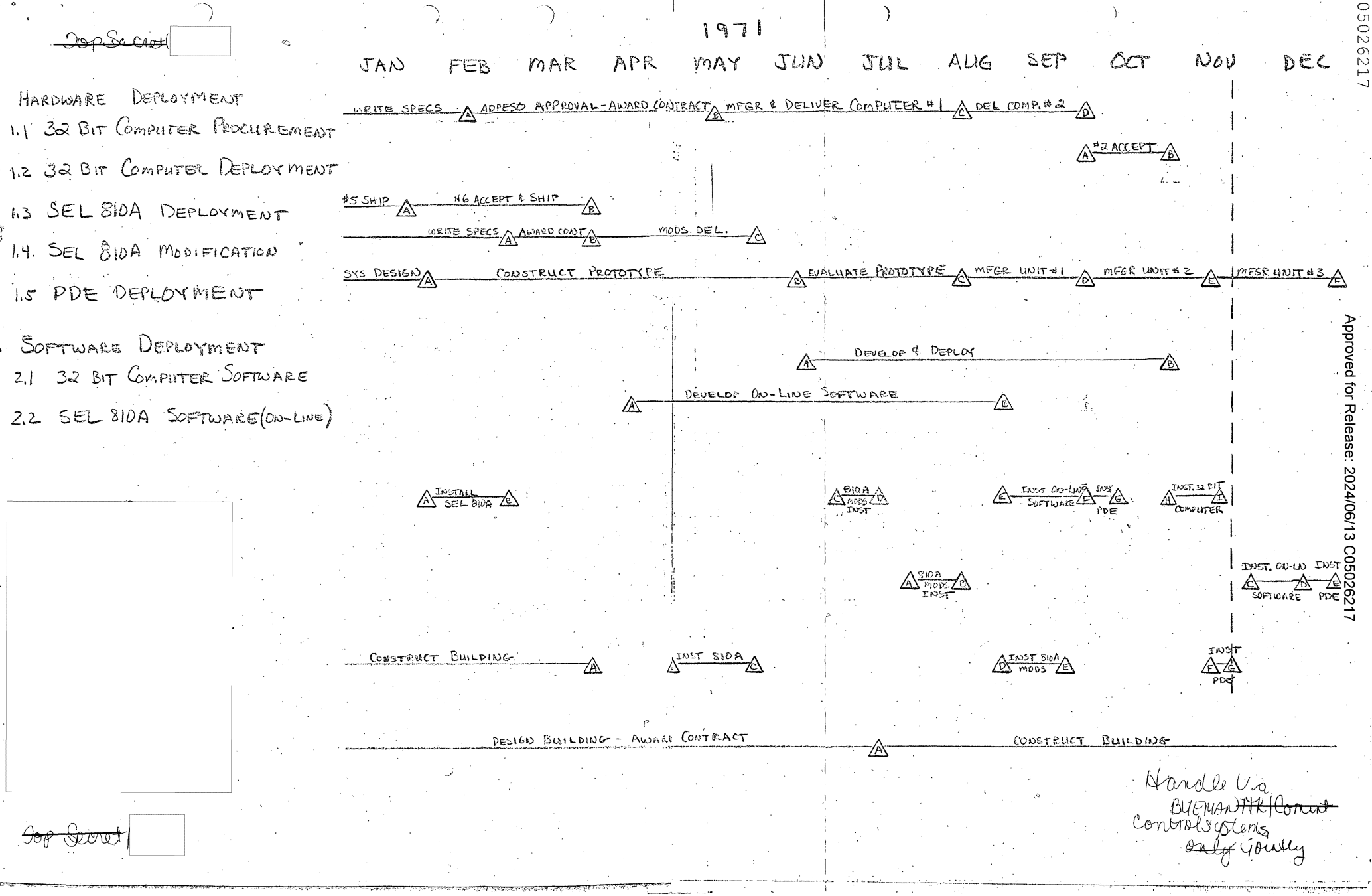

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COMPARISON

UNIVAC AN/UYK-7
XEROX SIGMA 5
SEL SYSTEMS 86

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I. UNIVAC UYK-7

The following list contains those characteristics of the UYK-7 system which we believe could prove to be serious shortcomings for our application.

A. The memory module size of 16K imposes an extraordinarily large memory size for optimum operation within our application. For example, to take maximum advantage of the UYK-7 hardware structure, we would need:

1. A minimum of two modules for input buffers such that the IØC can operate independently of the CPU (i. e., simultaneous input to one buffer and processing of the other).

2. A minimum of one module for the output buffer.

3. A minimum of two modules for the program (one for instructions and one for operands) so that we can use the memory overlap capability to offset the slow memory cycle time.

4. One module for the monitor.

This adds up to six 16K modules (96K memory) which is quite expensive considering that we would probably be effectively utilizing no more than 48-60K of this 96K. In addition, if we were to go with three input buffers for catch-up processing (where two are used for input and subsequent swapping to the fixed head disc, and one is used for processing) and if we wished to utilize two output buffers (where one is being output while the other is being filled by the processing routine), we would require eight 16K modules (128K memory).

B. The memory cycle time (1.5 usec) is the slowest of any machine being considered. This is somewhat offset by the CPU capability for memory overlapping; i. e., if the current operand and the next instruction are in different memory banks, the CPU can retrieve them in parallel.

However, maintaining an environment where all of the instructions and operands reside in

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different banks may prove to be extremely difficult. In addition, this situation could easily result in the wasting of memory.

C. The maximum guaranteed transfer rate for any one channel is only 167 KHz. Even under optimum conditions, the maximum rate will be only between 200-286 KHz.

D. There are only four distinct classes of interrupts. Within any of these four, software must determine (from the Interrupt Status Code) exactly what interrupt is to be serviced. This software identification scheme would definitely take more time than a hardware process.

E. If one wishes to permit an interrupt of the same class of interrupt being serviced, he must save the DSW's and interrupt group of registers so that the new interrupt won't destroy them.

F. Arithmetic is one's complement which may take some time to get used to, especially if one is working on the SEL-810A at the same time. Also, problems in converting some of the routines from the SEL-810A to the UYK-7 could conceivably arise due to this transition from two's complement to one's complement arithmetic. Additionally, the PDE design would have to be altered to provide a one's complement ATCØN format.

G. The floating point arithmetic package does not provide both single-precision and double-precision arithmetic. It operates with a format between single and double precision, where the fraction uses 32 bits and the exponent uses 16 bits. The exponent is expressed as a power of 2 (rather than 16); hence an exponent can range from -32767_{10} to $+32767_{10}$, which is less than the exponent range of the other machines being considered (16^{-64} to 16^{63}). Thus the floating point package for the UYK-7 is not as flexible as the other machines' packages and does not provide the precision granted by the others' packages.

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H. Presently, there is no FORTRAN IV compiler for the system; and the development of such a compiler is not envisioned in the near future. Needless to say, this would be quite a handicap for any attempt to convert existing FORTRAN programs. A procedure-oriented language, CMS-2, is being developed for the UYK-7 and should be completed in 1971; however, this would not aid conversion efforts. If we were to go with the UYK-7, then our applications programmers, who are proficient in FORTRAN, would have to spend time learning the CMS-2 language.

I. The Systems Software for the UYK-7 is accomplished under Navy sponsorship, where each package is developed under a contract. Therefore, the scope of the software evolution is totally dependent upon the Navy's direction and is not solely founded upon providing the software which is expected for a commercially-produced system.

J. The delivery time for a UYK-7 system should be defined. We seriously doubt that it is within the time frame which has been established for our operations.

K. Also, the price of the system has to be considered, and we do not currently have the figures for the UYK-7 available to us.

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II. XDS SIGMA 5

The following list includes those characteristics of the SIGMA 5 which we believe to be (1) serious shortcomings for our application or (2) weak points in respect to the other systems being considered.

A. A SIGMA 5 system may have a maximum of eight banks of core memory. Although this will pose no problem for our immediate application, which calls for 6-8 blocks of memory, it could conceivably be a detriment for future expansion of the real-time system.

B. From the standpoint of processing speed, the SIGMA 5 is considerably slower than the SEL-86. This comparison may be achieved by considering the following factors:

1. The memory cycle time of the SIGMA 5 is 850 nsec. as opposed to 600 nsec. for the SEL-86.

2. The memory referencing instructions for the SIGMA 5 take longer to execute than do their SEL-86 counterparts. For example, consider the following set of word referencing instructions:

Instruction	SEL-86 (usec.)	SIGMA 5 (usec.)	SIGMA/SEL
Add	1.2	2.0	1.67
Divide	10.8	15.8	1.46
Multiply	6.6	(7.2-8.9)	(1.09-1.35)
Load/Store	1.2	2.0	1.67
Compare	1.2	2.0	1.67
And/Or/Exclusive Or	1.2	2.0	1.67

3. The SIGMA 5 has no specific register-to-register (RR) instruction set (i. e., half-word instructions for RR operations). It handles RR operations by using a memory-referencing instruction where the second general-purpose register is given as the instructions's operand. In this manner, the CPU does not attempt to read from or write into memory. However, the 16 registers

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do not feed a matched set of adders for each register; therefore, in most cases, it takes additional time to access more than one register on RR operations since both registers must be supplied to the one common adder. Consider the following RR operation timings for the SIGMA 5 and the SEL-86:

RR Operation	SEL-86 (μsec.)	SIGMA 5 (μsec.)	SIGMA/SEL (relative to SEL)
Add	.6	2.16	3.6
Divide	10.8	15.96	1.48
Multiply	6.6	(7.36-9.06)	(1.12-1.37)
Transfer RR	1.2	2.16	1.8
Compare	.6	2.16	3.6
And/Or/Exclusive Or	.6	2.16	3.6

4. The immediate mode of addressing is very slow for the SIGMA 5. The following examples of immediate-address instructions can demonstrate this quite clearly.

Immediate-Address Instruction	SEL-86 (μsec.)	SIGMA 5 (μsec.)	SIGMA/SEL
Add	.6	1.8	3
Multiply	6.6	(7.2-8.9)	(1.09-1.35)
Load	.6	1.4	2.33
Compare	.6	1.8	3

5. Indexing adds to an instruction's execution time for the SIGMA 5 where it does not for the SEL-86. For example, indexing within a word referencing instruction adds .4 usec. to the execution time.

6. Indirect addressing adds more than the memory cycle time to the instruction's execution time for the SIGMA 5; it adds only one memory cycle (600 nsec.) per level of indirecting for the SEL-86. For example, indirect addressing within a word referencing instruction for the SIGMA 5 adds approximately 1.1 usec. to the execution time, where the cycle time is 850 nsec.

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7. The floating-point arithmetic package for the SIGMA 5 is considerably slower than that for the SEL-86.

Floating Point Function	SEL-86 (usec.)	SIGMA 5 (usec.)	SIGMA/SEL
Add	(2.4-3.6)	(4.9-9.9)	(2.04-2.75)
Add (double word)	(3.0-4.8)	(4.9-14.8)	(1.63-3.08)
Divide	11.4	(14.4-19.0)	(1.26-1.67)
Divide (double word)	21.8	(26.7-37.2)	(1.22-1.71)
Multiply	6.6	(9.5-12.5)	(1.44-1.89)
Multiply (double word)	11.4	(15.5-21.6)	(1.36-1.89)

C. The SIGMA 5 has no bit testing and manipulation instructions. This is a serious drawback for our data massaging and reformatting requirements. Whereas a significant portion of our analysis is dependent upon the detection of bits which define the data, bit testing and manipulation is very desirable. The alternatives, of course, are shifting a word or masking it to produce a data content which uniquely identifies a particular bit.

D. Indirect addressing is permitted only to one level and only post-indexing can be used with indirect addressing.

E. Only with a special interface that uses a separate port into memory can the maximum I/O transfer rate of one word per machine cycle be achieved (1.15 MHz).

F. An important factor to be included in the selection of a computer to meet our needs is the system cost.

Using the pricing which was quoted in the XDS Unsolicited Technical Proposal (deleting the cost of a card punch), a SIGMA 5 system which would do our job would cost approximately $710,000.

A comparable SEL-86 system which would also be capable of doing our application would cost approximately $570,000.

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Univac AN/UYK-7 Technical Discussion Report

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Enclosure (2)

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Univac AN/UYK-7 Technical Discussion Report

Technical discussions were held on 2 November 1970 at the Naval Ship Engineering Command between Fred Hellrich of NRL, Ens. [redacted] of NSG and Mr. [redacted] of NavSec concerning the AN/UYK-7 computer. This discussion was arranged by Fred Hellrich for the purpose of acquiring information about the AN/UYK-7 and its suitability for use in the augmentation of Siss Zulu Program. Briefly described herein is a summary of the discussion.

Methods of acquisition by this program of AN/UYK-7 and associated peripherals would consist of: (1) funds for the total system would be MIPR'd to NavSec. Only upon receipt of funds would NavSec respond and proceed to order the particular equipment from the various manufacturers. This would basically consist of an AN/UYK-7 central processor (Univac), a RD-294 Magnetic Tape Unit (Univac), an RO-280 High Speed Printer (Data Products), an RP-161 Card Reader (Philco), an RD-281 Disc File (IBM) and a Univac 1532 I/O console consisting of a typewriter and a paper tape reader-punch.

This ordering would actually just be adding the proper number of units to contract negotiations already progressing with each manufacturer.

Once the equipment is received from each of the various manufacturers, the responsibility of interfacing the peripherals to the central processor resides with the purchaser of the equipment. Technical assistance may be obtained from each of the various manufacturers by purchasing a technician for the time necessary to interface and debug the system. No commitment is given by any of the manufacturers of the system to guarantee a complete working system. Mr. [redacted] recommended at least one technician from each of the manufacturers of the equipment be procured for at least one month for interfacing the system.

Mr. [redacted] said that all AN/UYK-7 units to be produced for at least the next year have already been assigned to prime contractors for use in systems already under construction. This does not preclude the possibility of acquiring a AN/UYK-7 in less than a year, provided "pull" could be exerted at the proper level to divert two units to this program. Diverted units, however, may or may not suit the application of this program because of the construction of the CPU. Various

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parameters of the AN/UYK-7 must be specified at purchase time and the further the machine progresses down the production line, the more of these parameters are fixed into the unit and cannot be changed. For example, the AN/UYK-7 incorporates a read only memory that must be specified at purchase time. The wiring of the memory banks must be specified at purchase time. This is extremely important to this program, because, for the AN/UYK-7 to satisfy the high-speed I/O and processing requirements, memory interleaving must be utilized, and this requires special wiring of the memory bank. This one item places high doubt into the acquisition of a system early since no AN/UYK-7 has ever utilized interleaved memory and to the best knowledge of Mr. [redacted] none have been constructed.

Another system technical anomaly that arose in the course of discussion with Mr. [redacted] was that while the AN/UYK-7 was a 32 bit machine, all the peripheral controllers had a 30 bit interface, because they are a carry-over from the older 30 bit military CPU's. Although this does not prevent operation of the CPU with the controller or peripheral, quite a bit of efficiency is lost on I/O, and extra formatting and housekeeping must be done.

In the area of logistical support for the AN/UYK-7, Mr. [redacted] indicated that since the unit is so new, Naval technical maintenance instruction and Navy supplied spares would not be available before a year from now. Maintenance training on the AN/UYK-7, however, could possibly be obtained from Univac. No diagnostic type software is available for the AN/UYK-7 computer yet either. Diagnostic goals, however, are quite comprehensive. Design specifications at this time require that hardware fault isolation will be 75% to one P.C. card, 95% to three cards with the remaining 5% requiring a technician to probe with a scope and associated test equipment Tentative delivery of diagnostics is for not less than one year from now. Navy maintenance training does exist and spare parts have been incorporated into the Naval Supply System for all peripheral equipment, since the peripheral equipment has been in existence for some time.

The AN/UYK-7 and associated peripheral equipment is constructed to Military specifications and is ruggedized against shock, vibration, extreme temperature variations, and RFI. This is of course necessary for severe environment applications, such as ship board use. However, the use of this equipment for this program is strictly land base operation in a very well controlled environment meeting or exceeding the requirements for standard commercial equipment. The cost of constructing the equipment to military specifications is high. Also, upon inspection of the peripheral equipment available for the

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AN/UYK-7 system, it was found that under the RFI, shock and vibration enclosure, the standard commercial peripheral equipment existed. This would lead one to believe that with all the extra cost of military construction, the equipment would not be any more reliable than the standard commercial equipment when utilized in a commercial environment.

Approximate cost of the configuration determined necessary for this program's application is:

AN/UYK-7 Central Processer (Univac)	$400,000
RO-280 High Speed Printer (Data Products)	85,000
RP-161 Card Reader (Philco)	55,000
RD-281 Disc File (IBM)	247,000
RD-294 Magnetic Tape Unit (Univac)	80,000
Univac 1532 I/O Console	20,000
Hardware Total	$887,000
Engineering Services 10% of total	90,000
Total per system	$997,000

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