~~TOP SECRET~~

PROF-5

CENTRAL INTELLIGENCE AGENCY
WASHINGTON, D.C. 20505

2/26/1970

BYE-8098-70
Copy 1

MEMORANDUM FOR: Director, National Reconnaissance Office

SUBJECT : Electro Optical Imaging Program Status Report

In August 1969 the EXCOM directed a substantial expansion of the solid state Electro Optical Imaging (EOI) program, authorizing the immediate expenditure of [redacted] for development of critical components and technology, but restricting funds for systems level design work until further technology progress on the solid state array could be demonstrated. At that time, the Committee requested a review of progress in the technology programs in the January/February 1970 time period in order to determine whether or not additional funding appeared justified.

The purpose of this memorandum is to present to you the results of the tests and analyses that have been conducted to date and to let you know how supplementary FY 70 funds would be spent if they were made available. Attachments 1, 2, and 3 describe these results, and Attachment 4 describes alternative programs for the use of supplementary funds.

As you will see from the attachments, virtually all technical program objectives scheduled for January 1970 have been met or exceeded. In particular, we have accomplished the following:

1. We have demonstrated that arrays with the necessary performance can be fabricated in sufficient quantity and with adequate yield.

a. At [redacted] 5100 photo transistor devices were fabricated during the month of January, and the yield of the devices was about 0.4 percent. This was a larger yield than we anticipated for initial production. Those devices judged "useful" were those in which 96 percent of the detectors performed at or better than

BYE-8098/70 1 2

[redacted]

~~TOP SECRET~~

009-24-014

HANDLE VIA BYEMAN CONTROL SYSTEM ONLY

SUBJECT: Electro Optical Imaging Program Status Report

the design requirement of 1.2 microjoules/M^2, Noise Equivalent Signal (NES). Furthermore, all of them had a large fraction of detectors performing at two times better than the design requirement, and some had detectors performing four times better than the requirement. The measured input/output curves show that the detectors have sufficient dynamic range and that all detectors are well enough behaved over that range to be readily calibrated.

b. [redacted] whose program is a design cycle behind [redacted] produced and tested 1595 photodiode devices during January. The performance of these devices is about a factor of two poorer in the visible spectrum than that of the [redacted] phototransistor. However, the photodiode devices have substantially greater performance in the [redacted] and although we do not yet have enough data to quantify the overall performance gains that could be achieved by using the broadband characteristics of the photodiode, we believe that it is competitive with the phototransistor.

2. We have demonstrated the feasibility of assembling individual devices into the multiple device array. [redacted] has developed a laser trimming technique with the required precision for the edge trimming. A number of devices have been trimmed and subsequently tested to demonstrate that no degradation in device performance has resulted as a consequence of the trimming process. In addition, [redacted] has developed a modular assembly technique which appears to be both practical and dimensionally satisfactory. A mechanical model of a 12-device module has been fabricated to demonstrate compliance with the requirements. [redacted] is using chemical milling for edge trimming and is planning to experiment with laser techniques.

SUBJECT: Electro Optical Imaging Program Status Report

3. We have demonstrated that the electrical signals generated by a solid state array viewing a photographic scene can be geometrically processed into the correct format for image reconstruction and that, in this process, the signals from individual detectors can be calibrated to account for performance differences between detectors. Figure 2 of Attachment 2 is a representative picture generated using the [redacted] device. Figure 3 was generated using the [redacted] device. These pictures were constructed in the laboratory by imaging previously acquired photographs onto the solid state detectors. The illumination conditions and the test geometry were arranged so as to simulate the performance expected from the baseline image satellite design operating at an altitude of 280 nm. Both the calibration and the geometric processing are good enough so that no anomalies can be detected in the resulting imagery.

From these data, I think it is reasonable to conclude that we can now be confident that the solid state array can be fabricated economically with the performance needed to meet the satellite system requirements.

During the past five months, we have also made progress in developing the technology and confirming the feasibility of the other system components. Of particular interest is the progress on the optical system and the ground processing system.

1. In the optical area, [redacted] has been working on a 16-month contract which by December 1970 will produce detailed designs of two optical configurations and the completed fabrication and test of full size primary [redacted] and secondary mirrors. At the present time, [redacted] has completed its study of the various candidate configurations and has selected and confirmed the performance characteristics of the [redacted] design. Based on this work, we and [redacted] are confident that, with the advanced fabrication techniques that are now available to a development program, the optical components can be built with the necessary quality to meet system requirements.

SUBJECT: Electro Optical Imaging Program Status Report

2. Both [redacted] have completed preliminary ground processing facility design studies. These studies have shown that the necessary ground processing can be performed and images reconstructed for viewing within five minutes of receipt of the data. The overall complexity of the ground facilities required for the Electro Optical Imaging system will be roughly comparable to those required for the [redacted] system but probably not as costly as the [redacted] ground facilities. Considerable additional design study work will be required before a firm processing facility concept can be defined.

The optical and transducer activities will continue through June 1970 on funds already committed. [redacted] for example, we will continue to fabricate and test array devices, and in May we will [redacted] This will be a further confirmation of the capabilities already demonstrated in the Image Processing Laboratory. However, funds currently approved will not allow us to initiate certain new tasks which we think are timely and which would significantly increase the level of information that would be available to EXCOM for decisions this summer on the FY 71 program. In particular, we are ready now to begin engineering design studies of the solid state transducer and its associated on-board data processor. This is the next logical step in the component development, and the contractors are at a stage when they should begin this work. (It is worth noting that this design activity is a prerequisite to a precise definition of transducer and on-board processing reliability, a question that will be of great relevance to future EXCOM decisions.) We are also ready to begin system design studies. Indeed, the evolving component technology is suffering somewhat from the lack of guidance that needs to be provided by a systems level analysis. Again, many of the questions about overall systems performance and reliability that will be of interest to EXCOM this summer can only be addressed in this way.

SUBJECT: Electro Optical Imaging Program Status Report

On the basis of the foregoing then, we recommend EXCOM consider the possibility of providing supplementary funds in FY 70 for additional work. Two alternative plans for such funds and their estimated impact on a potential development program are as follows:

	FY 70 Supplementary	FY 71 Total	Start System Definition	Start System* Development
Option A			Mar 70	Mar 71
Option B			July 70	Aug 71

Option A pushes ahead at the maximum pace, beginning Phase I of the system definition immediately but allowing another decision point in July before Phase II is begun. We believe the technology could support this program if EXCOM wishes to proceed with this urgency.

Option B will provide for the additional work we think is timely and will provide a reasonable base of system information to support EXCOM deliberations this summer about whether to begin the system definition phases. It has the advantage of being a more deliberate program and of not requiring more FY 71 funds than the [redacted] already programmed for the system.

* In Attachment 4 we show a development schedule which would have initial operations occurring three years after the start of system development. This is based on what we consider to be a deliberate, reasonable schedule of events with no unnecessary development concurrencies.

SUBJECT: Electro Optical Imaging Program Status Report

A decision to provide no supplementary funds should recognize the fact that the EXCOM will then go into its FY 71 deliberations this summer with little more information about feasibility and overall system performance and cost than it has at its disposal at the present time.

CARL E. DUCKETT
Deputy Director
for
Science and Technology

Attachments: a/s

ATTACHMENT 1

SOLID STATE ARRAY DEVELOPMENT

PROGRAM PROGRESS

Reference (1) [redacted] Data Report, BIF-4C-0035-70

Reference (2) [redacted] Data Report, BIF-027-0004-70

INTRODUCTION

1. The solid state array transducer consists of an approximately linear arrangement of discrete solid state photosensitive detectors. For the Electro Optical Imaging System baseline design, each array consists of approximately [redacted] An array is built up from individual solid state devices or chips. Each chip contains a row of from [redacted] and associated amplification and switching logic for readout of the electrical signals. In practice better overall performance can be achieved by fabricating the photosensitive devices in two parallel, off-set rows of photosensitive elements. This arrangement permits the optimum shaping of each detector for best signal-to-noise ratio performance.

2. Figure 1 is a schematic view of two solid state devices or chips, showing the two parallel rows of detectors and the mechanical interface between adjacent chips. The better arrangement is shown at the top of Figure 1 where two rows continue from one chip or device to the next without any apparent discontinuity. An alternative arrangement is shown in the bottom of Figure 1 where the photodetector rows are offset from one chip to the next. This offset can be taken into account in the data processing as long as it is not excessive. In any case, the edges of the chips must be precisely trimmed and a mechanical arrangement devised for assembling the individual chips into a multi-chip array.

Attachment 1 to
BYE 8098-70

DESIGN REQUIREMENTS

1. An individual photodetector must meet a number of performance requirements in order to provide a useful capability in the context of the Electro Optical Imaging System. The most important of these are sensitivity, uniformity of response, spectral response, and detector transfer function (or detector shape). In addition, the individual solid state chips must be within the current fabrication state-of-the-art so that useful solid state fabrication yields can be achieved at a reasonable cost.

2. Table 1 lists performance specifications that have been established for the current phase of the solid state array technology programs. The sensitivity is measured in terms of the noise equivalent signal (NES). The noise equivalent signal is the minimum detectable input signal to a solid state array in that the noise equivalent signal will produce a peak-to-peak output equal to the rms electrical noise of the detectors. Based on early system studies, the NES has been set at a level of 1.2 microjoules/M^2. This sensitivity will permit the design of imaging satellites with an image quality better than two foot equivalent ground resolution operating in the altitude region of 200 - 300 n. m. An additional specification related closely to sensitivity is detector integration time. The current specification calls for measuring the noise equivalent signal at an integration time of one millisecond. This integration time is short enough to meet the overall system requirements with a reasonable frame time. This number also impacts the design of the attitude control system and one millisecond is practical from this standpoint.

3. The uniformity of the individual detectors must be bounded so that the dynamic range of all detectors overlaps in a sufficiently broad region of exposure. Because of the extreme dynamic range of the solid state detectors, this requirement imposes no real constraint. However, it is desirable to have the detector arrays as uniform as possible so as not to place an undue burden on the communication system. A preliminary uniformity specification calls for an offset and gain variation of no more than 4 to 1 over the entire array.

4. The dynamic range of the detector has been specified at 600 to 1. This again turns out to be more a communications design requirement than a detector requirement in that the solid state

detectors of interest have inherently a much greater dynamic range than is required for the Electro Optical Imaging system application.

5. The spectral response of the photodetectors must be sufficiently broad band to produce useful imagery. Again the solid state detectors of interest inherently possess broad band characteristics. For purposes of standardizing measurements, the performance specification calls for measuring array sensitivity over the spectral band of 0.4 to 0.8 microns. In addition, solid state detectors offer the inherent potential of good sensitivity beyond 0.8 microns to as far as 1.2 microns. There are indications that this portion of the spectrum can be used to advantage in the Electro Optical Imaging system. However, no firm performance specification in this regard has yet been established.

6. The shape of each individual detector must be controlled so as to provide an adequate modulation transfer function. This, coupled with the array pitch or spacing between detectors, will determine the limiting resolution of the array. It turns out that array pitch, detector area, and detector transfer function are interrelated for an optimum detector array design. These array characteristics are determined by the geometry of the masks used in the solid state fabrication process. An individual detector shape having rectangular dimensions of 0.9 mils and 0.7 mils has been specified. This shape is consistent with an array pitch of 0.6 mils. The entire array can be scaled either larger or smaller without any important overall system changes. The 0.6 mil pitch was selected as a reasonable design point based on solid state fabrication state-of-the-art and optical system design and packaging convenience.

7. The baseline Electro Optical Imaging system design calls for a solid state transducer consisting [redacted] linear arrays. Each linear array contains [redacted] Depending upon a final selection of the number of detectors per solid state chip, each array will require between [redacted] for a total requirement of [redacted] per transducer. This is a relatively small number of solid state devices by current integrated circuit standards. The number is small enough so that the program requirements can be met by a pilot plant production facility rather than a full scale manufacturing operation. However, in order to meet this objective a reasonable yield must be realized. An initial yield goal of between 0.1% and 1% has been established. The yield will be determined by

the complexity of the chip (the number of detectors on each chip) and the level of performance required of the chip. Therefore, the yield requirements couple back to the other performance requirements.

8. There are currently two major solid state array technology programs under way. The first of these is based on photodiode solid state detectors being carried forward by [redacted] The second of these is based on phototransistor solid state detectors being carried forward by [redacted] These technology programs as currently structured have three primary objectives:

a. Demonstrate that the performance requirements discussed above can be met with useful yields.

b. Assess the feasibility of assembling the individual photosensitive devices into large arrays.

c. Develop solid state arrays that demonstrate actual imaging performance.

9. Both [redacted] have completed major tasks in all three of these areas during January. The remainder of this attachment is a report on the photoelectric testing conducted by the two contractors as well as work relating to the assembly of the individual detector chips into larger arrays. Attachment 2 discusses the imaging tests completed using array breadboards delivered by both [redacted]

SOLID STATE DEVICE PHOTOELECTRIC TEST RESULTS

1. The photoelectric tests cover a series of definitive device (chip) level quantitative tests. The most important of the tests are sensitivity, measured in terms of noise equivalent signal, input/output characteristic curve, spectral response, and individual detector area profile measurements. In addition, a number of secondary performance characteristics are measured at the photoelectric test level. In general the photoelectric tests are conducted by mounting the solid state devices in an optical bench and illuminating the devices with carefully calibrated light sources. The devices are then operated in the dynamic mode as they would be in actual imaging performance in

a system, and the output electrical signals recorded. The output data is then computer processed and the appropriate performance measures derived,

2. As there are on the order of [redacted] per device, and many devices must be measured in order to collect a meaningful quantity of performance information, huge quantities of raw data must be collected and processed. Both [redacted] now have operational semi-automatic test facilities to support the collection of this data in a timely and efficient manner. Both companies also now have operational an appropriate library of data reduction computer programs to handle the raw data and generate reports in the various formats required. As has been mentioned above, both companies have now delivered their first major data reports generated using the new test facilities and data reduction programs.

3. The most critical measurement in the photoelectric test series is the noise equivalent signal measurement. As has been mentioned above, the noise equivalent signal by definition is the rms fluctuation in the output of a given solid state detector. This quantity is determined by recording a large number of successive detector readouts (64 in the case [redacted] and 128 in the case [redacted], and examining the statistical characteristics of the distribution of this collection of output signals. This measurement must be made for each detector on a given device at a number of different illumination levels over the useful range of the device to insure that all noise contributing sources are taken into account.

4. The test data reported below is summary in character. It does not represent a comprehensive report on the total information available. However, data presented does support the conclusion that solid state detectors arrayed in appropriate device configurations can be fabricated with useful yields and with the characteristics required for Electro Optical Imaging systems application.

TRW PHOTOTRANSISTOR TEST DATA

1. The [redacted] data report (Reference 1) is based on several production runs during the month of January. All told, [redacted] devices or chips were fabricated. The yield, through initial

functional testing, wafer dicing and packaging for test purposes, gave 82 devices on which all detector channels were functional. At the time the data report was written, 25 of these devices had gone through detailed photoelectric testing. Of these 25, eight devices appeared to be good enough for Electro Optical Imaging system application. At this point in the development program, this judgment is a qualitative one in that detailed acceptance criteria have not yet been defined.

2. The noise equivalent signal data on the 25 chips reported on is summarized in Table 2. Each line of the table corresponds to one device with 125 detectors recorded. The established noise equivalent signal specification for the purposes of the current technology program is 1.2 microjoules per square meter measured at a one millisecond integration time in the spectral band 0.4 to 0.8 microns. Table 3 contains more detailed information on the eight best chips of the 25 tested.

3. The best detector column shows the noise equivalent signal for the least noisy detector on each chip. The worst detector column correspondingly shows the noise equivalent signal for the noisiest detector on each chip. The body of the table shows the distribution of noise equivalent signal measurements in four categories: number of devices with noise equivalent signals lower than 0.6; number of detectors between 0.6 and 1.2; number of detectors between 1.2 and 2.0; and, number of detectors greater than 2. The data in Table 3 shows that most of the detectors on most chips had noise equivalent signals a factor of two better than specification (that is, the NES was one half the requirement). Table 3 also shows that every chip had at least one detector with an NES of better than 0.4 microjoules per square meter. The best detector data is indicative of the inherent performance potential of the basic photodetector devices.

4. Only one chip out of the eight had all detectors better than specification. However, on the other seven chips there were at most five detectors poorer than specification. In operation, these detectors would show up as slightly noisier channels and under most scene conditions would not be apparent in the reconstructed imagery.

5. Figure 2 is a typical input/output curve for the phototransistor detectors. The curve is the average for all detectors on one chip. The vertical lines show at each measured illumination level the lowest response detector on the chip and the highest response detector on the chip. This spread of input/output characteristics must be accounted for in the ground calibration process before reconstructing the imagery. The measurements as presented in Figure 2 show that (1) all detectors overlap over a dynamic range which is greater than would be encountered in any real operational situation, and (2) all detectors on the chip are well behaved and, therefore, can be readily calibrated with a straight forward calibration algorithm. The Image Processing Laboratory imaging testing discussed in Attachment 2 used a chip which was far worse than any of the 25 chips reported in the recent test data package and successfully generated good quality images with a simple six point calibration process.

6. Spectral response curves were measured on selected detectors from the 25 chips. There are small variations from detector to detector but these variations will not have a significant impact on device performance. A typical curve is shown in Figure 3. The curve is plotted in terms of relative response. The quantum efficiency at the peak of this curve is approximately 0.9. This high quantum efficiency is characteristic of pn junction-type detectors.

7. Response profiles for individual detectors were also measured. These response profiles demonstrated that the size and shape of the sensitive area can be controlled with sufficient precision by simply adjusting the final metallization masking.

WESTINGHOUSE PHOTODIODE TEST RESULTS

1. The [redacted] photoelectric test data report (Reference 2) was based on January production runs totaling [redacted] chips. Out of these [redacted] chips, a total of 20 were completely functional after dicing and packaging. All of these devices have been through complete photoelectric testing.

2. The [redacted] chip tested is not the final chip configuration. The detector photosensitive areas have the desired size and shape but are [redacted] rather than at the [redacted] Electrically, the chip under test has

circuitry similar to that of the final design. Table 4 shows the noise equivalent signal measurements for the 20 devices. As in the case of the data, each line of the table shows the distribution of noise equivalent signal (NES) measurements from one device. Table 5 shows NES data for the eight best devices from Table 4.

3. In general, it can be said that the photodiode test results to date show a noise equivalent signal performance approximately a factor of 2 poorer than phototransistor devices. This is seen most directly by looking at the best detector column of Table 5 and comparing it to the similar column in Table 3. However, as was expected based upon fabrication considerations, the photodiode devices show less performance dispersion in that the noise equivalent signal measurements on the individual detectors within a chip are more tightly grouped. This can be seen again most directly by comparing the worst detector column of Table 5 to the corresponding column in Table 3.

4. The noise equivalent signal measurements were made for both devices in the 0.4 to 0.8 micron spectral band pass. Figure 4 shows the photodiodes response curve. It is clear from inspection of this data that for a noise equivalent signal measurement in a broader pass band, for example, 0.4 to 1.0 micron, the photodiode response would be considerably better than that measured. In the portion of spectrum from 0.8 to 1.0 micron, the phototransistor device has very little response whereas the photodiode detector has its maximum response. The utility of the broad band characteristic of the photodiode detector for the imaging application intended is now being intensively investigated, both experimentally and analytically.

5. Figure 5 is a typical input/output characteristic curve for the photodiode detectors. As in the case of Figure 2 for the phototransistors, this curve is an average curve for all detectors on one device. The vertical bars show the dispersion from the lowest response to the highest response detector at each measured input light level. This data again shows that the photodiodes are high dynamic range, well behaved devices. Although the individual detectors are considerably more uniform than was originally expected, they are not sufficiently uniform to eliminate the requirement for calibration prior to image reconstruction.

SUMMARY

In general, the photoelectric test results to date have been very encouraging, both in the case of the phototransistor detectors and the case of the photodiode detectors. The best detectors have been substantially better than the noise equivalent signal specification originally established. The phototransistor test data has shown that even in this pre-production phase of the program useful overall device yields have been achieved. While the [redacted] photodiode program is approximately one design cycle behind the [redacted] phototransistor program, the results there, given the overall status of the program, have been equally encouraging.

10

TABLE 1

PRELIMINARY SOLID STATE

ARRAY PERFORMANCE REQUIREMENTS

Sensitivity (Noise Equivalent Signal at one ms integration time)	Less than 1.2 microjoules/ M^2
Spectral Response	0.4 to 0.8 microns
Uniformity	Better than 4:1
Dynamic Range	600:1
Transfer Function	0.32 at 32.8 lp/mm
Array Pitch	0.6 mils
Chip-to-Chip Offset	Less than 2.4 mils

Table 2

PHOTOTRANSISTOR CHIP NES STATISTICS

SPECIFICATION: 1.2 Microjoules/M^2

DETECTOR NOISE DISTRIBUTION (NES)				#DETECTORS	WORST DETECTOR
<0.6	0.6-1.2	1.2-2.0	>2.0	ABOVE SPEC	Microjoules/M^2
24	77	23	1	24	2.3
66	55	3	1	4	3.3
35	85	2	3	5	2.8
69	39	7	10	17	25.5
108	12	4	1	5	2.6
101	19	2	3	5	4.7
102	16	2	5	7	17.0
103	19	0	3	3	7.8
95	25	1	4	5	8.7
92	27	3	3	6	16.2
108	9	4	4	8	6.2
99	19	0	7	7	10.2
107	13	2	3	5	12.6
112	8	3	2	5	4.5
64	20	13	20	33	---
27	77	11	10	21	8.5
111	9	3	2	5	8.0
76	35	3	11	14	15.7
27	68	24	6	30	5.7
118	7	0	0	0	0.8
67	49	5	4	9	13.6
115	8	1	1	2	2.4
99	23	1	2	3	4.0
87	31	5	2	7	5.2
89	29	5	2	7	5.8

~~TOP SECRET~~

Table 3

EIGHT BEST PHOTOTRANSISTOR CHIPS

BEST DETECTOR Microjoules/M^2	DETECTOR NOISE DISTRIBUTION (NES)				WORST DETECTOR Microjoules/M^2
	<0.6	0.6-1.2	1.2-2.0	>2.0	
0.3	118	7	0	0	0.8
0.3	115	8	1	1	2.4
0.4	66	55	3	1	3.3
0.3	100	12	4	1	2.6
0.4	99	23	1	2	4.0
0.3	112	8	3	2	4.5
0.3	111	9	3	2	8.0
0.4	35	85	2	3	2.8

BYE-8098-70

~~TOP SECRET~~

~~SECRET~~

Table 4

PHOTODIODE CHIP NES STATISTICS

SPECIFICATION: 1.2 Microjoules/M^2

DETECTOR NOISE DISTRIBUTION (NES)				#DETECTORS	WORST DETECTOR
<0.6	0.6-1.2	1.2-1.0	>2.0	ABOVE SPEC	Microjoules/M^2
0	18	42	36	78	5.4
0	25	53	18	71	---
5	28	59	4	63	2.2
0	14	35	47	82	---
6	38	48	4	52	35
0	38	52	6	58	---
1	52	33	10	43	---
13	67	14	2	16	---
0	12	43	41	84	---
0	4	48	44	92	4.6
3	18	61	14	75	---
0	21	48	27	75	---
0	5	61	30	91	---
1	54	29	12	41	2.5
0	9	44	43	87	61.0
0	4	25	67	92	4.1
0	5	25	66	91	4.3
0	4	21	71	92	---
0	5	45	46	91	3.3
0	10	24	62	86	4.7

BYE-8098-70

~~SECRET~~

Table 5

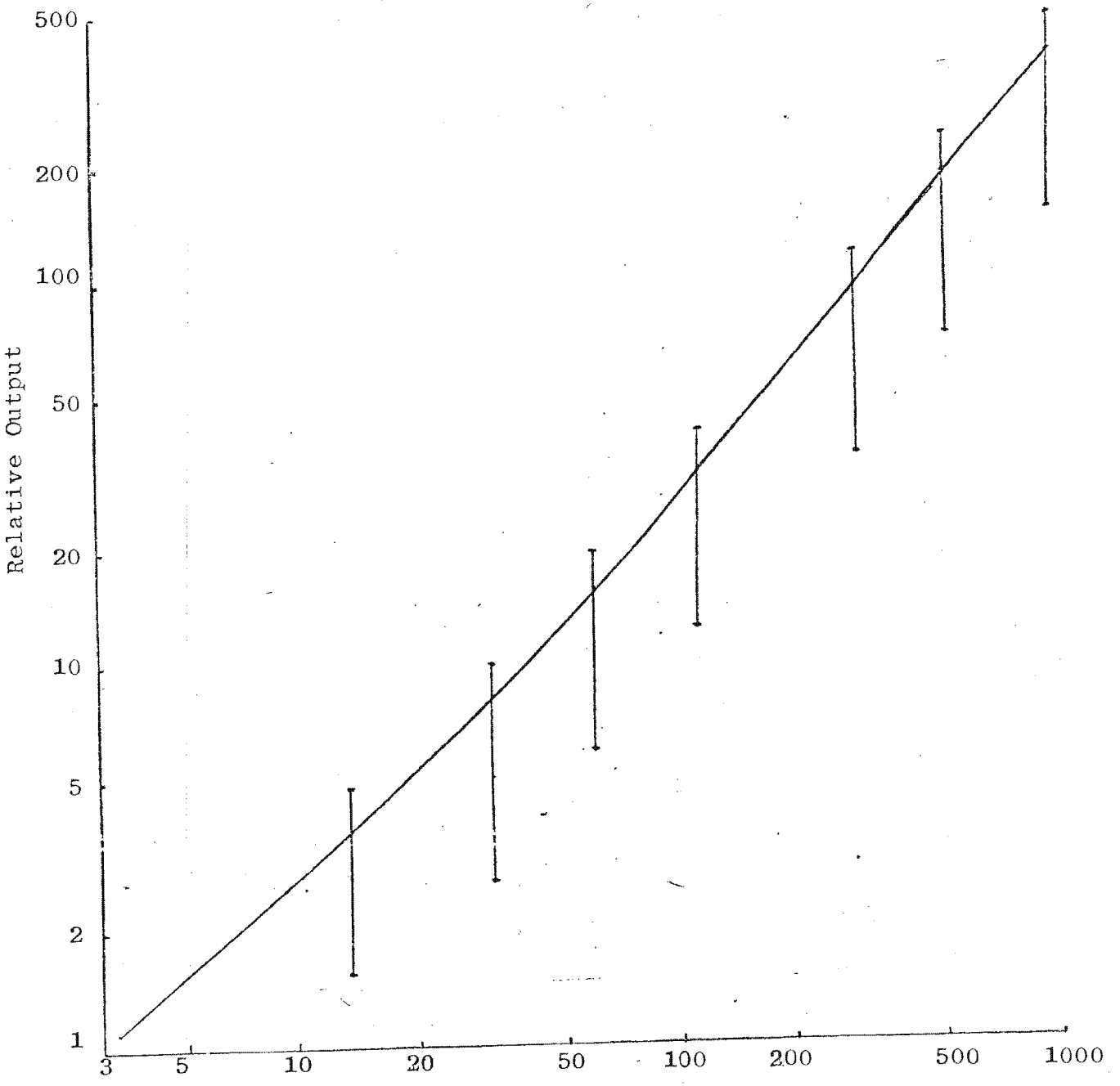
EIGHT BEST PHOTODIODE CHIPS

BEST DETECTOR Microjoules/M^2	DETECTOR NOISE DISTRIBUTION (NES) <0.6	0.6-1.2	1.2-2.0	> 2.0	WORST DETECTOR Microjoules/M^2
0.79	0	18	42	36	5.4
0.44	5	28	59	4	2.2
0.73	0	4	48	44	4.6
0.52	1	54	29	12	2.5
0.99	0	4	25	67	4.1
1.03	0	5	25	66	4.3
0.81	0	5	45	46	3.3
0.73	0	10	24	62	4.7

BYE-8098-70

Figure 2

PHOTOTRANSISTOR TRANSFER CHARACTERISTICS
MEAN AND PEAK DEVIATIONS FOR
CHIP NUMBER 41-49-8-9



BYE-8098-70

Figure 3
Phototransistor Spectral Response

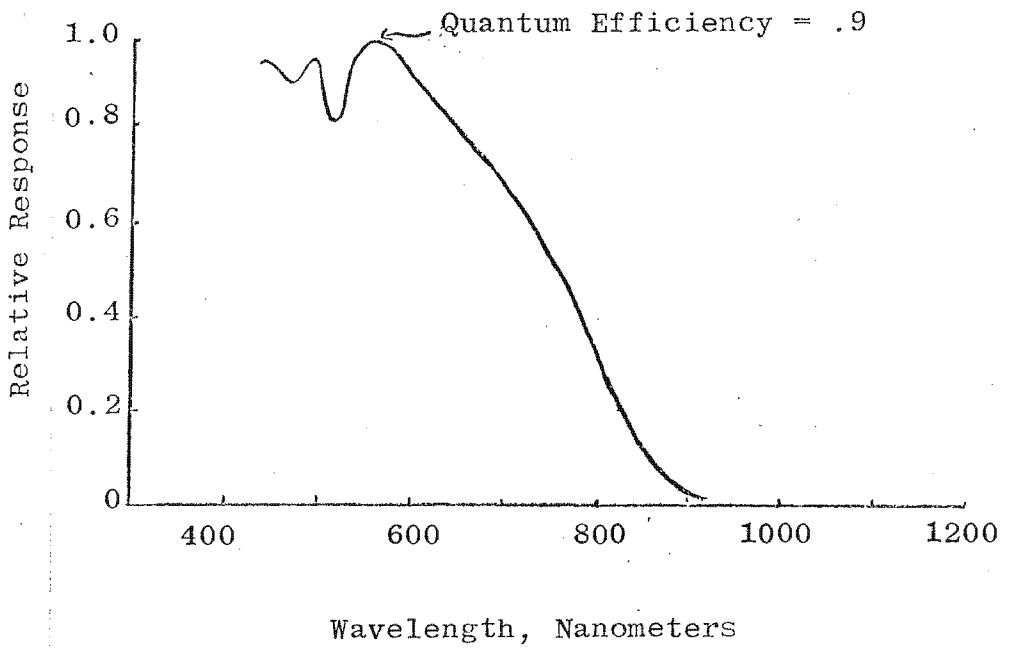
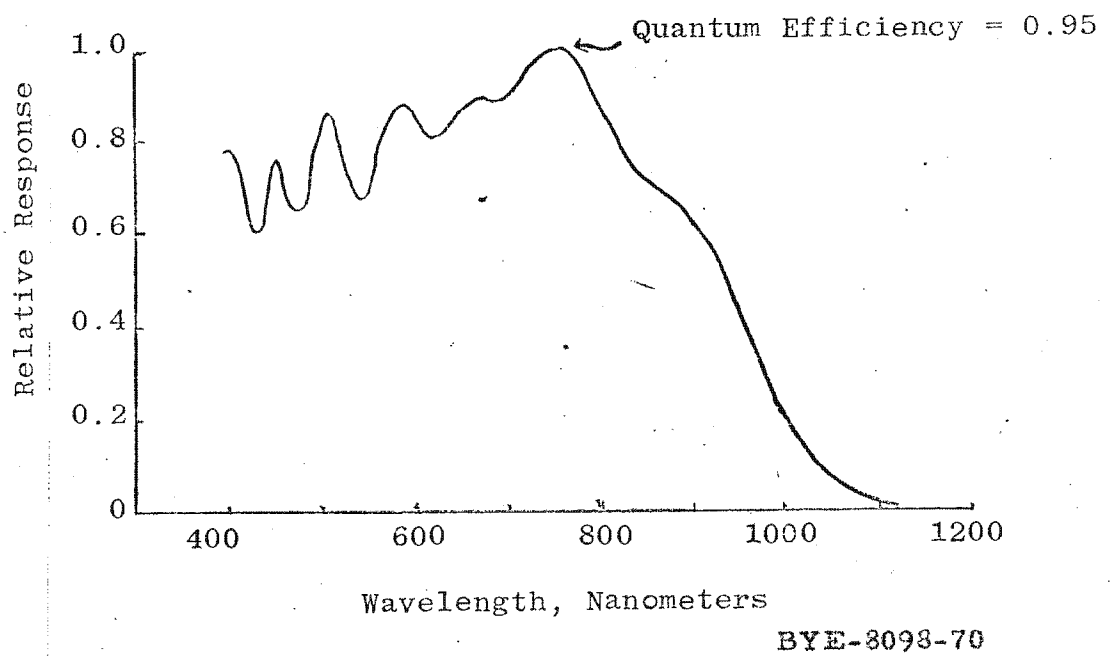


Figure 4
Photodiode Spectral Response

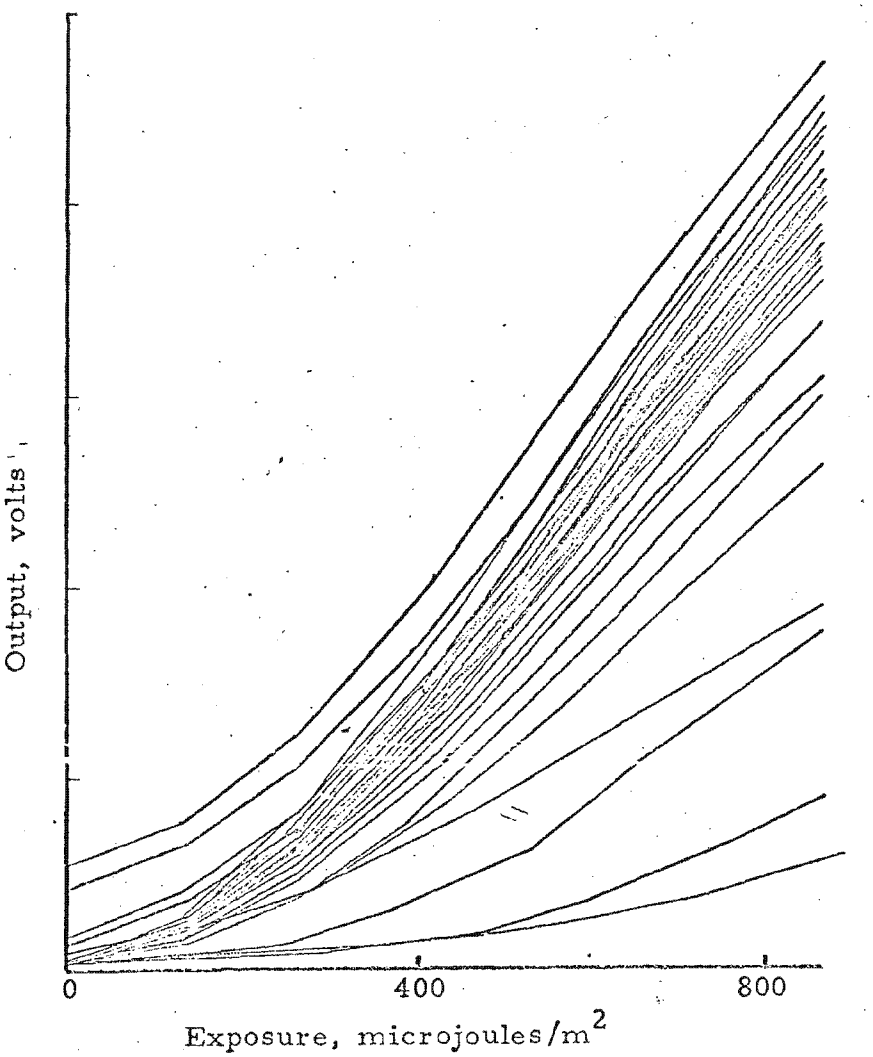


BYE-8098-70

FIGURE 5

TRANSFER CHARACTERISTIC CURVES

FOR [redacted] ARRAY



BYE-8098-70
HANDLE VIA BYEMAN
CONTROL SYSTEM ONLY

FIGURE 6

TRANSFER CHARACTERISTIC CURVES

FOR [redacted] ARRAY

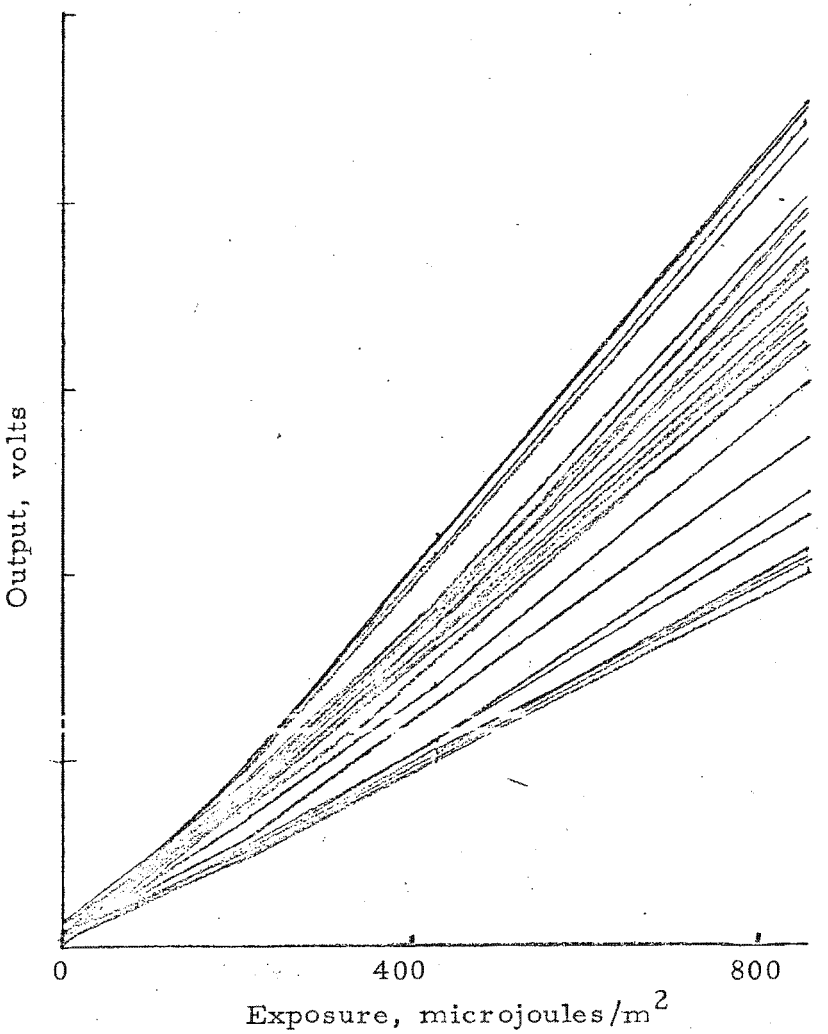
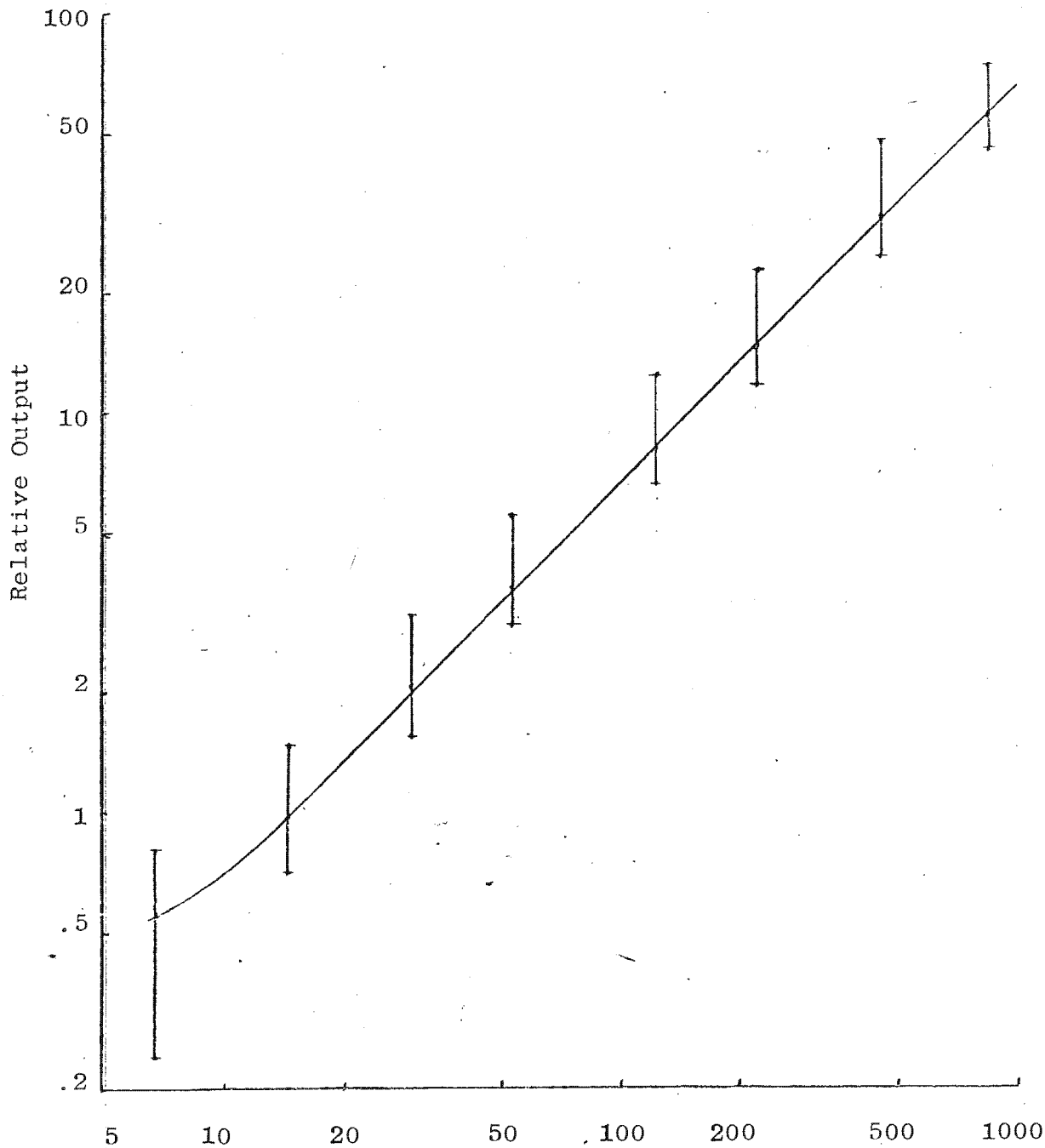


Figure 5

PHOTODIODE TRANSFER CHARACTERISTICS
MEAN AND PEAK DEVIATIONS FOR
CHIP NUMBER 750-21



BYE-8098-70

ATTACHMENT 2

SOLID STATE ARRAY IMAGING TESTS

Reference: [redacted] Report, BIF-165-0701-70

In order to achieve early imaging experience with solid state array transducers, both [redacted] were tasked in October 1969 to develop breadboard transducer devices. Both of these breadboards were delivered in early January 1970 and have subsequently been put through initial imaging testing at the Image Processing Laboratory. The primary purposes of these initial imaging tests were threefold:

a. To verify that the simulation of the arrays in the experimental image chain simulation program is realistic.

b. To demonstrate that the electrical signals generated by the solid state arrays can be geometrically processed into the correct format for image reconstruction.

c. To demonstrate that the signals from the individual photodetectors can be adequately compensated to account for variations in response between detectors.

These tests have now been completed and all three of these objectives have been achieved. The remainder of this attachment summarizes the procedures used to conduct the tests and the test results in the form of actual images.

SUMMARY OF TEST PROCEDURES AND EQUIPMENT

1. Figure 1 is a block diagram depicting the essential functions of the Image Processing Laboratory. The Image Processing Laboratory equipment performs two separate functions. First, the

imaging section of the Image Processing Laboratory equipment is concerned with generating a realistic simulation of real world scenes and projecting these onto the solid state array breadboards. This is a critical operation where great care has been taken to provide adequate control and calibration so as to insure that the test conditions are representative of realistic operational conditions. The second major portion of the Image Processing Laboratory is the data processing and image reconstruction equipments. The solid state array breadboards generate an output digital data stream. The Image Processing Laboratory records this data stream, performs the necessary data processing and reconstructs hard-copy output images. There has been no attempt in this area to actually simulate all of the functions of an operational EOI Processing Facility. Only those essential manipulations have been performed so that good quality, representatives images can be reconstructed. The image chain simulation experiments have shown that there are additional processing techniques which can be applied to the image data before image reconstruction which significantly improve the quality of the imagery.

2. The image projected onto the solid state arrays is generated using a high quality transparency. This input imagery is obtained under specially controlled acquisition and processing conditions. The general procedure is identical to that which has been used for the past eighteen months in the image chain simulation experiments. The light sources used to illuminate the imagery in the Image Processing Laboratory have been carefully calibrated to assure both uniformity of illumination and accurate simulation of real brightness levels. The transparency simulating the real scene is projected onto the breadboard arrays at a scale equivalent to one sample for each foot along the ground. The transfer function of the transparency plus that of the projecting optics also approximate the expected transfer function of the baseline system optics. The control of simulated ground scene brightness, scale factor, and transfer functions is such that the overall image quality of the resulting pictures should be generally representative of that to be expected from an operational system.

3. The characteristics of the breadboard arrays are described in Table 1. Each breadboard contains one sensor chip--in the case [redacted] this chip consists of [redacted] while in the case of

[redacted] there are [redacted] detectors on the chip. Integration times and readout sample times used for breadboard operations are identical to those planned for an operational system. The [redacted] detector chip can be operated in two modes--one, the older optically biased mode and, two, the newer electrically initialized mode. However, the electronics with the breadboard did not permit operation in the electrically initialized mode; therefore, the test images were done with the optical biasing technique. This technique is workable, but in general leads to poorer array performance than the electrical technique. These performance diferences do not have a serious impact on the Image Processing Laboratory testing; however, both the Westinghouse and the [redacted] breadboards processed the output electrical signals into a single serial bit stream with appropriate timing and synchronization bits added.

4. In order to provide a direct one-to-one comparison between the images derived from the image chain simulation program and from the Image Processing Laboratory using real breadboard transducers, the same input images were used in both programs to generate two sets of test images. The objective of this approach was to permit a direct qualitative comparison between the simulation which models the array performance, and imagery generated with actual array hardware. The results of this comparison and representative pictures will be discussed in the next section of this Attachment.

IMAGING TEST RESULTS

1. A complete report on the imaging tests conducted to date is contained in the referenced [redacted] document. The essential conclusions of this test program, however, can be readily deduced from inspection of Figures 2, 3, and 4. The pictures in Figures 2 and 3 were obtained using the [redacted] breadboard and the [redacted] breadboard respectively in the Image Processing Laboratory setup. The separate strips in these figures each correspond to one scan of the breadboard array over the projected ground scene. In an operational system, a total array will consist of multiple chips, and there will be no discernible gaps in the reconstructed image. The picture in Figure 4 was obtained using the same ground scene processed through the image chain simulation system. The qualitative

identity between the image chain simulation picture and the two pictures obtained using the breadboard arrays shows directly that not only is the image chain simulation a reasonable representation of the actual hardware, but also that the electrical signals derived from the breadboard hardware can be reconstructed into good quality images having all of the expected characteristics.

2. The comparability of subjective image quality between the two breadboard-derived images and the simulated image shows that the transfer function characteristics of the real breadboard arrays closely correspond to the transfer function computed from measuring array characteristics and simulating this transfer function in the image chain simulator. The transfer functions of the individual detectors in both breadboard devices were not designed for the optimum overall performance condition. However, this off-optimum condition has had no substantial effect on the subjective quality of the generated images.

3. The response curves of the individual detectors for the two breadboards are shown in Figures 5 and 6. All detectors on the Westinghouse breadboard were well behaved and therefore adequately handled in the simple calibration process used in the Image Processing Laboratory software. However, the [redacted] breadboard had two detectors with extremely low response and two others substantially lower than the remaining 121. The solid state device used in the breadboard came from an October 1969 production run and by current standards would be considered a reject. The two lowest performing detectors can be seen as streaks in the Figure 2 imagery. The two other low performance detectors can also be detected by careful inspection.

4. The photodiode breadboard imagery of Figure 3 shows only one imaging anomaly. The Image Processing Laboratory testing shows that some of the circuitry on the same chip with the photodiodes was also photosensitive. This effect can be seen most clearly by inspection of the edge of the warehouse in the lower lefthand corner. The final chip design has a metallization layer which will completely mask all of the chip circuitry except the photosensitive diode, thus eliminating this effect.

5. The geometric reformatting process necessary in reordering the sample data from both the photodiode and phototransistor arrays must be handled with a high degree of precision. Inspection of the imagery derived from the array testing shows quite clearly that this reformatting process was controlled to a sufficient level of accuracy; even a small amount of error would have shown up as a distortion of objects in the reconstructed ground scene.

6. The reconstructed imagery shown in this Attachment is printed at a relatively large scale of 1:850. (This was intentionally done to permit a detailed inspection of the effectiveness of the reconstruction process.) Consequently, image structure on the order of an individual sample size is evident to the unaided eye. As an example, note the sawtooth structure appearing at the object edges in the array derived imagery. This anomalous structuring is due to the current lack of fine control in the reconstruction spot shape and positioning in the Image Processing Laboratory equipment and is not inherent to the operation of the chip devices. Inspection of the simulation imagery demonstrates the effectiveness of spot shape control on improved image quality performance. Work is now being initiated at the Image Processing Laboratory to upgrade these functions in the image write-out equipment.

7. In general, the initial imaging tests using the breadboard arrays have been successful in demonstrating the feasibility of reconstructing high quality imagery from solid state devices having characteristics useful for the Electro Optical Imaging Program. The subjective quality of the imagery is very good by current standards of satellite photography. Furthermore, the image quality from an operational system using devices of this type tested in the Image Processing Laboratory will in general be qualitatively better as more sophisticated processing techniques are brought into use.

FIGURE 1

IMAGE PROCESSING LABORATORY BLOCK DIAGRAM

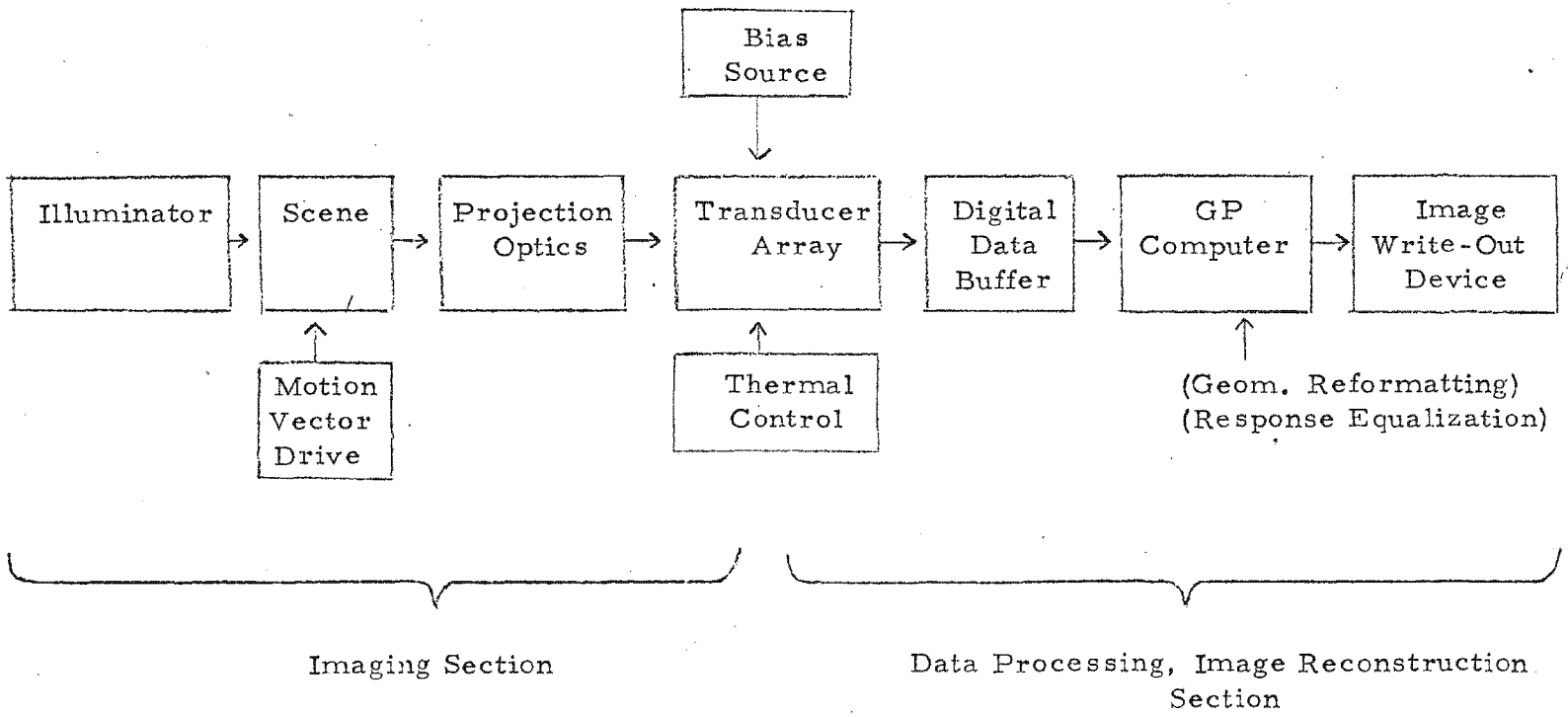


TABLE 1

BREADBOARD ARRAY CHARACTERISTICS

CHARACTERISTIC		
DETECTOR SPACING	0.6 MIL	0.9 MIL
NUMBER OF DETECTORS		
DATA ENCODING	12 BITS	10 BITS
INTEGRATION TIME	1 MILLISEC	1 MILLISEC

BYE-8098-70

ATTACHMENT 3

ENGINEERING DEVELOPMENT PROGRAMS

This Attachment contains a summary of the subsystem engineering development programs now being funded. All of these programs are on schedule and meeting all established requirements and demonstration objectives.

OPTICS

1. [redacted] is proceeding on a 16 month contract, September 1969 through December 1970, working in the following three areas: analysis and system performance; detailed design of two configurations; and fabrication and testing of full size primary and secondary mirrors.

2. After a review of various systems, [redacted] selected a [redacted] configuration and has completed detailed analyses and performance calculations. These studies have covered the range of [redacted] for the primary surface in an [redacted] system. Heterochromatic MTF's have been calculated as well as detailed estimates of OQF, obscuration and error budgets for tilt, decenter, and defocus.

3. Detailed designs of a flat field and a curved field [redacted] are well under way. Both configurations have been laid out and optical designs completed including definition of field lens requirements. Performance gains with the curved field look attractive and work will be continued to verify present estimates. Structural and thermal design details will be refined, and layouts will be carried to the subsystem level to identify requirements and to provide firm values for use in vehicle system studies.

4. The fabrication and test program is progressing very well. The [redacted] diameter Hindle sphere has been polished to .051 λ rms and the primary null corrector, to be used for testing purposes, to .016 λ rms. [redacted] solid Cervit primary and the

[redacted] ULE lightweight secondary have completed rough grind and are now being aspherized. The present schedule calls for delivery of the [redacted] lightweight ULE blank to [redacted] on 30 March 1970. Preparation of all test installations is on schedule, and checkout will be conducted as planned.

RF COMPONENTS

1. Design, fabrication and test programs are under way for: a nominal 30 watt [redacted] Travelling Wave Tube; a TWT cathode reliability program; and a [redacted] parabolic antenna.

2. The design of the TWT is complete, and fabrication is well along with completion scheduled in March 1970. A detailed test program is planned utilizing breadboard components to operate the tube at design power levels over the range of [redacted]

3. The cathode reliability program is just being initiated. A vendor survey is planned with emphasis on capability to fabricate impregnated tungsten cathodes with rigid process controls and thorough documentation. After selection of the vendor, multiple units will be put in test. Part of the testing will emphasize long-term operation at rated power or cathode current loading and part will be devoted to operating cathodes at very high current densities to evaluate life at extreme conditions.

4. The analysis, material selection, and design work for a [redacted] antenna are under way. It is planned that the antenna will be tested in June to demonstrate performance at ambient conditions using breadboard feeds, breadboard receivers and transmitters. Thermal testing will be conducted to determine surface deformations.

5. A SAMSO RF component program is under way to support the data relay satellite requirements. Several of these components, such as the receiver-exciter, are also potentially useful in the imaging satellite. The following development tasks are being closely coordinated by OSP and SAMSO:

[redacted]

a. A composite [redacted] diameter epoxy/fiber reflector with dual mono-pulse feeds for [redacted] and diplexer with a net gain of 60 db is being developed to operate in a space environment at a selected frequency within the [redacted] band. A metal reflector with the same characteristics as above is also being developed.

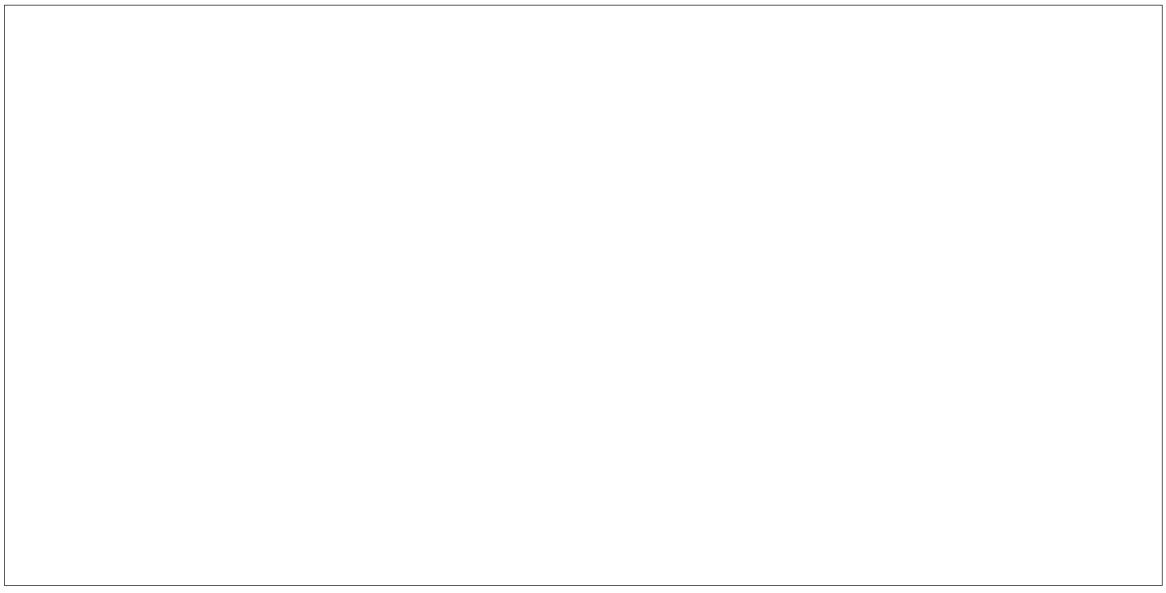
b. Receivers and drivers with 10 db noise figure, capable of accepting quadri-phase PSK signals from the antenna diplexer and driving a Travelling Wave Tube amplifier are being developed. The input and output for each is to be capable of operating at any one of three frequencies within the [redacted] band. One receiver driver will utilize a frequency translation technique and the other a demodulation/remodulation technique.

c. A 3 watt and a 75 watt Travelling Wave Tube are being developed for a 50,000 hour life requirement at a frequency selectable within the [redacted] range. This task also includes the development of associated power supplies and filters.

d. A Parametric Amplifier front end with a 6 db noise figure and a 17 db gain is being developed for use at a frequency within the [redacted] range. This amplifier provides an alternative solution to low noise receiver front end.

FLIGHT COMPUTER

1. A fabrication and test program, funded through SAFSP, is in process for three flight-type computers capable of performing the computation tasks for the attitude control system. These engineering models are to demonstrate the feasibility of modular, high density plated wire memory and LSI switching circuits. The design goals include low weight, volume, and power and relatively high speed arithmetic capability. Plans include delivery of one unit in September 1970 to the control moment gyro contractor for test with actual ACS hardware.



DIGITAL TAPE RECORDER

1. An analysis, design, and breadboard fabrication program for development of a high data rate digital tape recorder has been initiated. A minimum rate of 40 MBS per channel has been selected as an initial requirement although higher speeds are desirable. The initial work is emphasizing a thorough analysis of the interface with the data processor and examination of modem alternatives in order to pursue the method with the highest probability of success. After the analysis, design of a breadboard system, applicable to both flight and ground requirements, will be initiated. A rotary head, magnetic tape system will be utilized. Following completion of the breadboard, testing will be conducted to demonstrate performance characteristics.

2. A firm decision has not yet been made on whether or not an image data recorder will be included in the imaging satellite design. This decision depends largely on communications reliability considerations and relay satellite network selection.

ATTACHMENT 4

SUPPLEMENTARY FY 70 FUNDING

ALTERNATIVES

1. Progress in the overall Electro Optical Imaging Program has now reached a point where continued uniform program development requires additional funding both for accelerated technology activities and for related systems level design activities. Two FY 70 supplementary funding plans have been developed.

2. Option A at an FY 70 cost of [redacted] dollars is a maximum effort option leading to the earliest possible availability of an operational system. Option A requires the addition of approximately [redacted] dollars to the FY 71 Readout Program over and above monies currently budgeted.

3. Option B is a more measured option which assumes that the FY 71 budget will remain as currently planned. The FY 70 funding supplement under Option B is [redacted] dollars supporting design studies.

4. This attachment discusses the overall program plan structure and reviews the probable impact of selection of Option A or Option B on program schedule. The program content of Options A and B is reviewed along with an assessment of the probable impact of a decision not to supplement the FY 70 Readout Program budget.

PROGRAM PLAN STRUCTURE

1. The Electro Optical Imaging Program is structured into three major phases. The program is currently in the first of these phases, the Technology Phase, which is predominantly technology development and studies. The next program phase is the System

[redacted]

Definition Phase. This phase has been further subdivided into a Phase I System Definition and a Phase II System Definition. Following System Definition is the System Acquisition Phase. These program phases and their planned duration are summarized in Table 1.

2. The Technology Phase overlaps with the System Definition Phase. The Technology Phase continues until the System Acquisition Phase is initiated. Phase I System Definition is a broadbased system level design study activity intended to lay the ground work for the competitive phase of the program. During this phase, four parallel design studies will be carried forward for the imaging satellite and three parallel design studies for the processing facility. Based on the results of the Phase I studies, an overall system configuration will be selected as a basis for Phase II System Definition.

3. Phase II System Definition is the competitive phase of the program. Two contractors will be selected for the imaging satellite competition and two contractors for the processing facility competition. Both contractors in each area will start with the same overall system configuration and design requirements. The contractors will proceed into detailed design and based upon these detailed design activities will develop detailed program plans for the System Acquisition Phase and associated cost proposals.

4. After the final selection of one contractor for the imaging satellite and one contractor for the processing facility, the System Acquisition Phase can be initiated. At the start of System Acquisition, the selected contractors will have proceeded well into system design and should be within three to six months of the Preliminary Design Review (PDR) milestone.

5. Table 2 summarizes the major program events for Options A and B. The Option A FY 70 funding level supplement is [redacted] dollars. This is sufficient to support the initiation of Phase I System Definition immediately. The lower level of funding under Option B and the subsequent lower funding level requirements of FY 71 postpone the initiation of Phase I System Definition until at least July 1970. In either case, the dates in Table 2 are the earliest feasible dates given appropriate program approvals and funding levels.

[redacted]

(10)

OPTION A PROGRAM PLAN

1. The allocation of the [redacted] dollars of FY 70 supplemental funding under Option A is shown in Table 3. If the overall program proceeds directly into Phase II System Definition and subsequently into System Acquisition according to the schedule outlined in Table 2, the FY 71 - 74 funding requirements are summarized under the Option A listing in Table 4.

2. Under Option A, [redacted] dollars of the FY 70 supplemental funding will be allocated to four parallel System Definition studies for the imaging satellite. [redacted] dollars will be allocated for three similar processing facility studies. These studies will serve the dual purpose of providing required inputs for selection of the overall system configuration and developing a mature contractor base for the competitive Phase II System Definition activity.

3. The solid state array transducer development programs as currently structured are focused on the fabrication and testing of the individual detector devices. [redacted] dollars is allocated towards augmenting the two solid state array development programs to include engineering design studies. Design studies will explore alternative solid state transducer mechanical and electrical design layouts for application in the Electro Optical Imaging Program context. In addition, the two contractors will study the associated data processor design requirements and develop hardware designs to implement these requirements. The level of technology required for these devices has been proven feasible. Subsequent program progress will be significantly impaired unless these design studies can be initiated at this time.

4. Currently, a [redacted] RF power tube breadboard is under development as is a [redacted] antenna for the data communications subsystem. The program schedule implied by the election of Option A requires that the RF component technology programs be further expanded. Specifically, a power supply for the [redacted] RF amplifier must be put into development, [redacted] antenna tracking studies and

breadboard development must be initiated, and exciter/ modulator breadboarding must begin. dollars is allocated to these development efforts. This program has been planned in close coordination with SAMSO.

5. The critical new development in the imaging satellite A substantial program is already under way in this subsystem area; however, an expansion of this development program is required if a March 1971 System Acquisition start is desired. dollars is allocated towards expanding the current program and broadening the competitive base in this subsystem area.

OPTION B SUPPLEMENTARY FUNDING PROGRAM PLAN

1. The allocation of the dollars of FY 70 supplemental funding under Option B is shown in Table 3. Option B is structured with the assumption that the currently budgeted FY 71 funds for the Readout Program will not be increased. The FY 71 - 74 funding requirements for Option B are listed in Table 4.

2. Under Option B, the Phase I System Definition activity does not start until FY 71. Therefore, the system design studies for both the imaging satellite and the processing facility will not be carried forward on a parallel basis at multiple contractors. Rather, the limited funds under Option B will be focused so as to obtain the maximum systems level visibility in both systems areas.

3. As under Option A, the Option B plan calls for supplementing the solid state array development programs by dollars. The allocation of the dollars will be the same as in Option A. As discussed above, these funds are critical to continued progress in this development area. Since Option B delays the start of System Acquisition until at least August 1971, subsystem development work in both the RF components area and the area is less schedule critical; however, dollars is allocated for the antenna tracking studies and exciter/modulator design studies.

4. The system design studies under Option B for both the imaging satellite and the processing facility will provide a far more comprehensive development of the overall system configuration than has been available to date. In addition, these design studies will develop alternative design approaches in critical subsystem areas and provide further confidence that the critical subsystem technologies have been correctly identified in the supporting technology programs.

PROGRAM IMPACT OF NO FY 70 SUPPLEMENTARY FUNDING

1. The most serious impact of no FY 70 supplementary funding will be the inhibition of detailed system design studies. All of the critical component and subsystem technology has now been proven. The remaining questions are at the systems level, and little additional progress can be made without a direct attack at this level.

2. Detailed system design studies are also needed to develop comprehensive system configuration options and associated performance tradeoff information. Without a thorough background of information of these types, further policy level program direction will suffer for lack of adequate support.

3. A further consequence of the disapproval of FY 70 supplementary funding will be an overall inhibition of the continued logical evolution of the various technology programs. This will be particularly so in the case of the solid state array transducers where both more funding and system level design inputs are judged to be critical. Further systems level visibility is imperative for the most efficient management of all subsystem technology efforts.

4. The overall schedule impact of no further FY 70 funding will depend largely on subsequent program decisions. The March 1971 System Acquisition start under Option A funding could not be met under any circumstance without the required FY 70 supplementary approval. The August 1971 System Acquisition start under Option B could in principle be protected by initiating Phase I System Definition at the beginning of FY 71 (July 1970). However, if no supplementary funding is approved now, the information

available in June 1970 to support a decision to start Phase I System Definition in July 1970 will be qualitatively no different than that available now. Postponement of Phase I System Definition beyond July 1970 will result in a slip of the system initial operational capability date beyond August 1974.

TABLE 1

ELECTRO OPTICAL IMAGING PROGRAM

PLAN STRUCTURE

Program Phase	Duration
Technology and Studies	Until System Acquisition Starts
System Definition	
Phase I	4 months
Review and Evaluation	1 month
Phase II	6 months
Review and Evaluation	2 months
System Acquisition	37 months

TABLE 2

MAJOR PROGRAM EVENTS
(Dates are Earliest Feasible)

	Option A	Option B
Start System Definition		
Phase I	March 1970	July 1970
Phase II (Competitive)	July 1970	November 1970
Start System Acquisition	March 1971	August 1971
System Operational	April 1974	August 1974

TABLE 3

SUPPLEMENTARY FY 70

FUNDING ALLOCATION

	$ Thousands Option A	Option B
IMAGING SATELLITE		
Phase I System Definition		
System Design Studies		
Solid State Transducers		
Optics		
Digital Tape Recorder		
RF Components		
[redacted]		
Computer		
PROCESSING FACILITY		
Phase I System Definition		
System Design Studies		
IMAGE CHAIN PERFORMANCE DEFINITION		
Image Chain Simulation	-----	-----
Image Processing Lab	-----	-----
TECHNICAL CONSULTANTS	-----	-----
	[redacted]	

Attachment 4 to
BYE-8098-70
Page Nine

TABLE 4

SUBSEQUENT YEAR FUNDING REQUIREMENT
($ Millions)

	FY 71	FY 72	FY 73	FY 74	FY 75	TOTAL
Option A						
Option B						

Note: These estimates are exclusive of all launch vehicle and relay satellite costs.