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**QUARTERLY TECHNICAL PROGRESS REPORT**

**DUAL STRIP  
CAMERA BACK STUDY**

**PHASE IV**

22 NOVEMBER 1968

DEC 10 1968



**OPTICAL SYSTEMS DIVISION**

ITEK CORPORATION • 10 MAGUIRE ROAD • LEXINGTON, MASSACHUSETTS 02173

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#### ABSTRACT

The work to be accomplished during this, the Phase IV, period is to:

1. Fabricate and test the along- and cross-track sensor and servo brassboard.
2. Perform an investigation of focus sensor techniques, fabricate breadboards, and develop a composite focus sensor and servo for use with a moving image.
3. Design, fabricate, and test a cylindrical optics system which will be compatible with a maximum slit width of 2.3 inches and produce no "bias" magnification.

The following paragraphs summarize the work accomplished in the Phase IV period:

Along-Track Sensor/Servo. Optical/mechanical fabrication and assembly of the multichannel brassboard are complete with the exception of the beam splitting plates and the stainless steel aperture belt. Functional test of the signal detection and processing circuits is complete. Using simulated sensor signals, the 9 1/2-inch film drive servo was satisfactorily operated. Initial tests using a moving slit target belt showed encouraging results. The processed signal showed a variation equal to or less than  $\pm 0.02$  percent, 94 percent of the time.

Cross-Track Sensor/Servo. A block diagram for the cross-track control servo has been adopted. Fabrication of the K-mirror support structure and drive is in process. All long lead items have been delivered. The electrical design is in process. Electrical fabrication is expected to be completed by 15 December 1968.

Focus Sensor. Three focus sensing concepts have been adopted. Breadboard design of the three approaches is complete. Fabrication is in process.

Cylindrical Optics. The design effort for the cylinder has concentrated on optimizing a three-element set over the central 1-inch portion of the exposure slit. This design provides excellent performance over this portion of the format in that the proper magnification has been obtained, the bias magnification has been removed, the along-track distortion is zero, and the peak wavefront error is less than 1/4 wave. However, performance is degraded quadratically with field height over the remaining portion of the format. The peak wavefront error at the edges of the 2.3-inch slit width is 1.0 wave. Presently, the optimum design over the full 2.3-inch slit width is being sought. The cylindrical optics test fixture has been designed. The test program will be essentially identical to that conducted with the two-element design in the earlier phases of the program.

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## 1. INTRODUCTION

The Dual Strip Camera Back Development Program, presently conducted under Contract [REDACTED] is a continuation of the work done under Phases I, II, and III of Contract AF18(600)-2961. Theoretical analysis and experimental breadboard studies relating to along- and cross-track image motion sensing and image velocity grading for oblique pointing were carried out. The results of Phases I, II, and III were reported in Itek documents 9416-67-011, 9416-67-022 and 9416-68-026.

The results showed that:

1. A detection system capable of measuring image motion to an accuracy of  $\pm 0.1$  percent (90 percent of the time) at a sampling rate of 66 hz could be realized.
2. A detection system capable of measuring  $\pm 1$ -arc-minute misalignment between a moving image and fixed reference reticles could be realized.
3. Correction of image motion across the field during oblique operating conditions could be realized using cylindrical optics. Analytical and experimental studies have verified their performance.

Concurrent with the above work, system analysis, error budgets, and performance prediction studies were made.

At the conclusion of the Phase III work, the design of a multichannel along- and cross-track sensor brassboard was in process.

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## 2. ALONG- AND CROSS-TRACK SENSORS AND SERVOS

The multichannel brassboard under development is shown in Figs. 2-1, 2-2, and 2-3. A moving target is provided by transporting a 5-inch positive transparency of an aerial scene (containing selected detail and contrast characteristics) past a light source. An 18-inch EFL,  $f/9$ , distortionless, APO-Germinar lens images the moving scene onto a group of five stationary reticles. A dichroic beam splitter and compensator plate and a moving aperture belt are introduced between the reticle and the APO-Germinar lens. The beam splitter provides visible light to the moving 9-inch recording film, and allows the remaining near infrared energy to be used for the sensors.

The aperture belt is driven at approximately the image velocity. It contains groups of five apertures corresponding to the five sensor channels and one aperture for the aperture position detector (Fig. 2-3). The moving apertures serve to reduce phase changes in the frequency of the detected signals. A K mirror provides for rotation of the target scene (hence image) velocity vector for testing the cross-track sensor.

Located behind each reticle are five aspheric condensers which collect the light transmitted by the reticles and image this energy onto five low-noise, high sensitivity photodiodes. Three photodiodes (AT on Fig. 2-2) are used for along-track image velocity sensing. The remaining two photodiodes (CT) are used for sensing rotation of the image velocity vector (cross-track image velocity). A Tele-Pat light source, a pellicle, and a lens simulate haze light. Solid state electronics amplify and process the signals generated by the photodiodes into a form which can be utilized by two servomechanisms which synchronize and align the film velocity vector to the image velocity vector.

### 2.1 ALONG-TRACK SENSOR AND SERVOS

A block diagram of the signal processing electronics is shown in Fig. 2-3. The use of three photodiodes and staggered circular apertures increases the probability of having an acceptable signal level from which measurements can be made. Previous work has shown the SGD-444 photodiode to be the best choice for detecting the optical signal. The signal amplifier design is essentially unchanged from that previously reported, but analysis and test of the SGD-444 and signal amplifier combination is continuing in order to achieve the maximum signal-to-noise ratio. Commercial bandpass filters provide a further noise reduction. Automatic gain control (AGC) circuits present a constant high level signal to the zero crossing detectors (ZCD). The AGC circuits enable the sensor to operate over a wide dynamic range so that strong signals will not saturate the electronics and thereby cause deterioration in the signal-to-noise ratio at the ZCD input. The ZCD detects the positive going crossings of the amplified signal and produces a square wave signal (denoted as  $f_i$ ) for digital processing. Signal selection logic compares the levels of the three photodiode signals (A, B, C) and selects the output of that ZCD circuit corresponding to the largest photodiode signal. Auxiliary aperture position detection diodes detect whenever a circular aperture is just entering (or leaving) the image gate. When this

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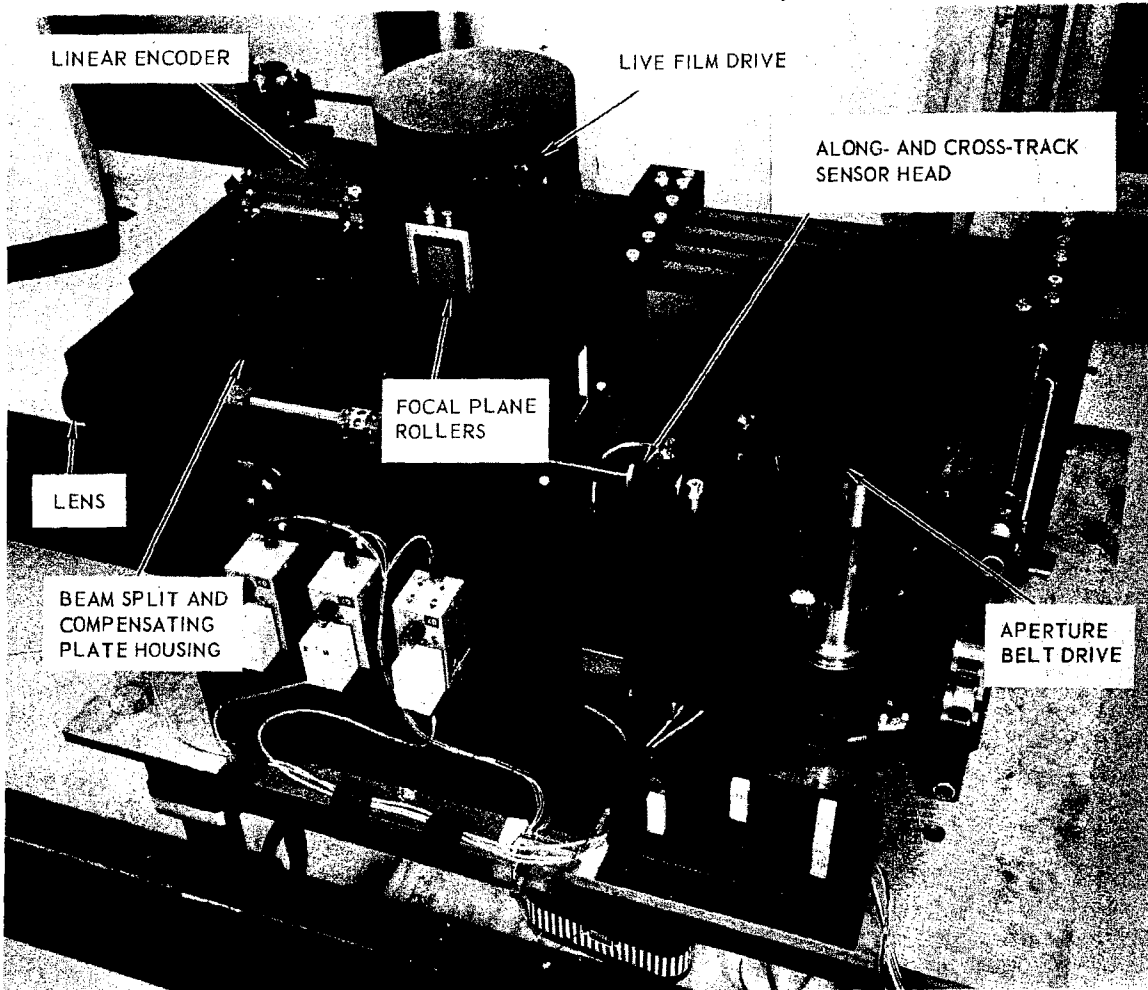
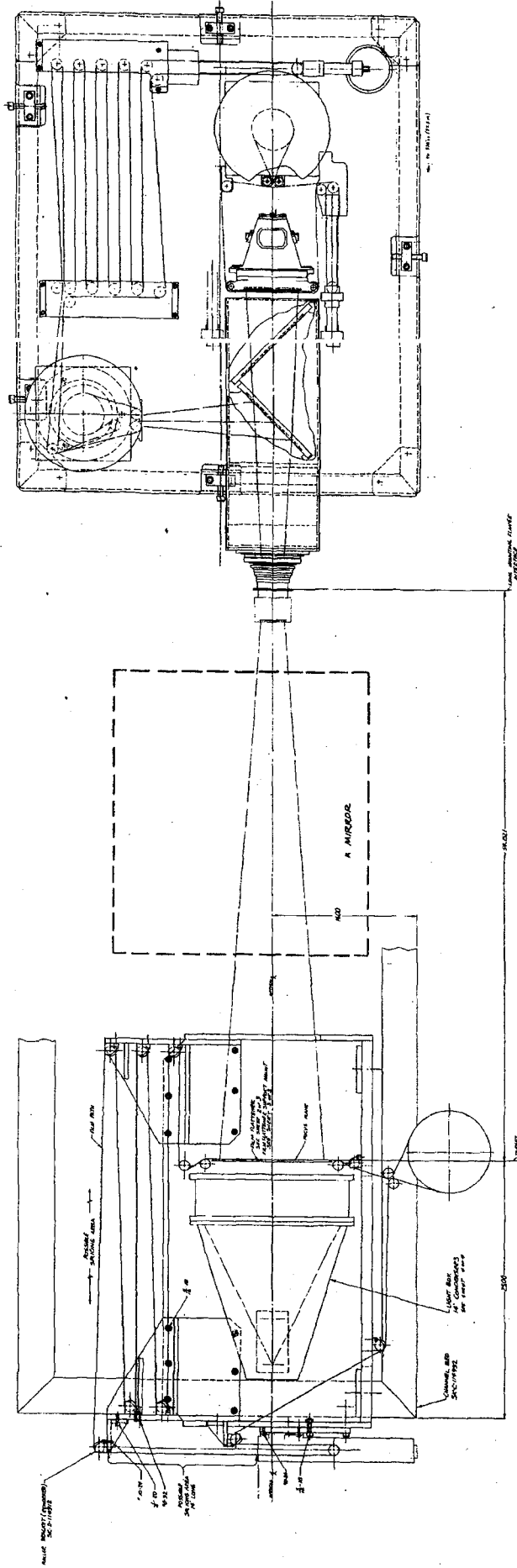


Fig. 2-1 — Multichannel brassboard (left side)

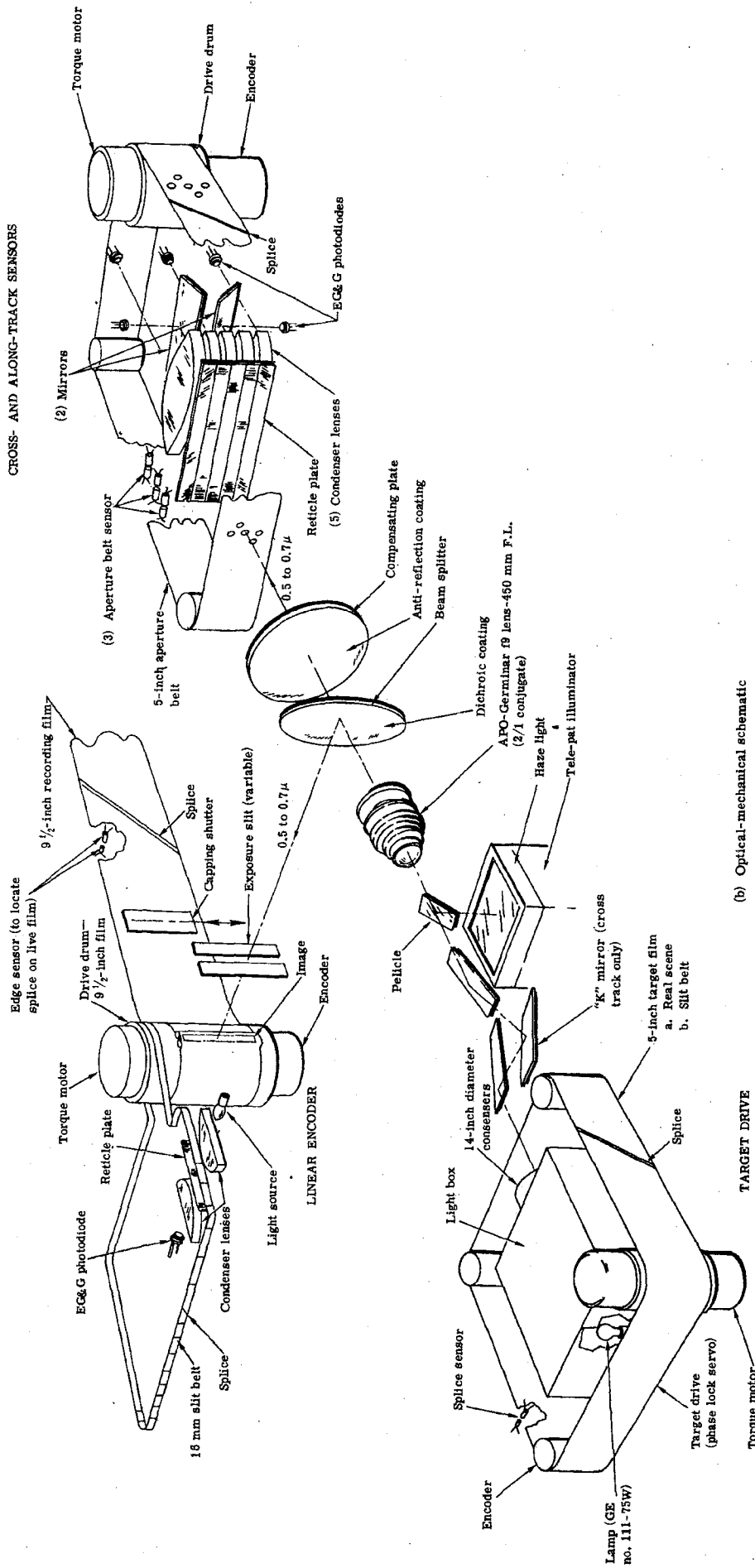


(a) Brassboard design layout

FIG. 2-3 - Multichannel brassboard

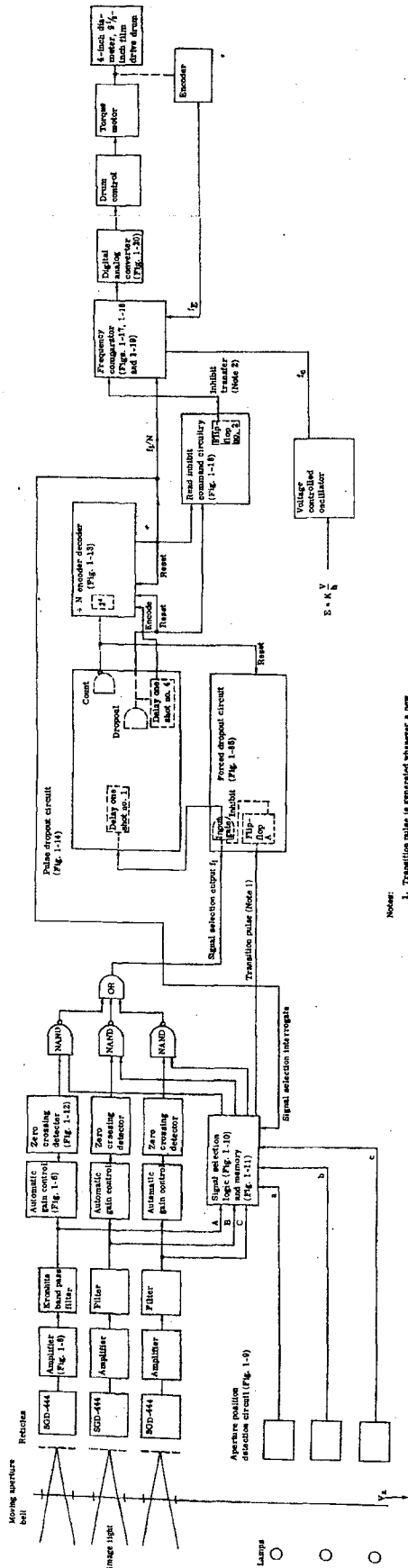


CROSS- AND ALONG-TRACK SENSORS



(b) Optical-mechanical schematic

Fig. 2-2 - Multichannel brassboard (Cont.)



- Notes:
1. Transition pulse is generated whenever a new signal selection is made.
  2. Inhibit transfer pulse is generated whenever a signal selection is made.
- Table above frequency comparator (house 8-inch drive servo) is continue operating on last measurement of  $f_1$ .

Fig. 2-3 — Along-track sensor/servo multichannel brassboard signal processing

occurs, the corresponding signal channel is ignored in the signal selection process. The selected signal is applied to the "signal dropout and divide-by-N" circuit. The optimum value of N depends on the signal-to-noise ratio at the input to the ZCD and for the present is made variable. The counted down or "smoothed" signal,  $f_i/N$ , is next quantized to a resolution of  $\pm 0.01$  percent by the frequency comparator logic circuits. The signal is now in a form suitable for use by the  $9\frac{1}{2}$ -inch film drive control servomechanism. In the event that the signal level is low in all three channels, the ZCD output will be quiescent. The pulse dropout detection logic senses this condition and initiates controls to hold the last quantized signal in the memory within the frequency comparator logic. This memory feature is also employed whenever there is a selection of a new channel. At the time of selection, a transition pulse which inhibits the  $f_i$  signal is generated to simulate a signal dropout.

### 2.1.1 Along-Track Sensor

#### 2.1.1.1 Sensor Signal Generation and Processing

The circuitry used to generate and process the three signals generated by the photodiodes for the along-track sensor is described below.

#### Photodiode Optimum Load Resistance

The detector used in the along-track sensor is the EG&G silicon photodiode (SGD-444). A primary reason for selecting this unit is its low noise characteristics. This cell has very low surface leakage due to the diffused "guard ring" construction. The guard ring allows the surface leakage current to be shunted around the load resistor. Thus, the bulk leakage of the cell, which is normally two orders of magnitude below the surface leakage becomes the limiting dark current. The noise due to dark current is thereby reduced by a factor of 10.

The electrical structure of the photodiode permits the evaluation of a load resistor value which gives a maximum signal-to-noise ratio. A simplified electrical equivalent circuit for the photodiodes is shown in Fig. 2-4.

A current source which is proportional to the incident light level is represented by  $i_g$ .  $R_C$  is the channel resistance which increases with increasing bias. For the 12 volt bias level used, this value of  $R_C$  is approximately 350K ohms.  $R_L$  is the external load resistor whose optimum value is to be determined.

Associated with each of these quantities is an equivalent noise generator. Shot noise associated with the current source is derived from the formula

$$i_{sn} = \sqrt{2e(bw) i_g}$$

where  $e = 1.6 \times 10^{-19}$  coulomb

$bw$  = bandwidth, hz

$i_g$  = diode current, amperes

$i_{sn}$  = shot noise, amperes rms

The resistors contribute Johnson (thermal) noise in accordance with the formula:

$$E_n = \sqrt{4KT R (bw)}$$

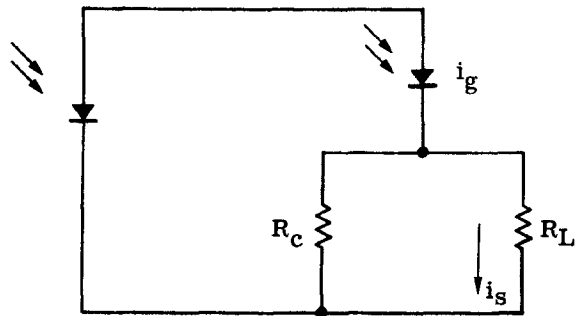


Fig. 2-4 — Simplified electrical equivalent circuit

where  $E_n$  = thermal noise, volts rms  
 $K$  = Boltzman's constant,  $1.38 \times 10^{-23}$  joule/°K  
 $T$  = temperature, °K  
 $R$  = resistance, ohms ( $R_c$  or  $R_L$ )  
 $bw$  = bandwidth, hz

The output signal is the fraction of  $i_g$  which goes through the load resistor,  $R_L$ , i.e.,

$$i_s = \frac{R_c}{R_c + R_L} i_g$$

Consequently, the signal-to-noise ratio,  $i_s/i_n$ , is given by the expression

$$\frac{i_s}{i_n} = \sqrt{2e (bw) i_g + \frac{4KT R_L (bw)}{R_c^2} + \frac{4KT (bw)}{R_c}}$$

The maximum value for the expression will occur when  $R_L$  is set to zero. This approach allows all the photodiode current to flow through the external connection and bypass the channel resistance. As is discussed in the following paragraph, this is accomplished by having the input to the first stage amplifier at virtual ground.

#### Signal Amplifier

Fig. 2-5 shows the electrical schematic of the circuitry for amplifying the photodiode current signal.

The first stage is a Philbrick Model Q25AH high performance differential operational amplifier connected as a current-to-voltage amplifier. In this configuration, the amplifier input is a virtual ground, and the photodiode has the desired zero impedance load, thus permitting the photodiode to operate at maximum signal-to-noise ratio as determined above. The Q25AH amplifier was selected for its low noise characteristics (approximately 1 microvolt of noise at the frequency of interest). Film resistors were used in the first stage to minimize thermal noise.

The second and third stages are Philbrick Model EP55AU differential operational amplifiers. The third stage gain is set to give a reasonable signal level. An automatic gain control following this stage properly adjusts the signal to the desired level.

#### Noise Calculations

The expected theoretical value of the noise from the photodiode circuit is given by the expression:

$$\begin{aligned} i_{nd} &= \sqrt{(\text{shot noise})^2 + (\text{thermal noise})^2} \\ &= \sqrt{2e (bw) i_g + \frac{4KT (bw)}{R_c} + \frac{4KT R_L (bw)}{R_c^2}} \end{aligned}$$

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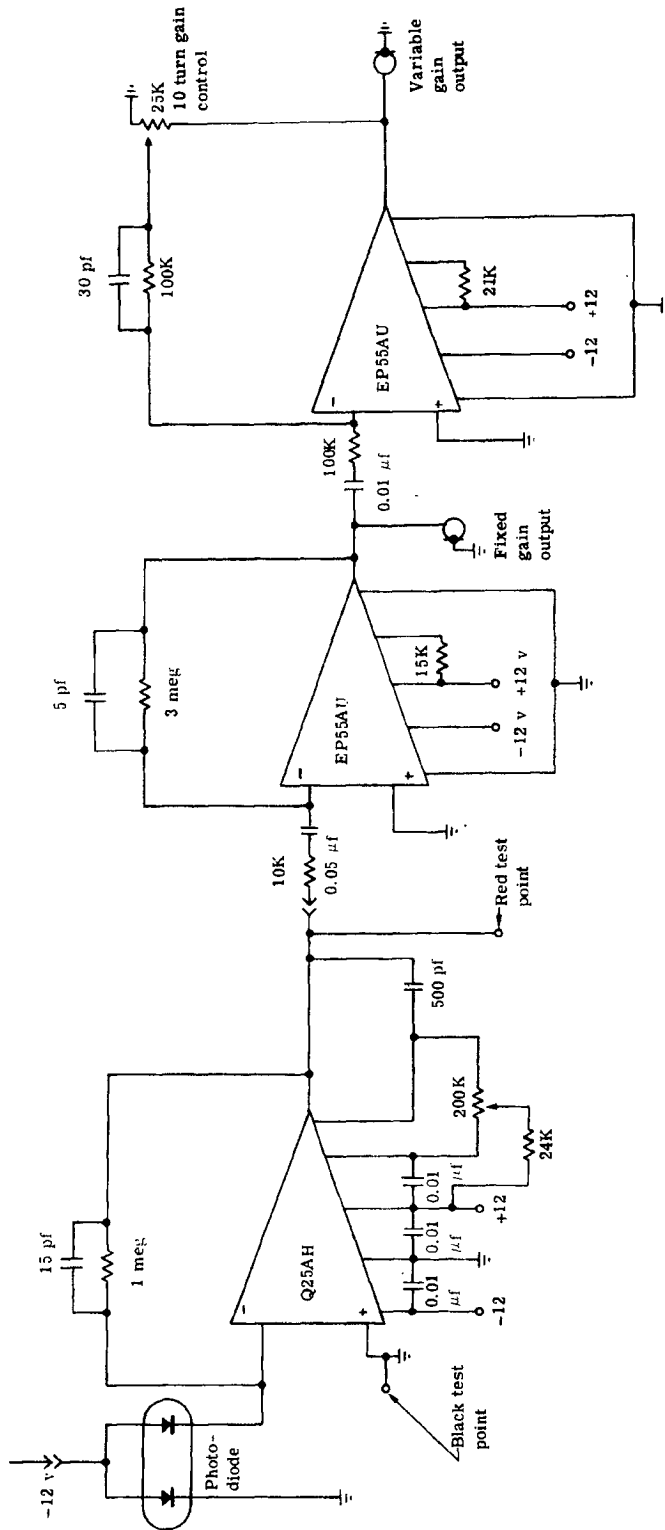


Fig. 2-5 -- Electrical schematic for amplifying photodiode signal

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where  $i_{nd}$  = noise current from photodiode, amperes  
 $e = 1.6 \times 10^{-19}$  coulomb  
 $bw$  = bandwidth, hz  
 $i_g$  = diode current, amperes  
 $K =$  Boltzman's constant,  $1.38 \times 10^{-23}$  joule/°K  
 $R_c$  = channel resistance, ohms  
 $R_L$  = load resistance, ohms

For  $bw = 1,000$  hz  
 $i_g = 1 \times 10^{-6}$  amp  
 $R_c = 350K$  ohms  
 $R_L = 0$  (for maximum signal-to-noise)

$$i_{nd} = \sqrt{2(1.6 \times 10^{-19}) \times 10^3 \times 10^{-6} + \frac{4 \times (1.3 \times 10^{-23}) \times 300 \times 10^3}{3.5 \times 10^5}}$$

$$i_{nd} = \sqrt{(3.2 + 0.47) \times 10^{-22}}$$

$$i_{nd} = 1.9 \times 10^{-11} \text{ amperes}$$

At this light level, the major contribution to the photodiode noise comes from the shot noise rather than the thermal noise. This condition will remain until the light level is reduced by a factor of 7, at which level the thermal noise will start to predominate. (The shot noise from the dark current of the photodiode is an order of magnitude less than the thermal noise and does not enter into these calculations).

The noise voltage on the output of the amplifier equals the diode noise current multiplied by the voltage gain of the system.

$$E_{nd} = K_1 K_2 K_3 i_{nd}$$

where  $E_{nd}$  = noise voltage due to noise current, volts  
 $K_1$  = first stage gain, 1 volt per microampere  
 $K_2$  = second stage gain, 300 volts per volt  
 $K_3$  = filter insertion loss = 6 db = 0.5

$$E_{nd} = 1.5 \times 10^8 \times 1.9 \times 10^{-11}$$

$$E_{nd} = 2.85 \text{ millivolts (theoretical noise value)}$$

An experiment was conducted which measured the noise using a dc light source which produced one microampere of diode current. The measured noise value was 2.87 millivolts, which includes the amplifier electronic noise. By shorting out the input to the amplifier (with the photodiode disconnected), the noise contribution from the amplifier alone was found to be 0.8 millivolts. (The 0.8-millivolt noise results primarily from the amplification of the noise signals inherent in the first stage operational amplifier.) The expression for noise from the diode alone is

$$E_{nd} = \sqrt{(E_n \text{ total})^2 - (E_n \text{ amp})^2}$$

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where  $E_{nd}$  = noise from diode, volts (actual)  
 $E_n$  total = total measure noise from system, volts  
 $E_n$  amp = noise contribution from amplifier alone, volts

For  $E_n$  total = 2.87 mv and  $E_n$  amp = 0.8 mv

$$E_{nd} = \sqrt{8.23 - 0.64}$$

$E_{nd}$  = 2.75 mv (measured noise value) in excellent agreement with the theoretical value of 2.85 millivolts.

#### Automatic Gain Control

The function of the AGC circuits is to prevent a deterioration of the signal-to-noise ratio, at the inputs to the zero crossing detectors, which may occur with a fixed amplifier gain and wide fluctuations in signal levels. The AGC circuit, shown in Fig. 2-6, provides a constant, low distortion signal to the ZCD. Its function is provided by a voltage controlled resistance element in series with operational amplifier A1. Field effect transistors, Q1 and Q2, provide this variable resistance,  $R_v$ , as a function of the applied gate bias voltage. The output signal is given by

$$E_{out} = \frac{R_F}{R_v} E_{in}$$

Operational amplifier A2 is arranged to rectify the output signal to yield a proportional voltage ( $E_0$ ) dc. This rectified voltage is summed with a reference voltage,  $E_{ref}$ , by operational amplifier A3 whose output is applied to the gates of Q1 and Q2, thereby closing the AGC control loop. For an increase in input signal, the output will initially increase. This increase is summed with the reference voltage to cause the output of A3 to decrease, which in turn causes the combined resistance,  $R_v$ , of Q1 and Q2 to increase. For high loop gain, the steady state output voltage will remain constant and proportional to  $E_{ref}$ . Amplifier A3 is arranged as an integrator to provide high loop gain at low modulating frequencies. Integrator A3 also maintains a stable AGC loop by virtue of its decreasing gain versus frequency characteristics.

Fig. 2-7 shows the measured transfer characteristic of the AGC circuit.

Operational amplifier A4 is arranged to amplify and rectify the input signal. This rectified signal is applied to the signal selection logic circuits.

#### Signal Selection Logic

The function of the signal selection logic is to compare the three amplified photodiode signals in channels A, B, and C, and to pass the largest of the three to the signal dropout and divide-by-N circuits as pulses. When one of the three apertures is in transition, a comparison of the remaining two channels is made.

A drawing of the signal selection logic is shown in Fig. 2-8.

The various components of the signal selection logic and their function are discussed below.

##### 1. Signal Rectifiers

There are three signal rectifiers, one for each channel. The rectifiers convert the circular aperture signals to positive voltage levels.

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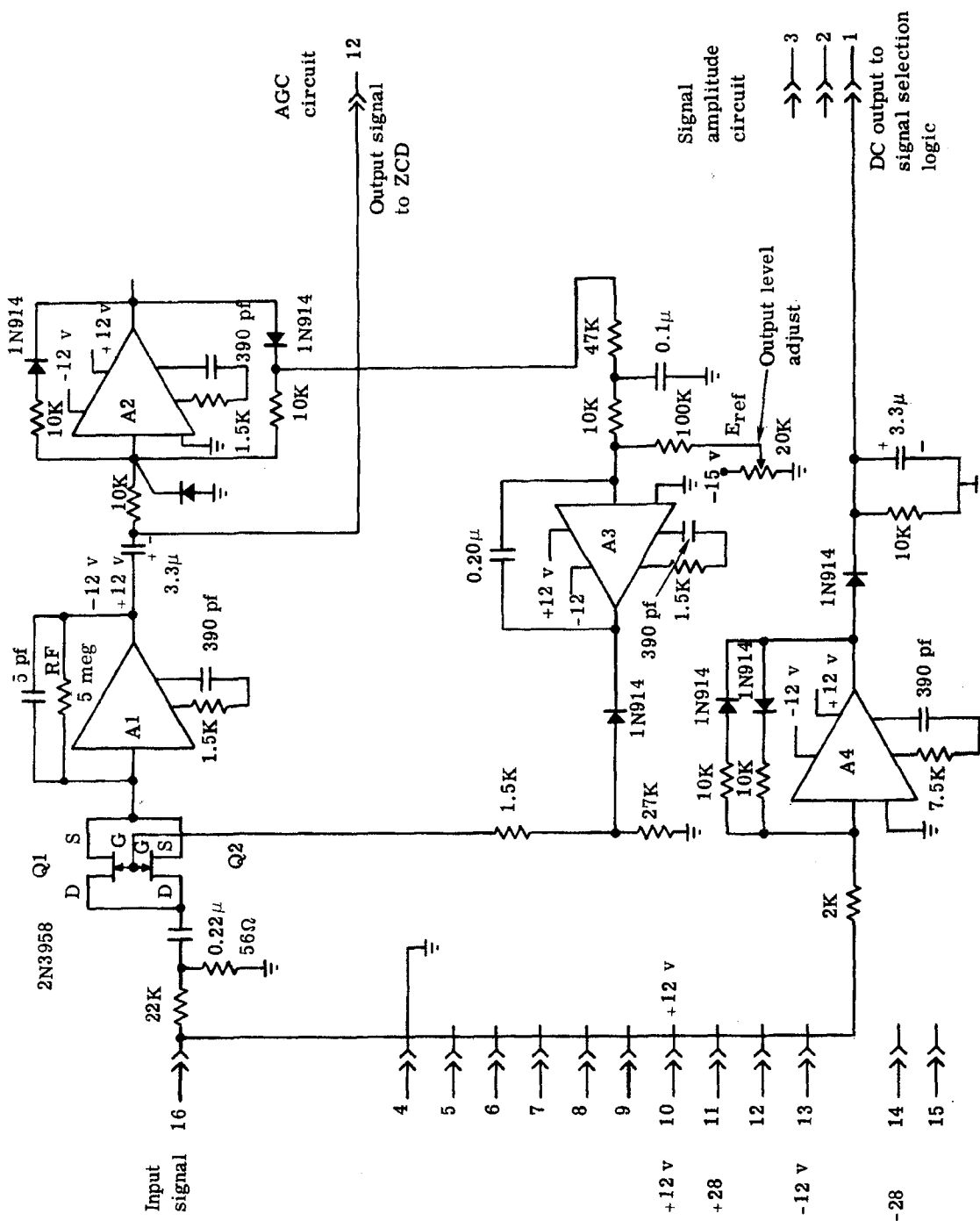


Fig. 2-6 — AGC circuit

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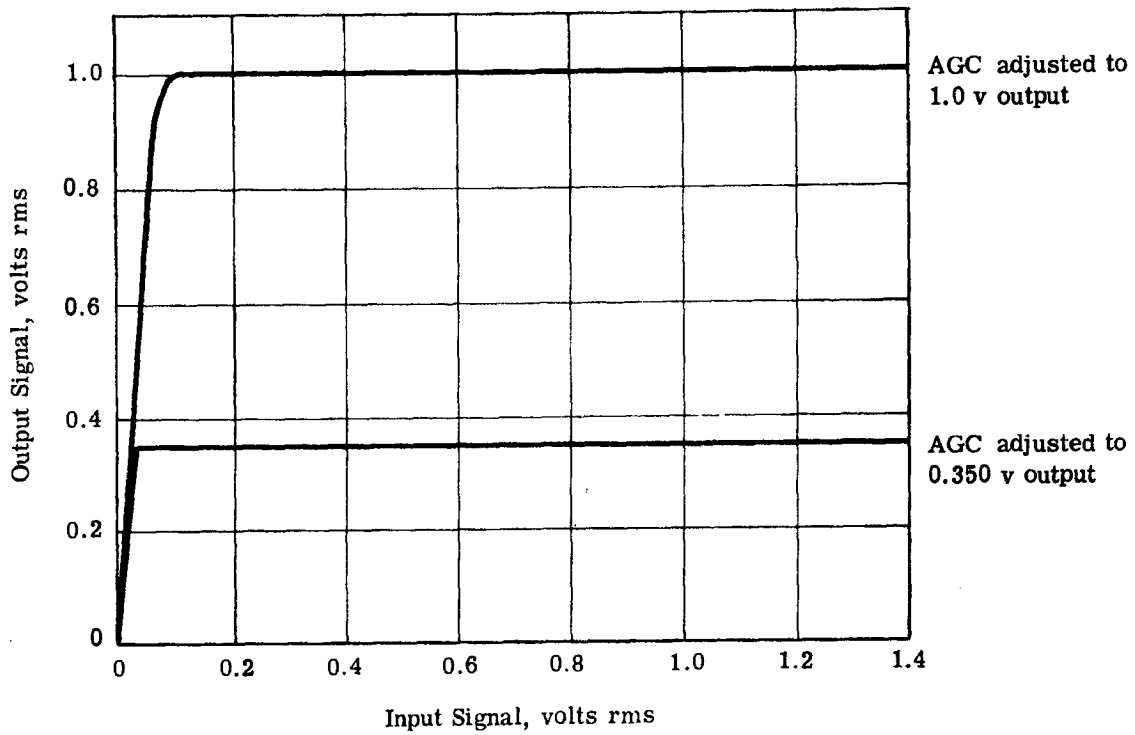


Fig. 2-7 — Transfer characteristics of AGC circuit

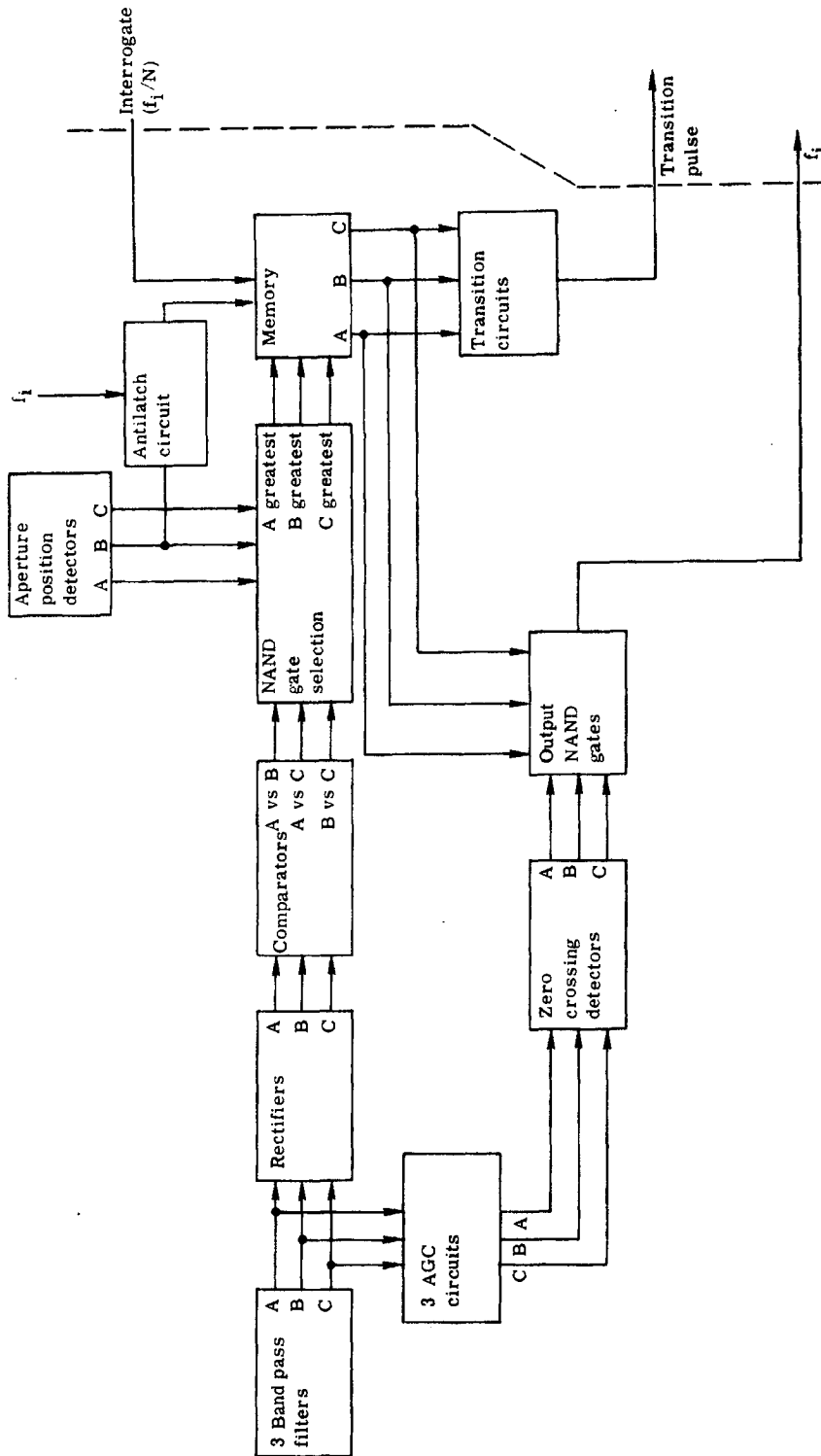


Fig. 2-8 — Signal selection logic

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## 2. Comparators

Each of the three comparators compares the outputs of two rectifiers and produces at its output either a logic level zero ( $LL_0$ ) which is zero volts or a logic level one ( $LL_1$ ) which is +6 vdc (i.e., if the dc level of channel A is larger than that of channel B, comparator A versus B will have an  $LL_1$  at its output; if the dc level of channel B is larger than that of Channel A, comparator A versus B will have an  $LL_0$  at its output).

## 3. Aperture Position Detectors and NAND Gate Selection

Fig. 2-9 shows the aperture position circuit. This circuit is simply a photodetector/transistor switch which produces an  $LL_0$  when light impinges on the photodiode and an  $LL_1$  when no light is on the photodiode. The output, then, indicates when one of the circular apertures is in transition within the image gate.

When all three circular apertures are within the image gate, the outputs of all three aperture position detectors are at  $LL_1$ . The NAND selection logic examines the three comparator outputs and the three aperture position detector outputs and provides output control lines to each of three memory flip-flops. These control lines are designated as A greatest, B greatest, and C greatest as shown in Figs. 2-8 and 2-10.

## 4. Memory

Three JK flip-flops make up the memory. The set output will be at  $LL_1$  when the set control input is at an  $LL_1$ , the reset control input is at an  $LL_0$ , and a pulse is applied to the clock terminal. The flip-flop will change state if the JK inputs (set control and reset control inputs) change state and the clock pulse arrives. The various logic states of the memory flip-flops are shown in Fig. 2-11.

Since only one of the control lines (A greatest, B greatest, C greatest) can be at  $LL_0$  at any given time, only one of the flip-flops can have an output of  $LL_1$ .

## 5. Zero Crossing Detectors

There are three identical zero crossing detectors which are of the Schmitt Trigger class.

The functions of the zero crossing detector are (1) to detect positive-going zero crossings of the AGC output, and (2) to produce a signal which is compatible with logic circuits, i.e., in this case  $LL_0$  to  $LL_1$  pulses.

Adjustments for trigger level and hysteresis are provided and are labelled in Fig. 2-12.

## 6. Output NAND Gates

These gates logically select the proper ZCD output corresponding to the largest signal to be transmitted as logic pulses to the next subsystem, namely the signal dropout detection and divide-by-N logic.

## 7. Transition Circuits

When one of the memory flip-flops changes state, one of three monostable multivibrators is triggered to produce a 1-microsecond pulse. This transition pulse is fed to the signal dropout detection divide-by-N logic which is discussed later in this report.

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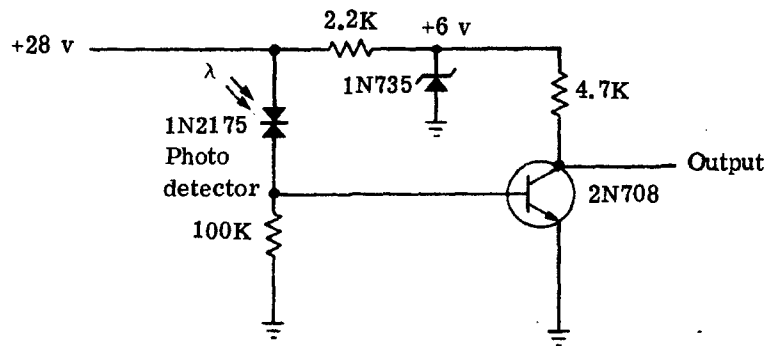


Fig. 2-9 — Aperture position detector circuit

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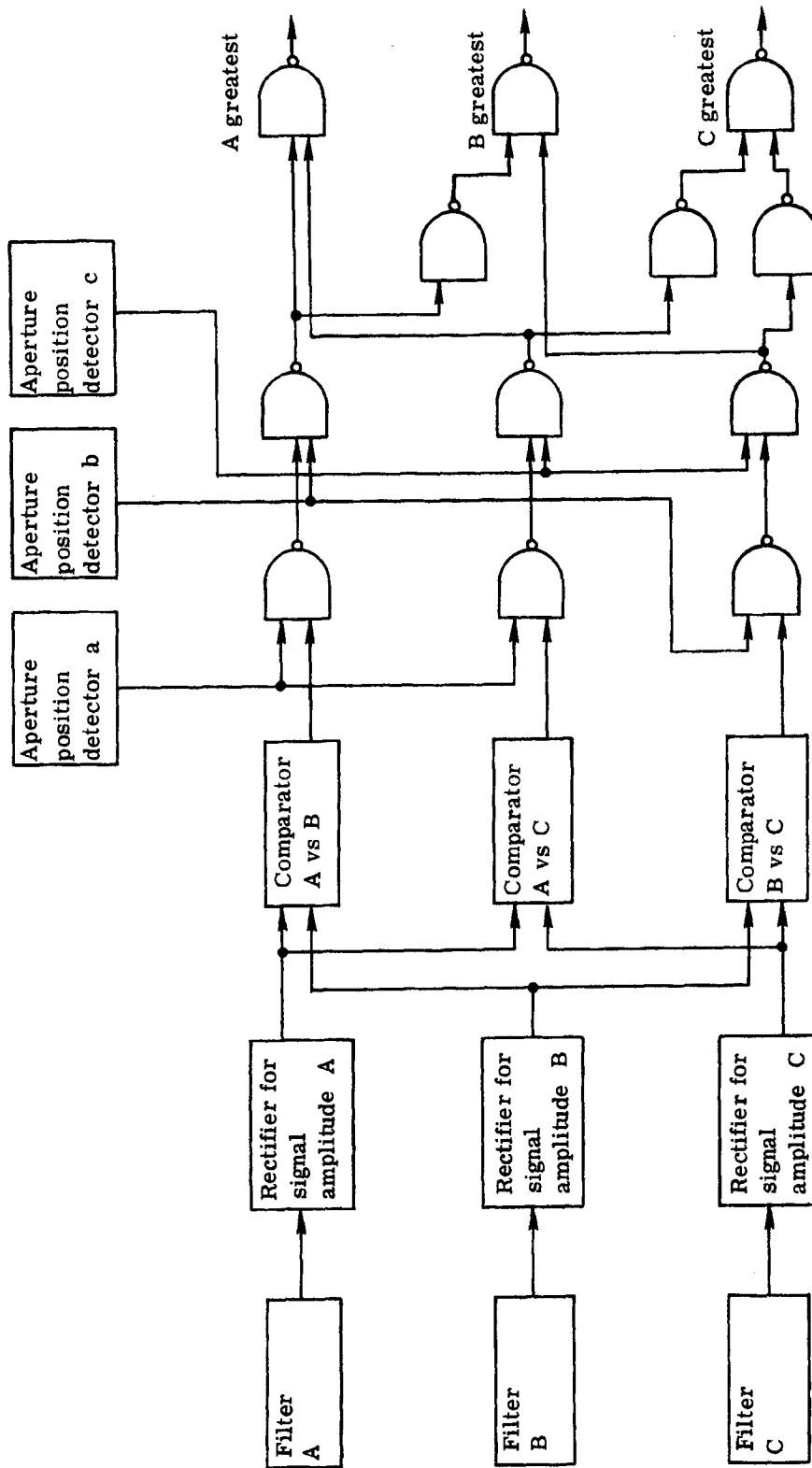


Fig. 2-10 — Signal selection logic, aperture position detection

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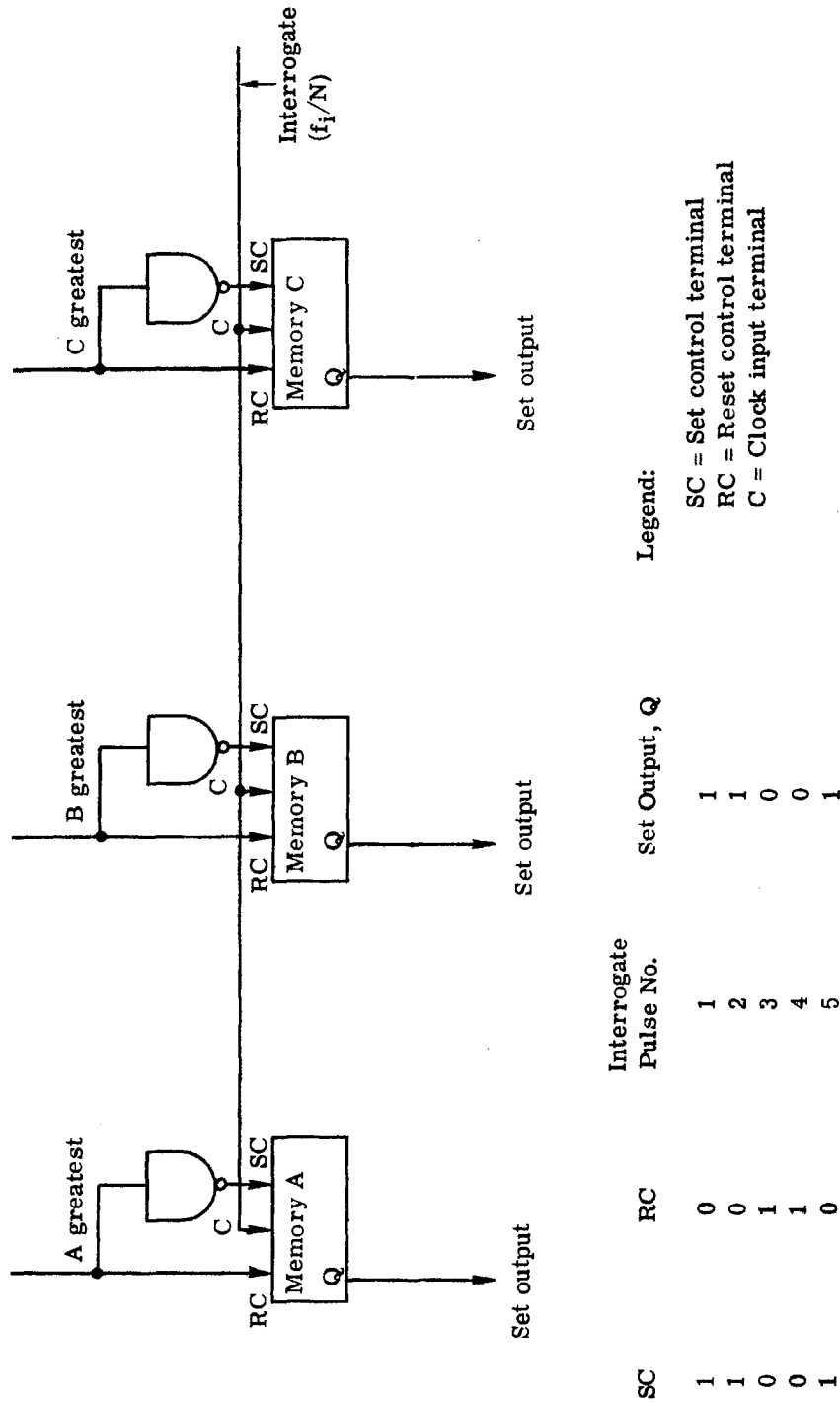


Fig. 2-11 — Memory logic states for signal selection logic (refer to Fig. 1-10)

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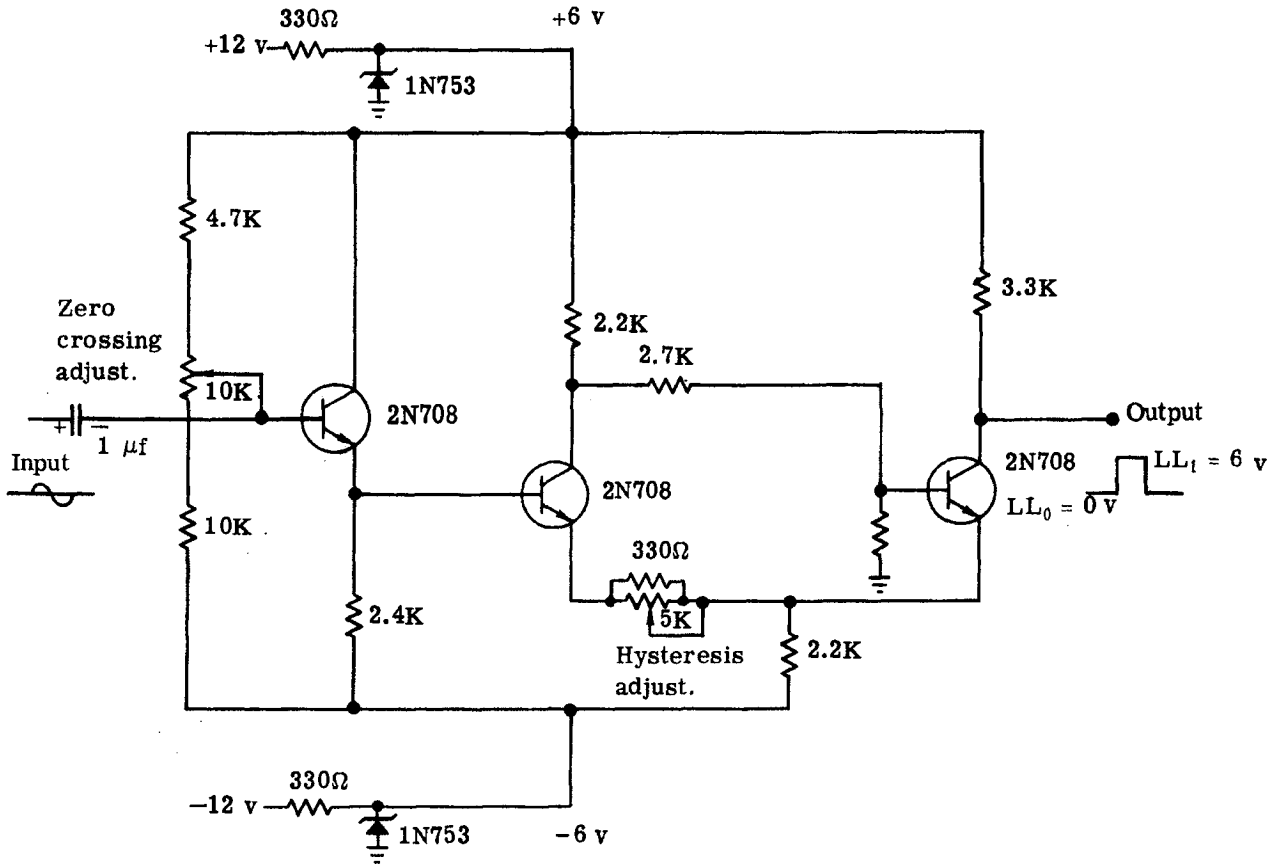


Fig. 2-12 — Zero crossing detector



### 8. Antilatch Circuit

The output of the output NAND gates may be zero due to one of two causes: (1) no circular aperture signals on any channel, and (2) latch up when power is turned on. If condition (2) exists, the absence of a signal for a period of time in conjunction with Aperture B position detector will cause the memory flip-flops to be sampled, thus removing any latch up. This situation is described in the next section.

### Pulse Dropout and Divide-By-N Logic

The function of this subsystem is to divide the output signal (from the signal selection logic) by N, where N can be 30, 40, 60, or 80. In addition, it detects when a signal has dropped out either naturally or by forced conditions.

The various components of this subsystem are discussed below.

#### 1. Counter-Encoder-Decoder

A ganged manual switch is used to set the encoder and decoder so that the counter will divide by the chosen value of N.

There are seven flip-flops in the counter which are necessary to count up to an N of 80. A diagram of the logic is shown in Fig. 2-13.

The signal at the arm of the encoder switch swings from an  $LL_1$  to and  $LL_0$  when there is a dropout (see Figs. 2-13 and 2-14). The encoder is designed to set the flip-flops in the counter to N-1. Therefore, if the decoder is set to 40, the encoder is set to 39. Note for example that if N = 40, the counter will be encoded to 39 (a count of 39) when a dropout exists. The next input to the counter will bring the counter to 40 and will be decoded. This encoding to N-1 allows for fastest processing of information in the frequency comparator when the counter receives another 40 pulses it will cause another decoded output.

The counter is reset to zero every time a count of N is reached. The flop-flops used are of the toggle type.

#### 2. Pulse Dropout

The circuitry used to develop the count input to the divide-by-N counter also detects a dropout. The dropout detection is best understood by referring to Fig. 2-14.

The input pulse is passed through a series of one-shot delay circuits, and, in addition, through a pulse shaper. The output of the "bracket" one shot is such that two succeeding pulses will be NAND-gated. In other words, the first input pulse is delayed and then looks for the second input pulse. If the second pulse exists, one NAND gate will pass this information to the counter. If the second pulse does not exist, another NAND gate develops what is called a dropout pulse.

Every time the signal selection logic generates a transition pulse, a forced dropout is introduced. The circuit for forced dropout is shown in Fig. 2-15.

The transition pulse will cause the set output and reset output of flip-flop A to go to  $LL_1$  and  $LL_0$ , respectively. This inhibits the input signal to cause a dropout via the input gate. The input signal will, however, pass through gate X and flip-flops B and C until the reset output of flip-flop C goes to an  $LL_0$  which resets flip-flop A to its normal state. Flip-flops B and C are reset via the count NAND gate.

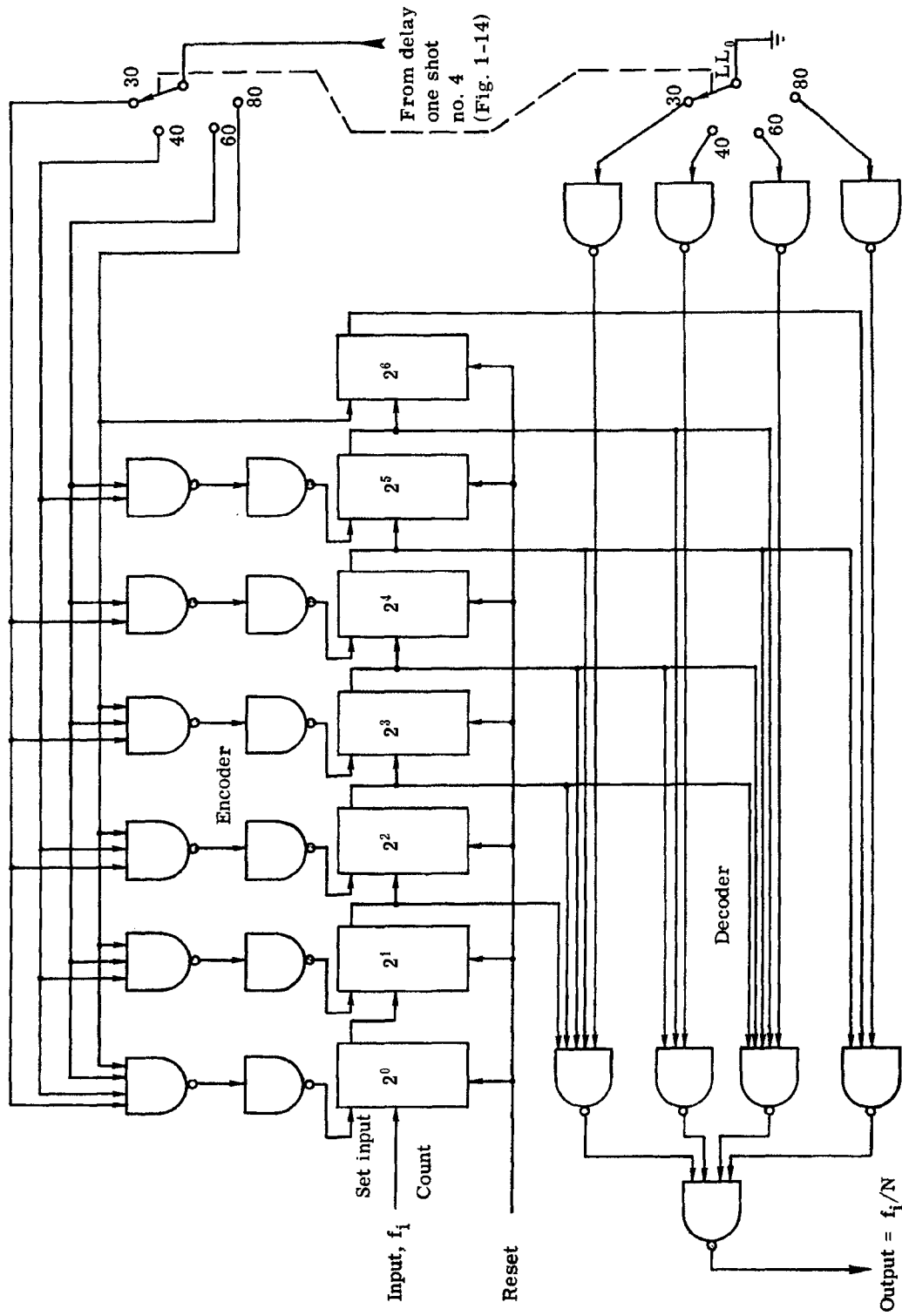


Fig. 2-13 — Pulse divide-by-N encoder and decoder circuit

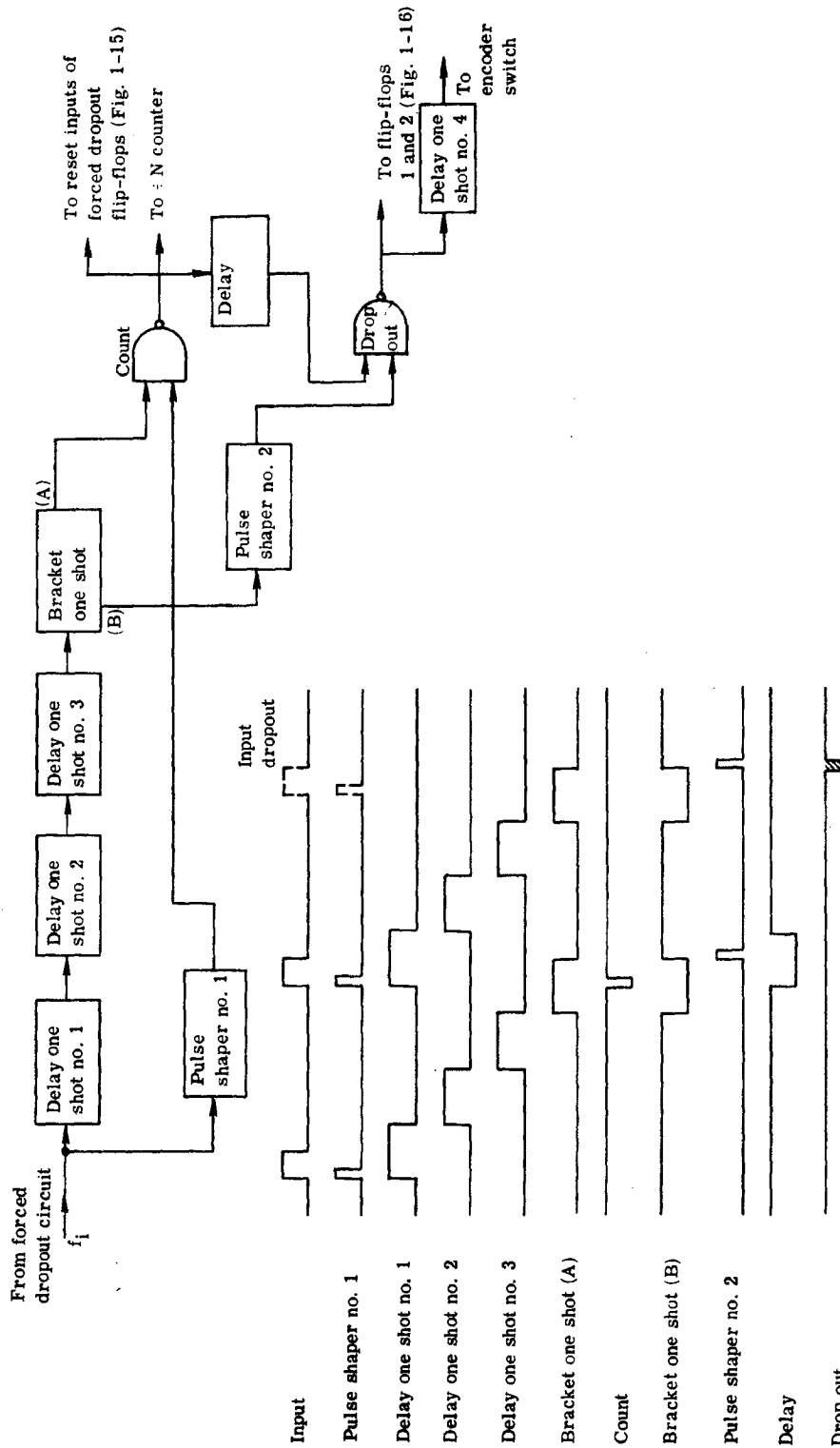


Fig. 2-14 — Pulse dropout circuit and timing diagram

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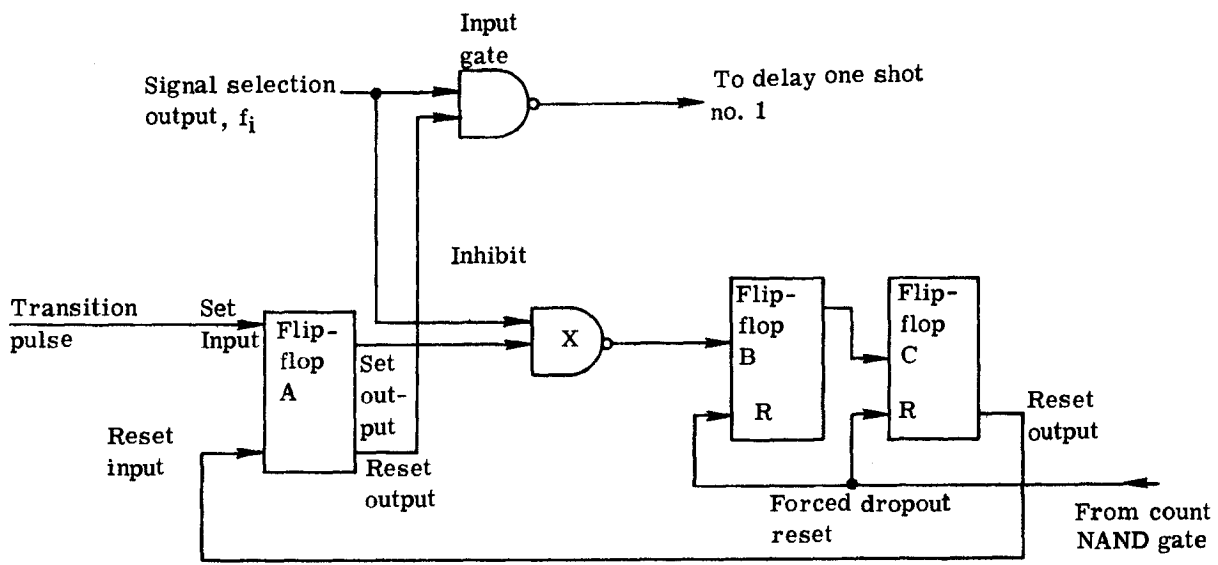


Fig. 2-15 — Forced dropout circuit

The purpose of detecting a dropout is to develop a read inhibit command which interfaces with the frequency comparator.

### Read Inhibit Command Circuitry

This circuitry is shown in Fig. 2-16. Under normal operating conditions, the set output of flip-flops 1 and 2 is at  $LL_1$ . When a dropout occurs, the set outputs of both flip-flops 1 and 2 go to an  $LL_0$ , thus inhibiting the read command gate in the frequency comparator. Because of the delay one shot, it takes two successive pulses from the decoder to bring the flip-flop no. 2 set output to  $LL_1$ . The first decoder pulse after a dropout will change the flip-flop no. 1 set output to 1, thus arming gate Y. The next decoder pulse will pass through NAND gate Y and trigger flip-flop no. 2 set output to an  $LL_1$ .

### Frequency Comparator

The various components of this subsystem are shown in Fig. 2-17. A discussion of their operation follows.

Let the output of the signal selection logic be called  $f_i$  and the output of the pulse dropout and divide-by-N logic be called  $f_i/N$ .

It is this signal,  $f_i/N$ , and  $f_o^*$  which are compared in the frequency comparator.

#### 1. VCO and N/5

The VCO is a voltage controllable clock. The frequency is adjusted according to the frequency of  $f_i$ . If it is desired to obtain, for example, a count of 10,000 clock pulses between successive  $f_i/N$  pulses, then the clock frequency

$$f'_c = 10^4 f_i/N$$

For example, if  $f_i = 2,500$  hz and  $N = 40$ , then

$$f'_c = \frac{1 \times 10^4 (2,500)}{40} = 625 \text{ khz}$$

Since the VCO is divided down by 8 in this case, the actual VCO frequency is 8 (625 khz) = 5.0 mhz.

The factor 8 is derived by a frequency divider whose division is  $N/5$  where  $N$  is 30, 40, 60, or 80. With these values of  $N$ , the corresponding frequency divisions are 6, 8, 12, and 16. The  $N/5$  counter is shown in Fig. 2-18.

For discussion purposes, let the output of  $N/5$  be designated as  $f'_c$ .

#### 2. $f_i/N$ Sync Logic (Fig. 2-19)

The function of this subsystem is to:

1. Obtain sync between  $f_i/N$  and  $f'_c$

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\* $f_o$  is a pulse rate generated by a reticle or shaft angle encoder.

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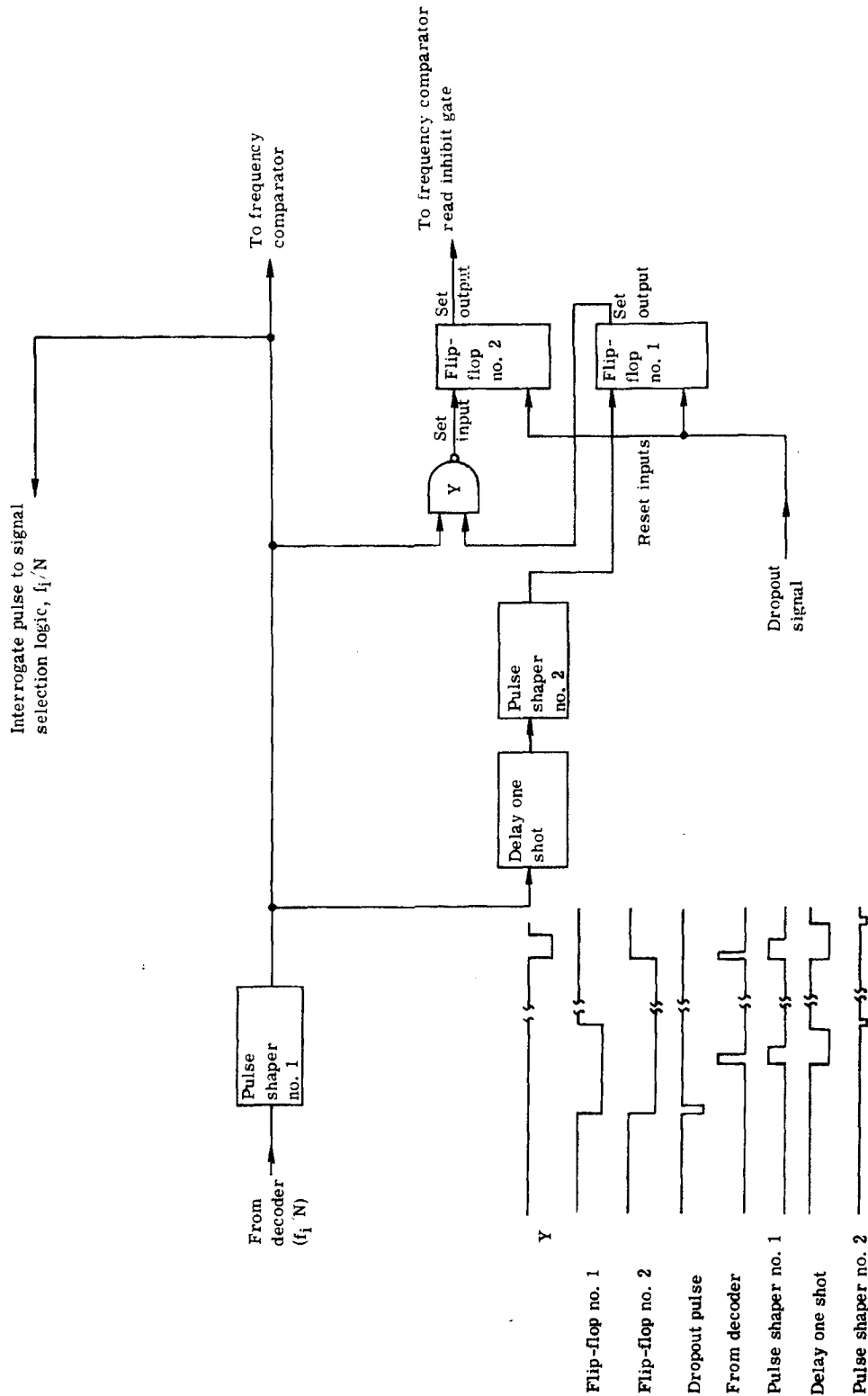
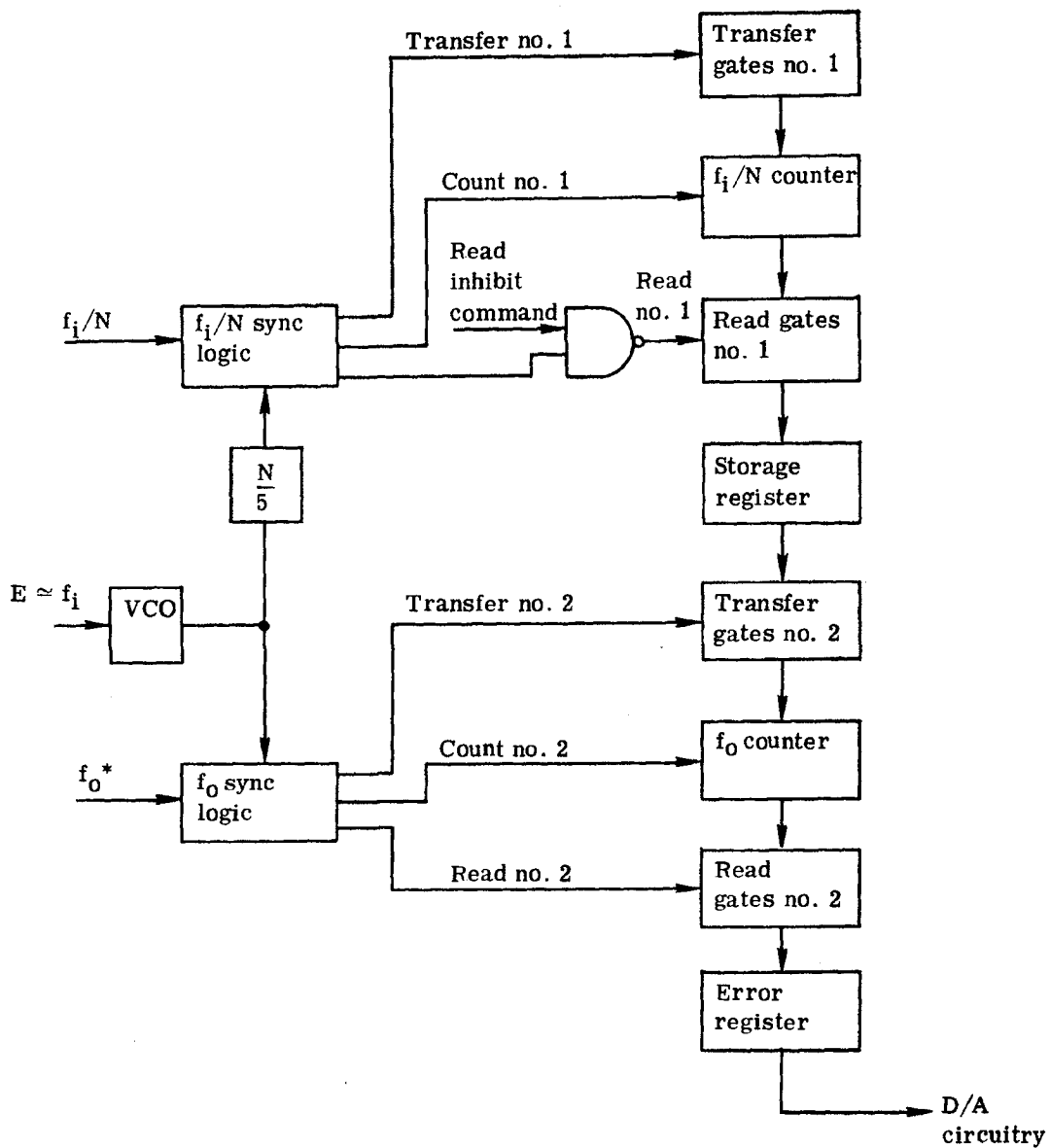


Fig. 2-16 — Read inhibit command circuitry



\* From reticle encoder  
or shaft angle encoder.

Fig. 2-17 — Frequency comparator

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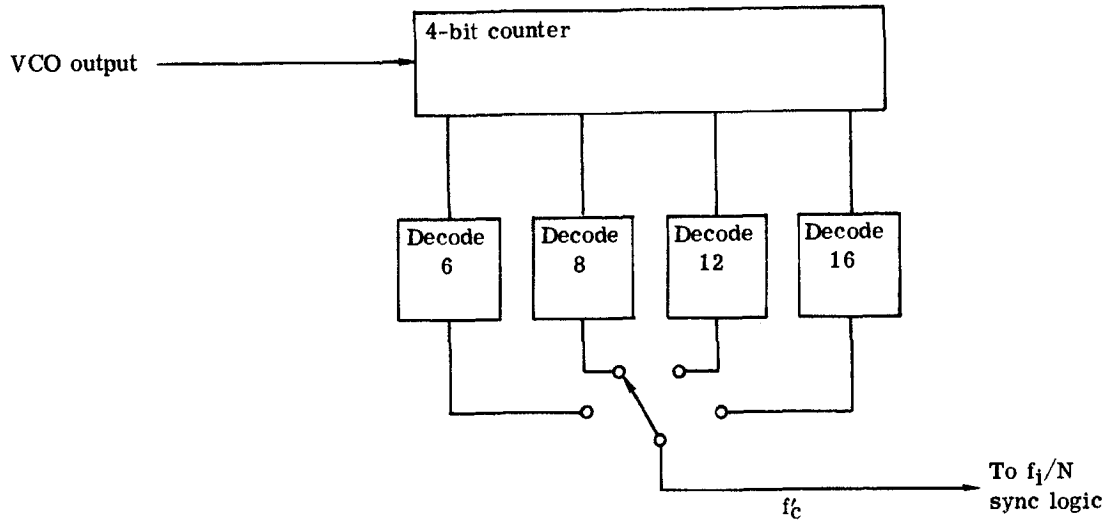


Fig. 2-18 — N/5 counter

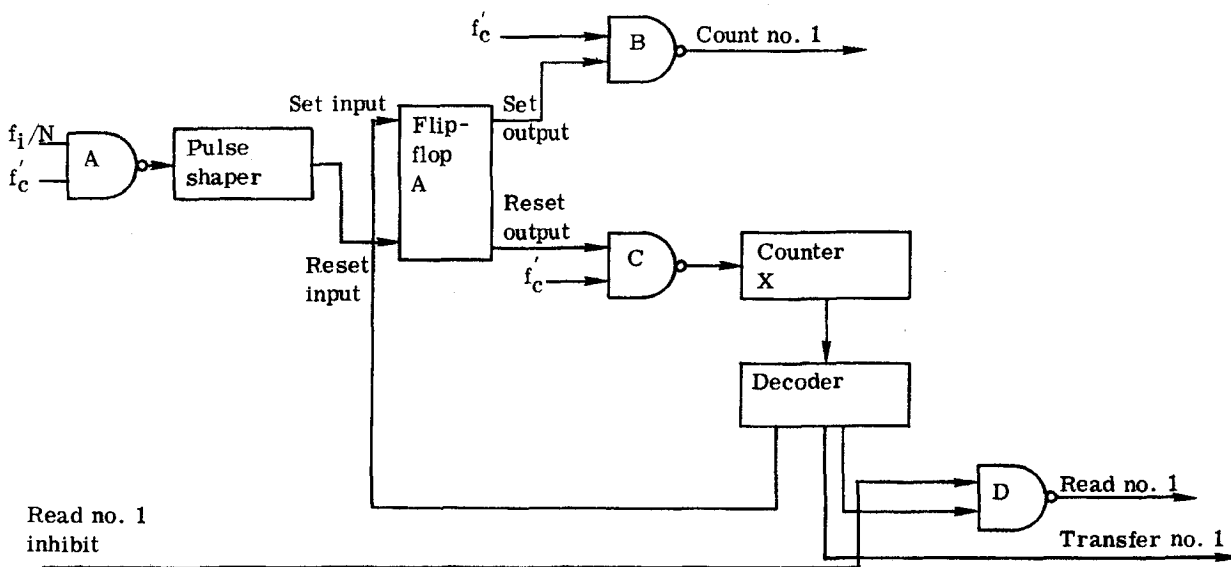


Fig. 2-19 —  $f_i/N$  sync logic



2. Generate, after sync is obtained, the following commands:

- a. Read no. 1
- b. Transfer no. 1
- c. Count no. 1

When  $f_i/N$  and an  $f'_c$  pulse coincide, NAND gate A will trigger the pulse shaper which in turn resets flip A to set out =  $LL_0$ , reset out =  $LL_1$ .

With this condition, gate B does not pass any  $f'_c$  pulses into the  $f_i/N$  counter. Gate C, however, passes  $f'_c$  information into counter X. The information in counter X is decoded at various counts to develop the read no. 1 command, transfer no. 1 command, and a reset pulse which changes the state of flip-flop A to set out =  $LL_1$ , reset out to  $LL_0$ . These commands are generated in the above sequence; eight  $f'_c$  pulses are required for this process to occur. Once flip-flop A has reset gate B,  $f'_c$  pulses will increment the  $f_i/N$  counter. Since this is a periodic event, it can be said that eight  $f'_c$  pulses are deliberately deleted in the count of the  $f_i/N$  counter.

Note that gate D contains the read no. 1 inhibit input which is generated in the pulse dropout and divide-by-N logic.

3. Transfer Gates No. 1,  $f_i/N$  counter, Read Gates No. 1 and Storage Register

The  $f_i/N$  counter is a ripple through counter containing 14 bits which can count to  $2^{n-1} = 16,383$ .

Attached to the set and reset inputs of each flip-flop is a NAND gate which sets each flip-flop upon receiving the transfer no. 1 command. In this case, each flip-flop set output will be set to an  $LL_0$  and the reset output to  $LL_1$ . These input NAND gates are the transfer no. 1 gates. Attached to the set and reset outputs of each of the flip-flops are another set of NAND gates which are called the read no. 1 gates. Upon receiving the read no. 1 command, the read no. 1 gates transfer (in parallel) the count which is in the  $f_i/N$  counter at that time to the storage register.

4.  $f_0$  Sync Logic

The  $f_0$  sync logic works in much the same manner as the  $f_i/N$  sync logic. The outputs of the  $f_0$  sync logic are the read no. 2, transfer no. 2, and count no. 2 commands in that time sequence. In this subsystem, seven clock pulses are deleted from the count entering the  $f_0$  counter, one less than the deleted count entering the  $f_i/N$  counter.

The incoming signal,  $f_0$ , has a frequency of 2,500 hz when  $f_i$  is 2,500 hz. Within the sync logic is a divide-by-5 counter. Therefore, the VCO which is at 5 mhz is sync'd with  $f_0/5$  or 500 hz, allowing for a count of

$$N = \frac{f_c}{\frac{f_0}{5}} = \frac{5 \times 10^6}{500} = 1 \times 10^4$$

5. Transfer No. 2 Gates,  $f_0$  Counter, Read 2 Gates, Error Register, D/A Circuitry

The transfer no. 2 gates are arranged such that the output of each flip-flop in the storage is complimented into the  $f_0$  counter. The  $f_0$  counter has one extra flip-flop and its

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associated input gate which is used for the sign bit. This flip-flop is turned to  $LL_0$  at the set output via the transfer no. 2 command. Note that there is no associated flip-flop in the storage register for the sign bit.

Due to the fact that the  $f_0$  counter has the complimented output of the  $f_1/N$  counter (bit by bit) and one more clock pulse is allowed to increment the  $f_0$  counter than the  $f_1/N$  counter, then if  $f_0 = f_1$ , the output of the  $f_0$  counter after counting will be 00000000000001, corresponding to a zero error.

The read 2 command will gate the first seven (least significant) bits plus the sign (most significant) bit into the error register.

The outputs of the error register are fed into the D/A where the analog equivalent signal is developed.

The output characteristic of the D/A circuitry (which is a D/A plus a buffer amplifier) is shown in Fig. 2-20.

#### 2.1.1.2 Aperture Belt Studies and Measurement

As is discussed in report 9416-68-026, the moving aperture is essential to sensor performance. The present sensor concept uses an aperture belt configuration as shown in Fig. 2-21.

The two methods of manufacturing these belts are: (1) photographic, and (2) punched pattern.

The primary difficulty in fabricating the belt is maintaining the accuracy on the hole diameter to  $\pm 0.0001$  inch.

##### Photographic Method

The photographic method utilizes a step and repeat process on 5-inch, 3404 material. A fixture which has the required aperture pattern, indexing feature, and attached light box has been fabricated (see Fig. 2-22). Results have been very satisfactory in that sharp edges and accurate indexing have been obtained. Measurements of the repeatability of the hole diameters have not yet been made, but no problem is expected.

##### Punching Method

Photographic belts are adequate for laboratory work with brassboards. Ultimately, however, the aperture patterns punched in a metal belt will be required. In anticipation of this requirement, an experimental punch and die (see Fig. 2-23) has been fabricated. Several different punch configurations have been tried. Results were excellent when 0.001-inch stainless steel was used. Edges of the punched holes were extremely smooth, and the diameter is repeatable to within 2 microns.

#### 2.1.2 Along-Track Servo

The along-track servo completes the along-track portion of the multichannel brassboard. This servo design is unchanged from that previously described and analyzed in Itek Final Report No. 9416-68-026, dated 19 April 1968.

#### 2.1.3 Status

All the signal processing circuits previously described have been fabricated and satisfactorily tested. The 5-inch target drive and aperture belt drive are both operational. Integration of

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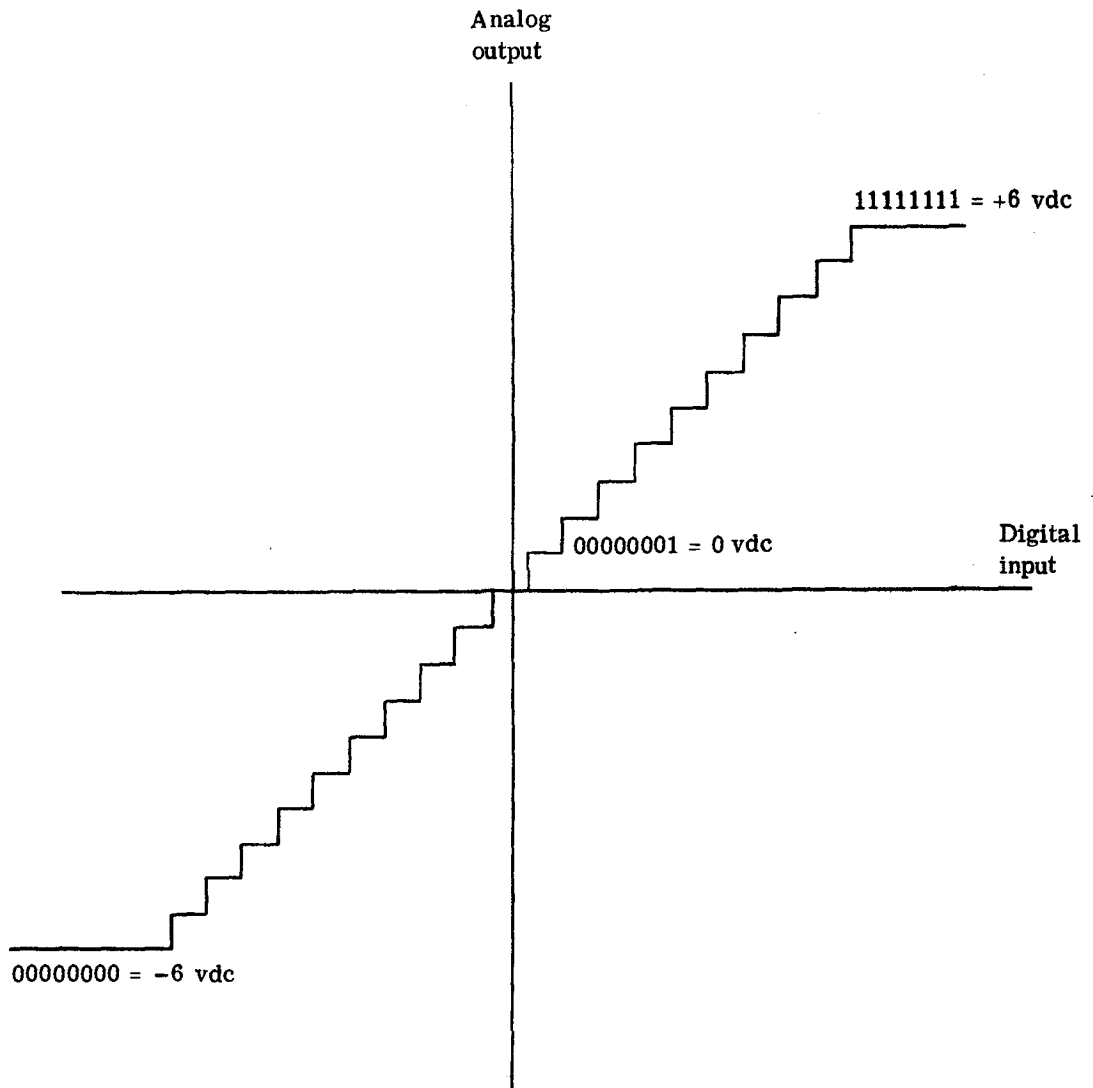


Fig. 2-20 — Output characteristics of D/A circuitry

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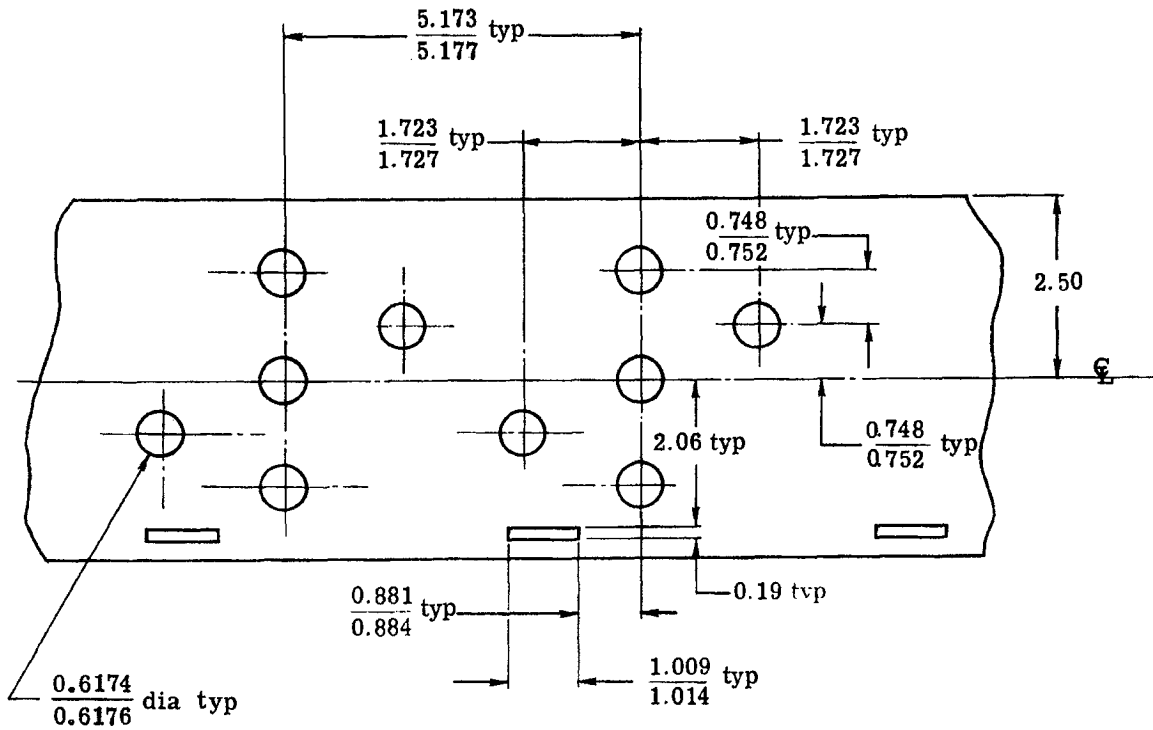


Fig. 2-21 -- Multichannel aperture belt

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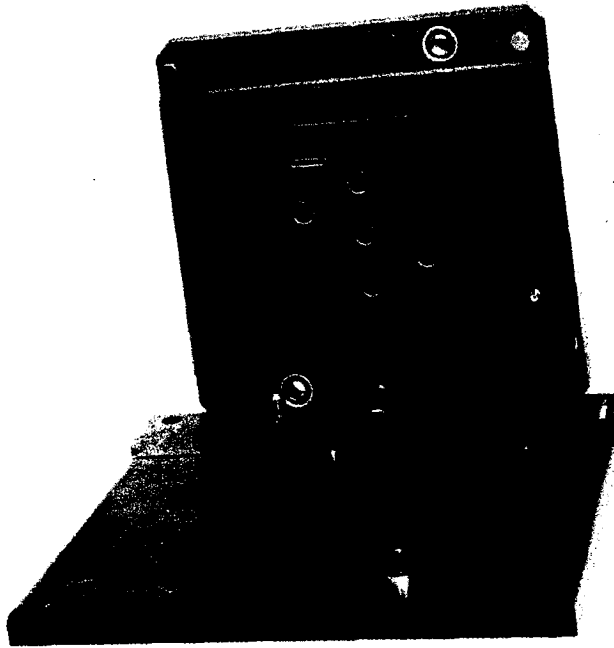
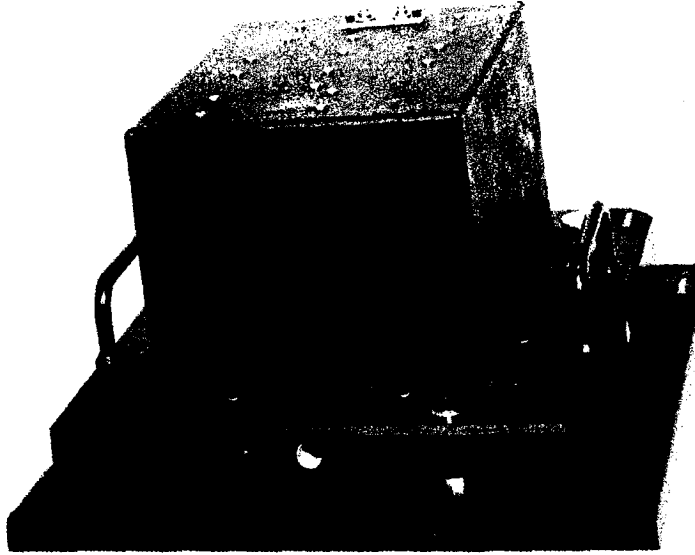


Fig. 2-22 — Aperture belt photographic fixture

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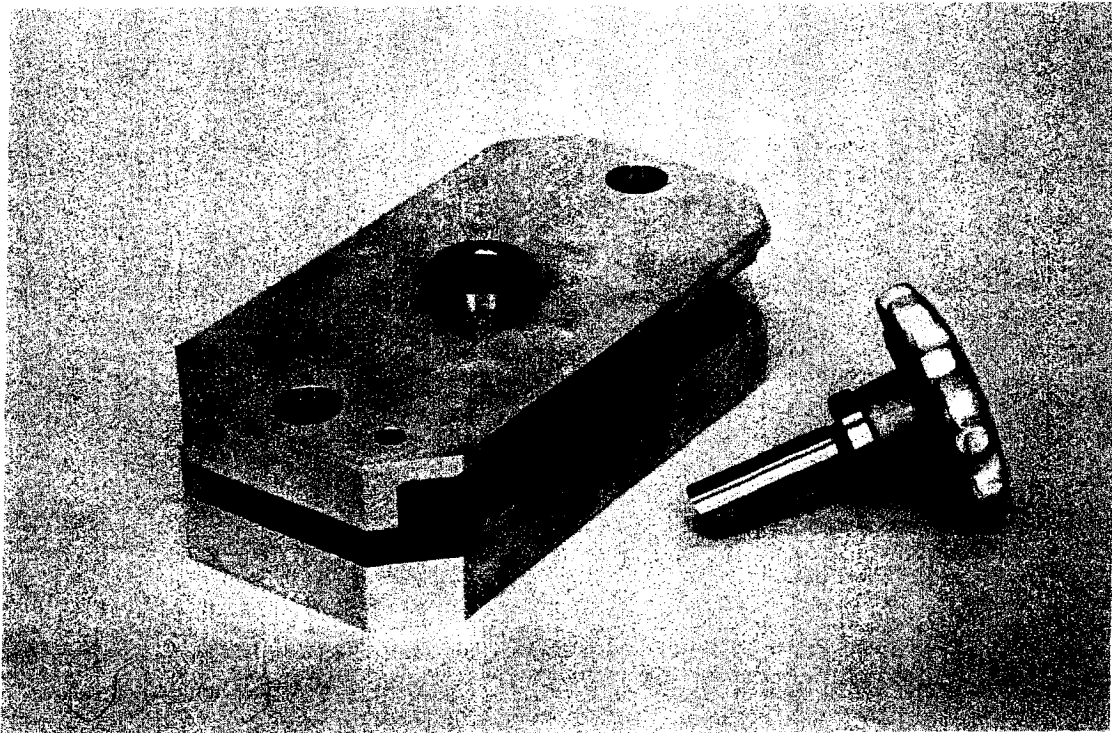


Fig. 2-23 — Punch and die fixture

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the 9 1/2-inch film drive servo with the along-track sensor electronics is essentially complete. The sensor electronics-servo integration was accomplished using a sinusoidal oscillator to simulate the signals in each of the three along-track channels. Signals of variable amplitude and phase were simulated. The effect of signal selection switching transients on the 9 1/2-inch film drive is essentially nil.

Test and alignment of optical components and fabrication of an aperture belt are complete. Testing of a fully integrated along-track sensor is expected to be started in the middle of November.

## 2.2 CROSS-TRACK SENSOR AND SERVOS

In the search for a technique to apply to the cross-track sensor, it was noted that the along-track sensor technology could be applied directly to the herringbone reticle configuration shown in Fig. 5-1 of report no. 9416-68-026. As shown in the figure, an angular misalignment,  $\delta$ , of the image velocity vector and the reticles causes a difference frequency ( $f_R - f_L$ ) of magnitude.

$$(f_R - f_L) = \frac{2v_i}{\lambda} (\sin \theta) (\sin \delta)$$

or, if  $\delta$  is small

$$(f_R - f_L) = \frac{2v_i}{\lambda} (\sin \theta) \delta$$

The fraction of change in frequency is given by

$$\frac{(f_R - f_L)}{f} = \frac{2v_i/\lambda (\sin \theta)}{v_i/\lambda \cos \theta} \delta = 2 (\tan \theta) \delta$$

where  $f$  = nominal frequency of the two sensor channels.

Since  $\tan \theta$  approaches  $\infty$  as  $\theta$  approaches  $\pi/2$ , it would appear that the fractional change in frequency can be made arbitrarily high. Practical considerations such as sensor frequency response, electronic noise, and the magnitude of  $\delta_{\max}$  prohibit this. Tentatively, a compromise angle,  $\theta$ , of 45 degrees has been chosen which gives a sensitivity of 0.06 percent per arc-minute and a nominal output frequency which is 70 percent of maximum.

It should be noted that the herringbone reticle configuration is subject to the same phase rate errors and noise sources as the along-track sensor. Because of this, moving apertures will be utilized.

### 2.2.1 Brassboard Design Approach

The K-mirror system (Fig. 2-24) provides the means for introducing image rotation. In a final configuration, the entire camera back would be rotatable and servoed to align the angle bisector of the cross-track sensing reticles to the image vector. However, this arrangement would have been cumbersome in the brassboard. Therefore, the sensors are held fixed and the K mirror is driven. This scheme does not compromise the cross-track sensor testing. Testing with this arrangement will consist of first aligning the image vector to the cross-track sensor, and noting the position of the K mirror. A micrometer located on the K-mirror housing

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will be used for this purpose. Next, the K mirror will be offset, thereby causing the image to rotate with respect to the sensing reticles. The amount and direction of the offset will be measured electronically, and used to servo the K mirror back to the initial alignment position. Performance of the system will be verified by recording the micrometer position.

Fig. 2-25 shows a block diagram of the brassboard cross-track control loop. The blocks titled "signal processing electronics" and "frequency comparator" are essentially identical in design to those circuits previously tested and described in Section 1.1. The output,  $\Delta N$ , of the frequency comparator is a parallel binary number proportional to the difference frequency,  $f_R - f_L$ , which in turn is proportional to the image rotation angle,  $\delta$ . Control of the K-mirror position is accomplished by transferring the digital number,  $\Delta N$ , into the up/down counter.

When the K-mirror servo is energized, the incremental encoder will increment the counter contents toward zero, thereby returning the K mirror back toward the initial alignment position. The constants of the control system are such that  $22\frac{1}{2}$  degrees of rotation at the motor shaft produce 64 encoder pulses and 8 minutes of K-mirror rotation (16 minutes of image rotation).

### 2.2.2 Cross-Track Sensor Signal Generation and Processing

Generation and processing of the right and left cross-track sensor signals will be identical to the methods used for the along-track sensor signals; however, signal channel selection logic will not be employed. The bandwidth requirements of the cross-track sensor can be an order of magnitude lower than for the along-track sensor. Hence, multichannel signals are not felt to be necessary at the present time. The up/down counter design is straightforward and should not present any problem.

### 2.2.3 Status

Fabrication of all optical and mechanical components of the cross-track sensor and servo are essentially complete. Optical assembly and alignment are continuing. Design of the signal processing circuits is in process and fabrication is expected to be completed by 15 December 1968.

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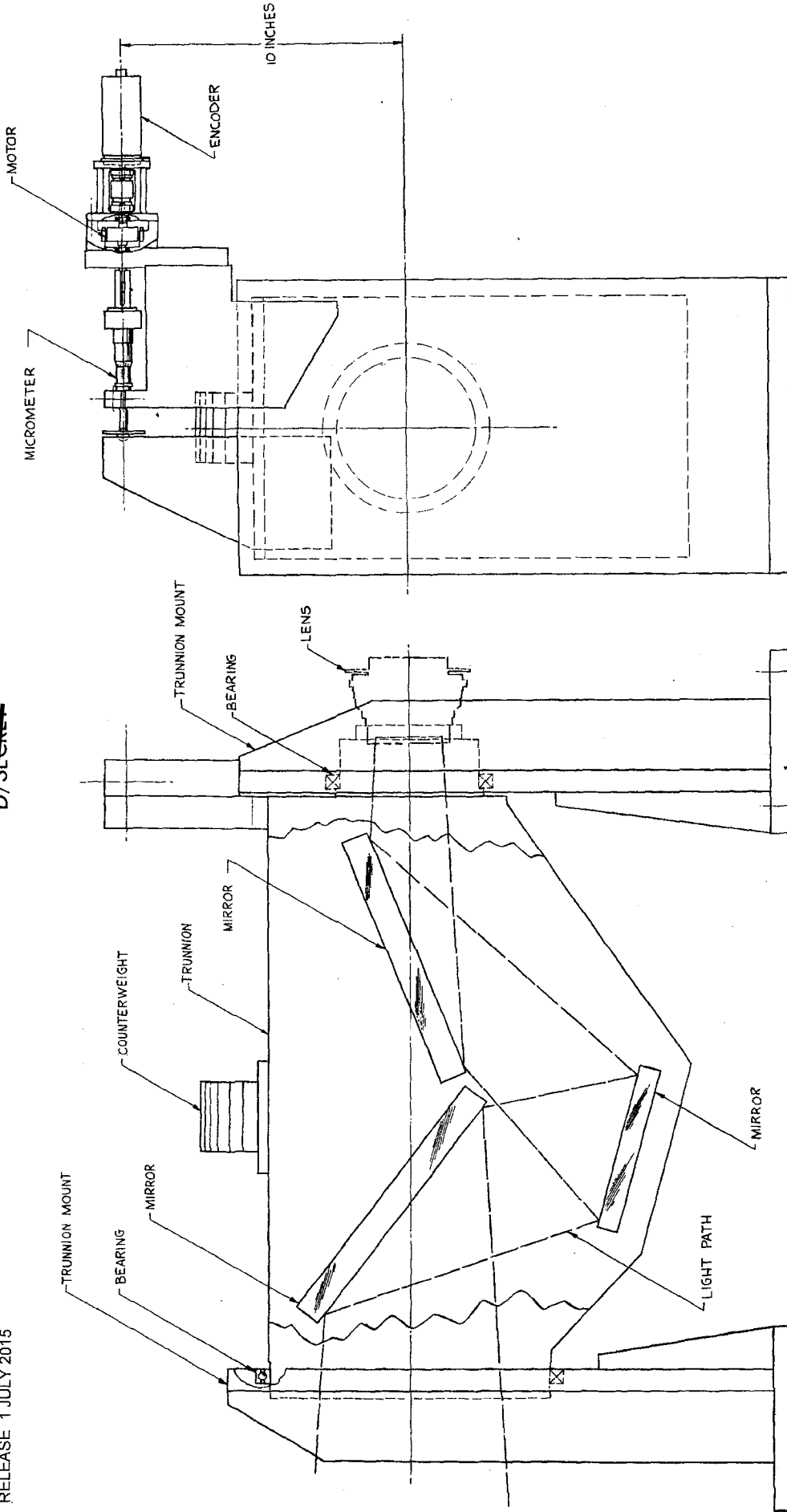


Fig. 2-24 — Descriptive outline of K-mirror assembly

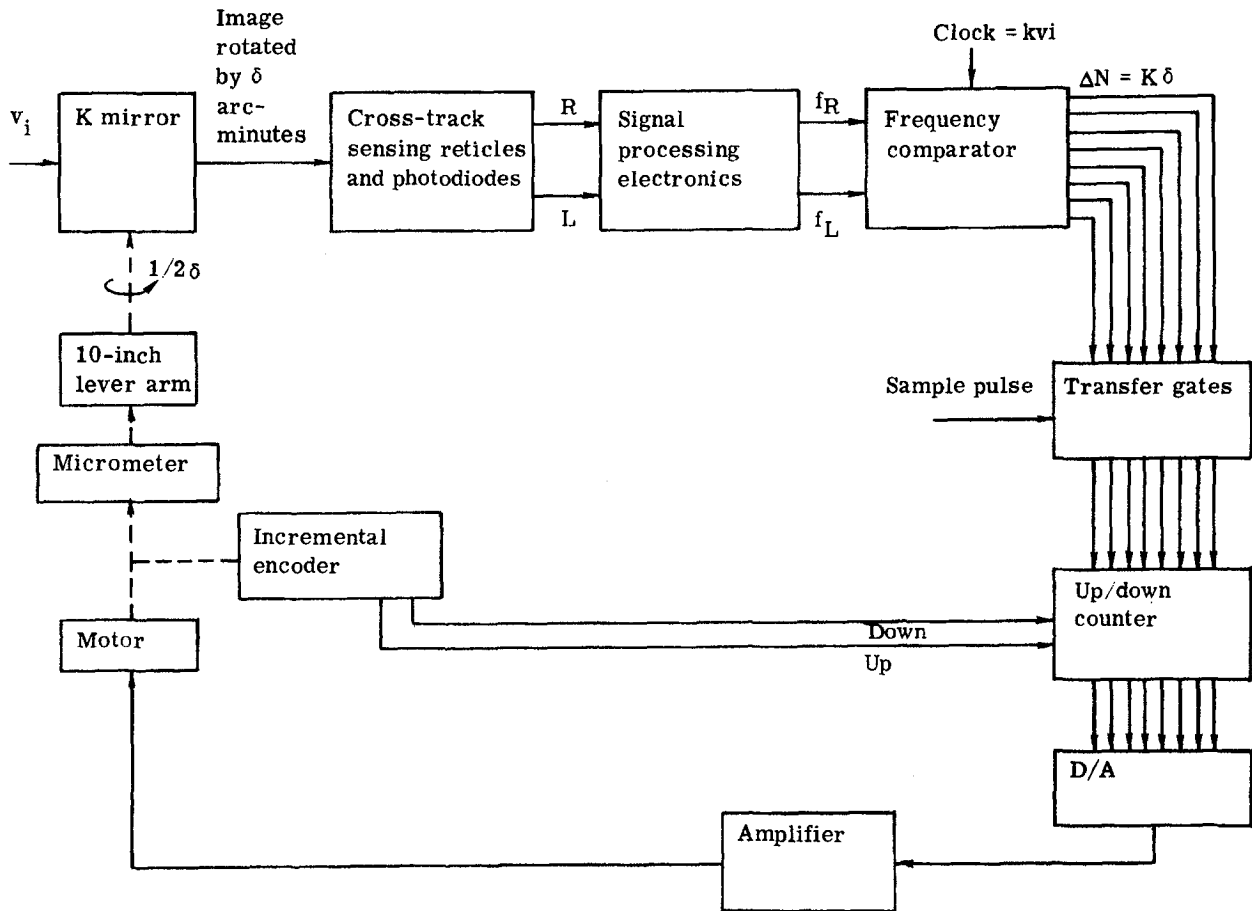


Fig. 2-25 — Block diagram cross-track sensor/servo

### 3. FOCUS SENSOR

#### 3.1 FOCUS SENSOR REQUIREMENTS

The system analysis conducted under Phase I of this feasibility study was reported in Itek report no. 9416-67-011. The 2-sigma focus error budget was presented in that report and is reproduced here as Table 3-1. For a detailed description of the various sources, reference should be made to Section 2.4 of the above referenced report. Essential requirements of the sensor are: (1) operation with image quality of the variable obscured entrance pupil ( $f/7.0$  to  $f/10.0$ , as described in Section 2.5.3 of the report); (2) sensitivity of  $0.4 \times 10^{-3}$  inch (10 microns); (3) capability of being set to  $0.9 \times 10^{-3}$  inch; (4) capability of operating in a servo with a focus adjustment error better than  $0.2 \times 10^{-3}$  inch; and (5) operation with the entrance pupil modulation from approximately 0.09 to 0.31 with the correlation with sun angle as indicated in Figs. 2-2 and 2-5 of report 9416-67-011. The total rss allowable defocus error is [REDACTED]

#### 3.2 DOUBLE SLIT SENSOR

It is known that the MTF of a lens is dependent upon the focal position. For an essentially aberration-free lens, the transfer function at lower spatial frequencies is a maximum at best focus and falls off nearly symmetrically on both sides of the best focal position. When a moving scene (Wiener spectrum) is convolved with the lens transfer function, the resulting power spectrum, detected by a slit and photosensors, exhibits the same maximum at best focus. If parallel identical slits are offset in the focus direction, they will exhibit equal electrical power only if the focal plane is midway between them, and the difference in power will be a function of the focal error. Processing of the difference signal will then give a focus error signal for servo operation. A block diagram of the double slit experimental arrangement appears in Fig. 3-1. The double slit type sensor brassboard consists of a double slit, directly behind which is mounted a double photodiode. The assembly is rotatable about an axis parallel to and approximately coincident with the slits. The relative defocus of the slits is established by the angle of rotation. This whole assembly is mounted on a focusing slide. The potential simplicity of the sensor makes it most attractive.

#### 3.3 RETICLE TYPE FOCUS SENSOR

Experimental studies with the along-track sensor have permitted an evaluation of the dependence of signal amplitude at the reticle generated temporal frequency (i.e.,  $f = v_i/\lambda$ , where  $v_i$  is the image velocity and  $\lambda$  is the reticle wavelength) on the focal position. The focal sensitivity of this signal is dependent upon the reticle wavelength, the bar-to-space ratio, the lens image quality, and the spatial information content of the scene (see Itek report no. 9416-67-011). In the evolution of the along-track sensor, techniques for image splitting were investigated, and the initial study of the sensor will utilize the configuration shown in Fig. 3-2.

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The reticle type sensor brassboard consists of two sensor channels, the energy being divided equally between the two by a pellicle. Each channel can be focused individually with its own slide. Condensers image the lens pupil onto the photodiodes, thus collecting all the light transmitted by the reticle.

### 3.4 FOUCAULT SENSOR

A novel concept which is similar to a Foucault test has been generated for a focus sensor (see Fig. 3-3). An image point, P, is moving at velocity  $v_i$ . A stationary slit, S, is placed in the image beam at a position which is displaced from best focus. Note that as the bundle moves past the slit, only a small portion of the light is transmitted. The transmitted portion sweeps across plane A in the same direction as  $v_i$ . If the slit were placed outside of focus, as in Fig. 3-4, the transmitted portion of the beam would scan across plane A in the opposite direction. Now if two photosensors (A and B) were placed at plane A, it would be possible to detect whether the slit was inside or outside of focus by knowing which cell is illuminated first, i.e., the relative phase of the two sensor outputs. This is the basic concept of the Foucault focus sensor. A practical method of implementing this basic concept is described below.

As shown in Fig. 3-5, a condenser lens images the pupil of an optical system onto a photocell with two segments, A and B. A square wave reticle is placed in the vicinity of best focus. Note that the space, d, between bars is small compared with the wavelength,  $\lambda$ . For purposes of discussion, assume that a point (or line image parallel to the reticle bars) is moving across the reticle with velocity  $v_i$ . As the point image traverses the reticle, the reticle spaces behave as individual slits. The "shadow" of the spaces sweep across the photocell, the direction being dependent on whether the reticle is inside or outside of focus. The net result is that each segment of the photocell would produce an approximate square-wave output. The relative phase of these two square waves changes abruptly as the reticle moves through focus. The signal processing circuit would detect these phase changes, thus determining best focus.

For purposes of discussing the operating principle of the device, it is convenient to consider the image to be a single point source. The generalization to the case of a real scene is based on the fact that a segment of a real scene can be constructed from an array (albeit an infinite array) of point sources.

The Foucault sensor testing will be done on one of the sensor channels of the reticle type sensor brassboard. The only difference is that the single photocell is replaced by a segmented (dual) photocell.

### 3.5 TEST CONFIGURATION

Fig. 3-6 is a layout of the focus sensor brassboard. A modular approach affords the required flexibility. The basic structure is an optical bench on which are mounted the target drive, lens, and sensor head modules.

The single channel brassboard (which is the earlier generation of the along-track sensor brassboard) is used as a target drive. In order to ensure that accurate target focusing is maintained, the target film will be run over rollers which are mounted to the optical rail, as opposed to having the assembly mounted on a separate structure.

The lens, a Goerz Magnar II, is mounted in a straightforward manner in a rigid holder; a 2:1 conjugate is used.

Figs. 3-7 and 3-8 show the three sensor head modules.

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### 3.6 TEST PROGRAM

The experimental program will comprise an evaluation of each of the three focus sensors at elementary level. The evaluation of the electrical signals produced will be used to determine which of the sensors will be refined and developed into a complete focus sensor breadboard. The common characteristic of the sensors, namely the absence of the moving parts (which seems possible because the image moves), will be a goal of the development.

Table 3-1 — Focus Error Budget (2- $\sigma$  probability)

Random Sources	Error, inches $\times 10^{-3}$
Focus sensor sensitivity	0.4
Focus adjust servo error	0.2
Film flatness	0.7
Film thickness variation	0.2
Focal plane roller runout	0.1
Camera back thermal changes $\pm 2^\circ\text{F}$ temperature differential	0.12
Vibration	0.1
Slant range variation over format	0.45
Terrain height variation	0.01
Root sum square, random	1.0
Systematic Sources	
Focus sensor initial setting	0.9
Camera back structural stability	0.3
Root sum square, systematic	1.0
Total, random and systematic	$2.0 \times 10^{-3}$ inch

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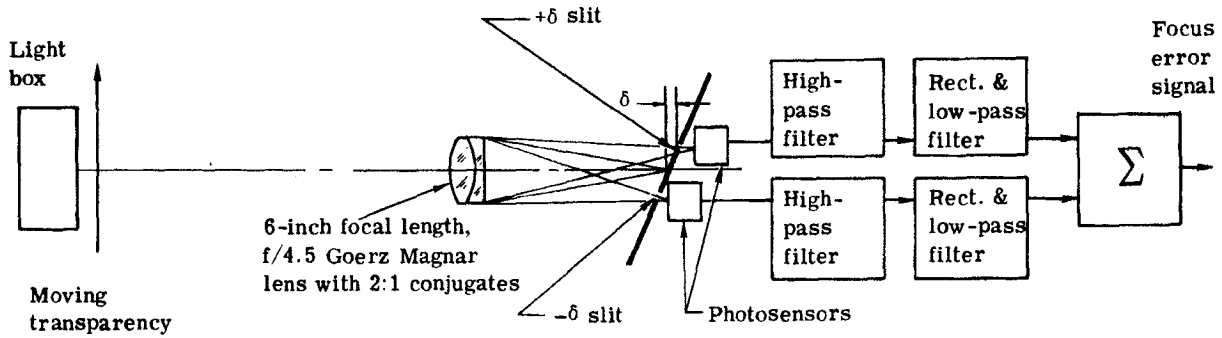


Fig. 3-1 — Double slit focus sensor

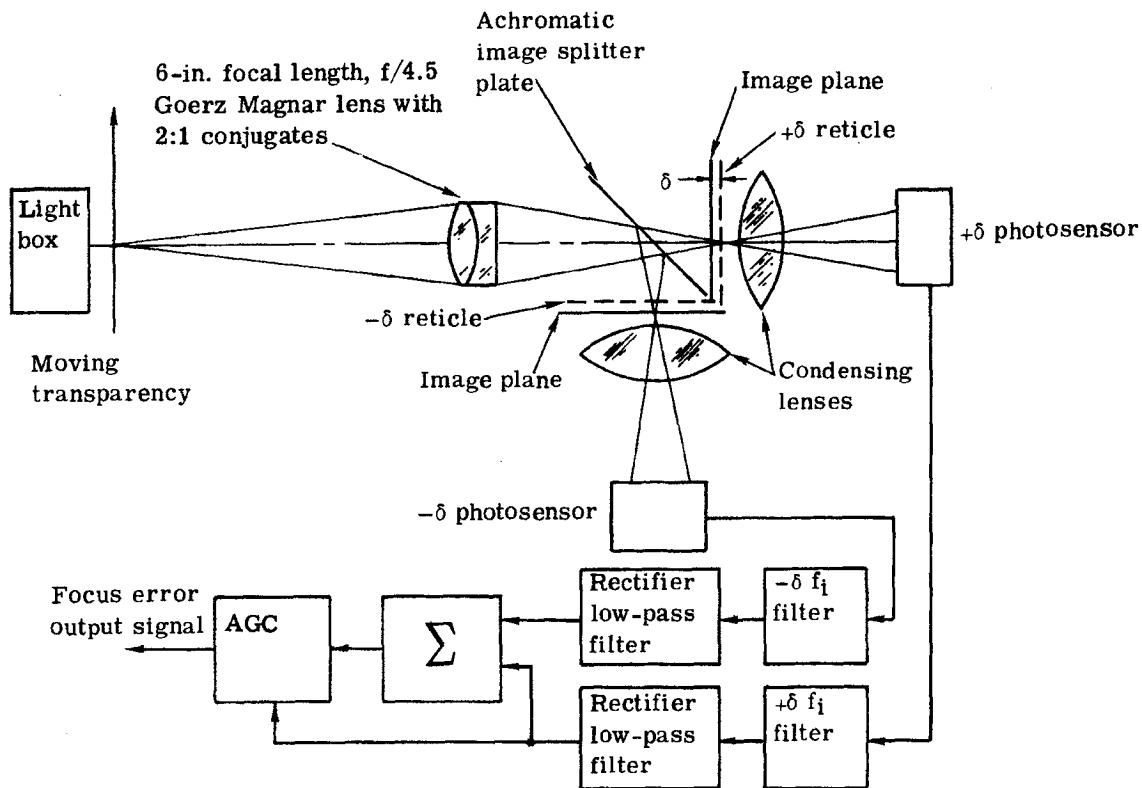


Fig. 3-2 — Reticle type focus sensor

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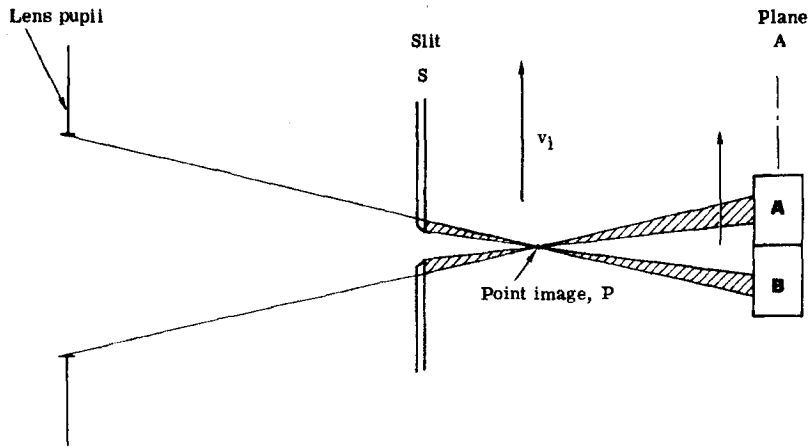


Fig. 3-3 — Foucault focus sensor concept (inside best focus)

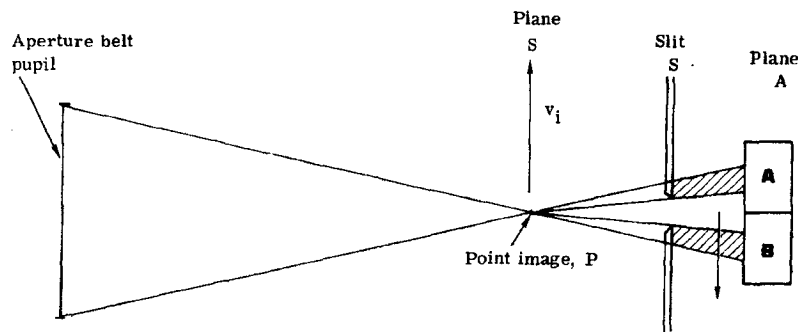


Fig. 3-4 — Foucault focus sensor concept (outside best focus)

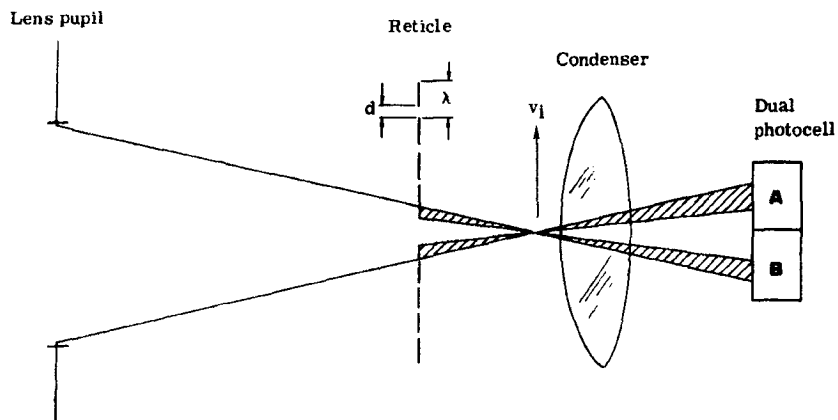


Fig. 3-5 — Foucault sensor configuration

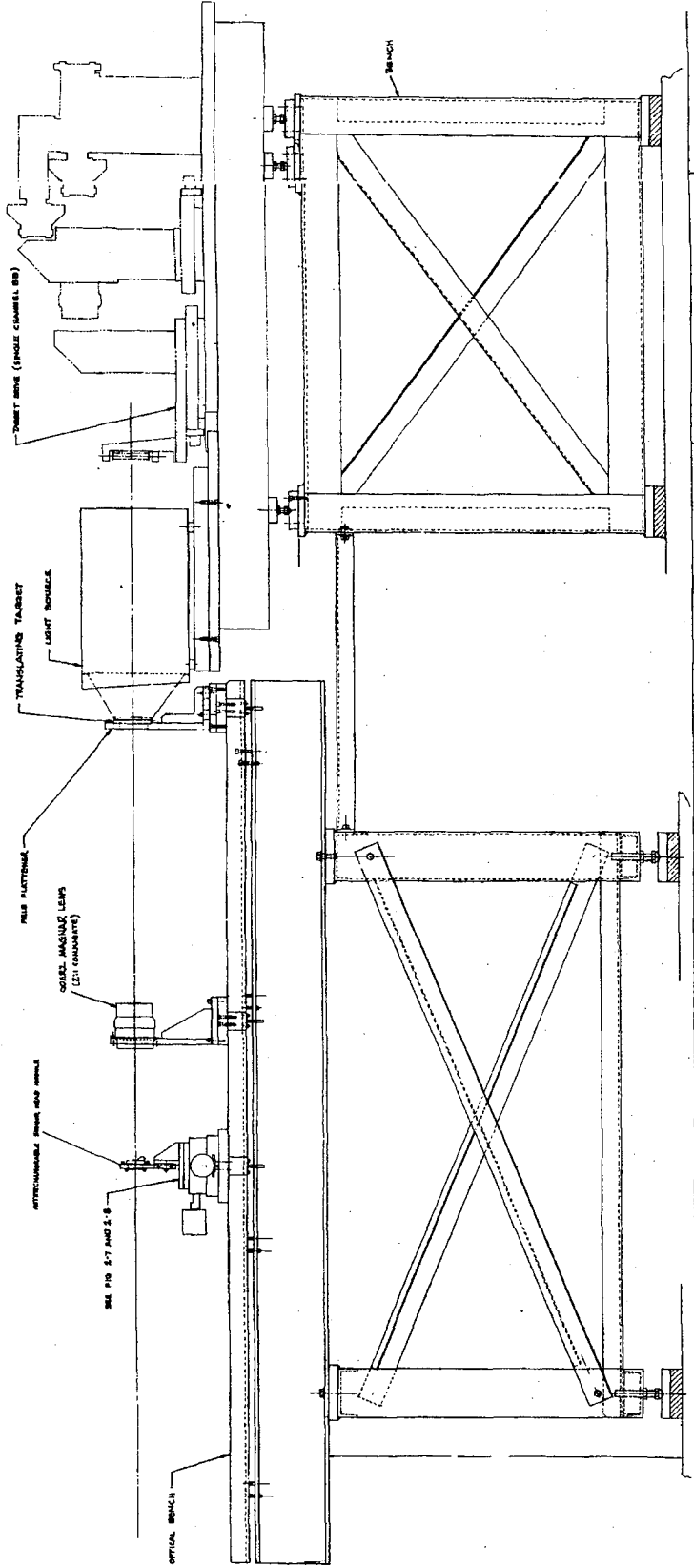


Fig. 3-6 — Focus sensor BB—general layout (sheet 2 of 3, right end)  
(128777)



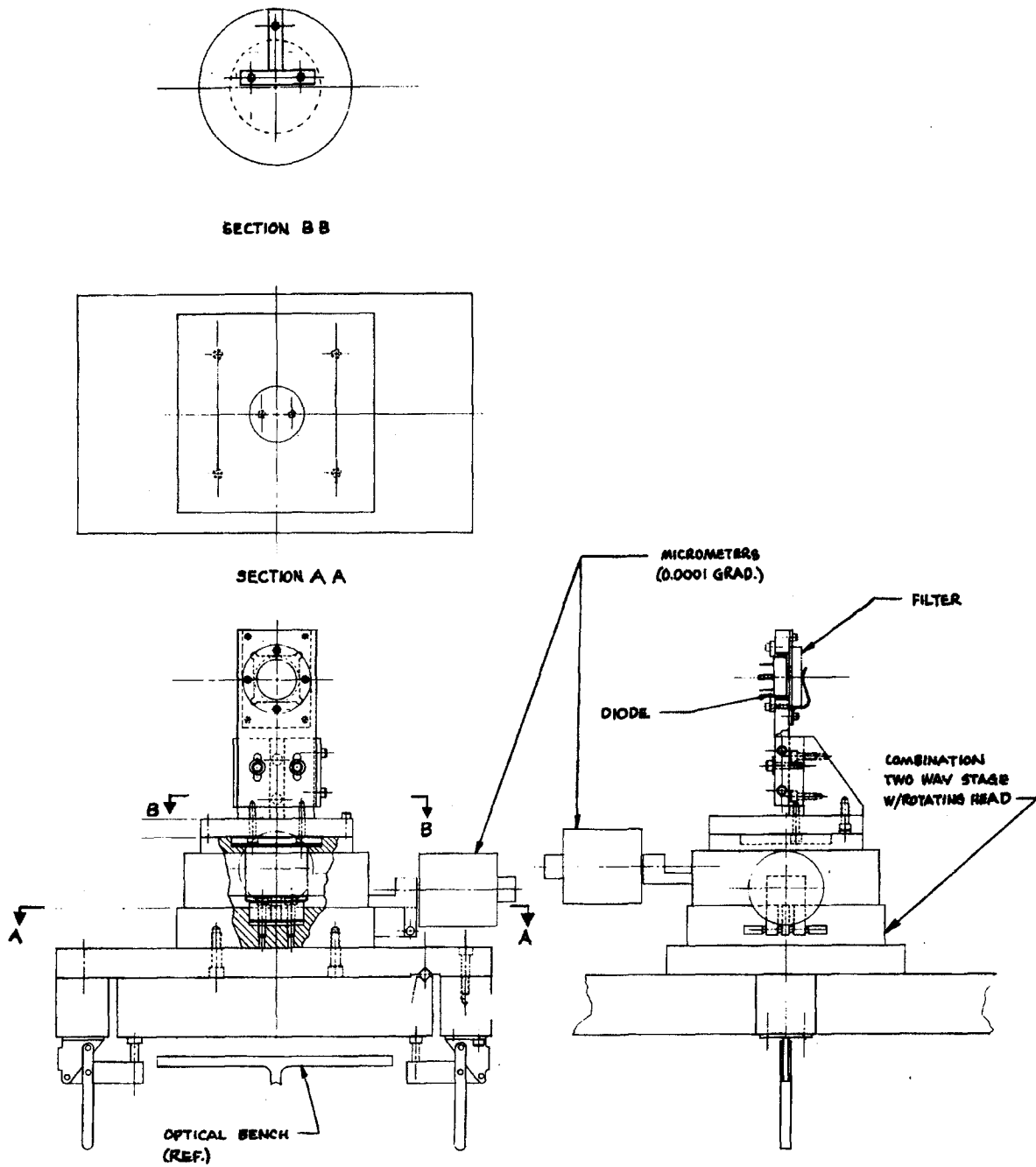


Fig. 3-7 — Focus sensor BB—double slit type (sheet 2 of 3, left end) (128737)

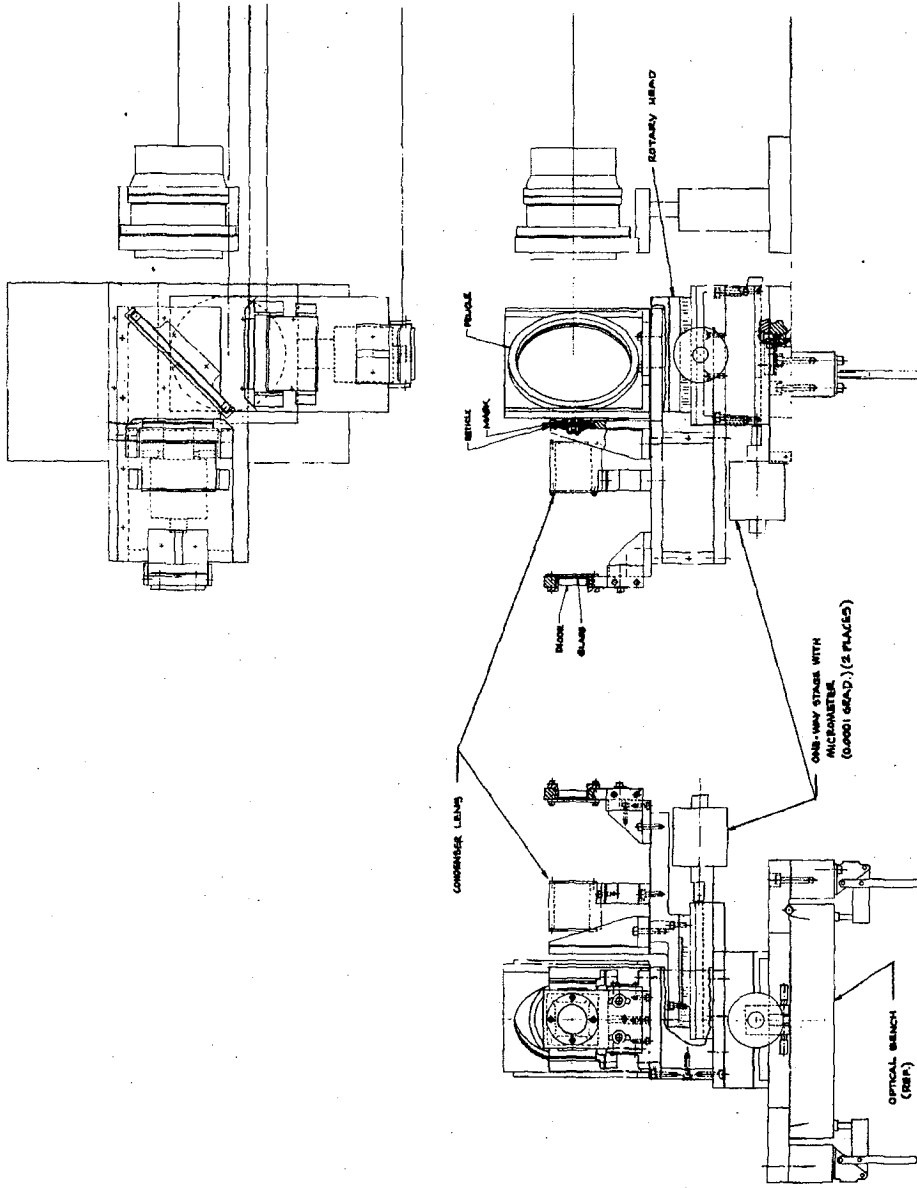


Fig. 3-8 — Focus sensor BB—reticle type and Foucault type (sheet 3 of 3)

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#### 4. CYLINDRICAL OPTICS

Fig. 4-1 shows a strip camera viewing in the side oblique mode. Differences in the vehicle-to-ground slant range within the field of view,  $\Delta\theta$ , of the camera produce an image motion which varies from one end of the slit to the other. The along-track axial image motion is given by

$$v_a = \frac{fv}{h} \cos \theta$$

Assuming a small field angle, the variation in velocity across the exposure slit,  $\Delta v_a$ , is given by

$$\Delta v_a = \frac{fv}{h} \sin \theta \Delta\theta$$

or the percent variation is given by

$$\frac{\Delta v_a}{v_a} = \tan \theta \Delta\theta = 1.9 \text{ percent}$$

for  $\theta = 45$  degrees and  $\Delta\theta = 1.08$  degrees. This velocity variation is intolerable for a high acuity strip camera. The method for correcting this velocity variation is to place an anamorphic optical system in front of the exposure slit.

##### 4.1 CYLINDER DESIGN

A cylinder pair was designed under a previous contract.\* Analytical and experimental evaluation of the design confirmed the performance of this cylinder pair over a 1-inch exposure slit width. The present contract calls for the design and test of an improved version of the cylinders. The improvements consist of (1) increasing the slit width to 2.3 inches, and (2) removing the "bias" magnification inherent in any two-element design.

In addition to the toroidal lens design program which previously was exclusively used for the cylinder design, Itek's zoom lens design program is now fully operational on the CDC-3300. The addition of the zoom program has greatly increased efficiency in the design of the cylinders because the cylinder tilt and displacement functions can be automatically determined, and automatic aberration correction under tilted conditions can be performed. Previously, this process was very laborious.

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\*See report no. 9416-67-011, "Feasibility Study for Dual Strip Camera."

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To date, the cylinder design effort has been concentrated on a three-element design. In addition, the design was optimized over the central 1-inch field. A scale drawing and characteristics of the best design effort to date appear in Fig. 4-2. Figs. 4-3 through 4-6 are ray traces of the design. All the traces are for a perfect  $f/7.0$ , telecentric input and a 1.0-inch slit width. The relationship of the exposure slit to the pupil is shown in the lower left corner of each trace. Tangential fans lie in the plane of the cylinder power. Sagittal fans lie in the plane perpendicular to the power; i.e., these fans see plane parallel plates in traversing the cylinders. Full field on each plot represents 0.5 inch off axis. Referring to Fig. 4-2, it can be seen that when the cylinders are untipped, only two aberrations are present—a slight amount of longitudinal color, and cylindrical field curvature of the sagittal fans. The longitudinal color is very small and entirely negligible in its effect on performance. The cylindrical field curvature of the sagittal fans is described below.

The sagittal fans encounter only plane parallel plates in traversing the cylinders. However, because there is power in the tangential plane, the equivalent plane parallel plate thickness changes quadratically with field height. The sagitta of this curve at a given field height,  $h$ , is given by:

$$\begin{aligned}\Delta h &= \frac{n-1}{n} \text{ (axial plate thickness minus plate thickness at } h\text{)} \\ &= \frac{(n-1)}{n} \frac{h^2}{2} \sum_i (C_{i1} - C_{i2})\end{aligned}$$

where  $C_{i1}$  = curvature of the first surface of the  $i$ th element  
 $n$  = refractive index  
 $h$  = field height

For the case of 0.5 inch off axis

$$\begin{aligned}\Delta_{0.5} &= \frac{(1.5-1)}{(1.5)} \frac{(0.5)^2}{2} (0.122 - 0.130 - 0.092 + 0.048 + 0.010 + 0.072) \\ &= 0.0013 \text{ inch}\end{aligned}$$

as is discussed in report no. 9416-67-011, Appendix A.

Figs. 4-4, 4-5, and 4-6 are ray traces of the design under fully tipped conditions ( $\pm 1$  percent magnification variation). These traces show that there is very little change in the aberration from the untipped condition. Sagittal fans are identical. The change in the tangential fans consists only of a slight disturbance to the color correction and the addition of some coma because the cylinders are tipped. Performance under tipped conditions is far superior to that obtained with any previous two-element design.

The bias magnification which was inherent in the two-element design has been successfully removed. The residual is 0.001 percent as compared with 3 percent for the two-element design.

#### 4.2 TEST AND MANUFACTURING PROGRAM

The test program for the cylinders will include:

1. Resolution measurements over the format with a telecentric,  $f/7.0$ , near perfect input beam

2. Measurement of the local magnification over the format to verify the predicted magnification variation and the absence of any bias magnification
3. Distortion measurement.

To accomplish this, a test fixture very similar to that used to test the two-element cylinder set (see report no. 9416-67-011) is being fabricated. The only changes required are the holder for the additional element and a slight modification to accommodate the increased format size.

The manufacture of the improved version of the cylinders is slightly more difficult than for the two-element set because both surfaces of each element have power and are larger in the along-track dimension. However, no problems are anticipated because even though more care is required in manufacture, the technology required is basically the same as was required for the two-element set.

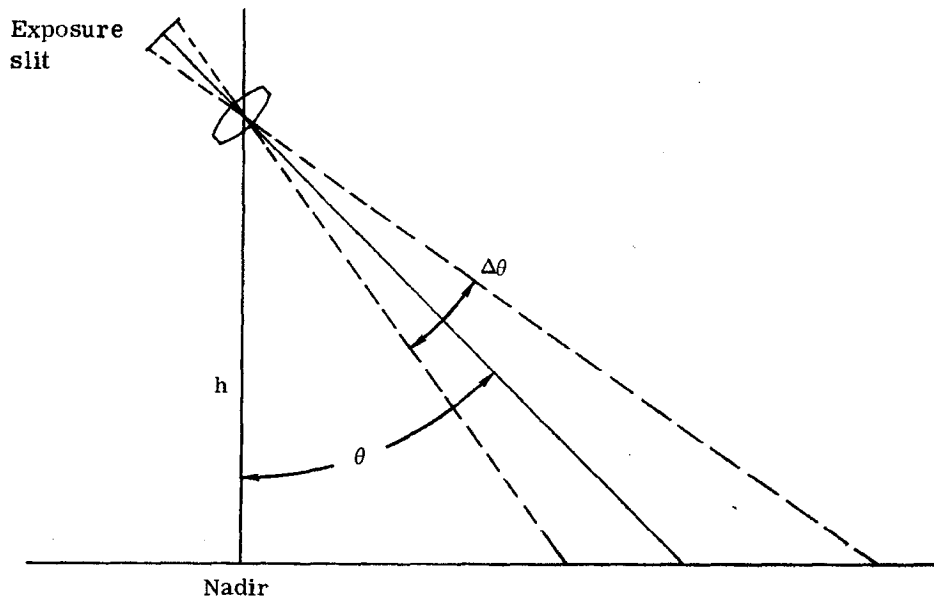
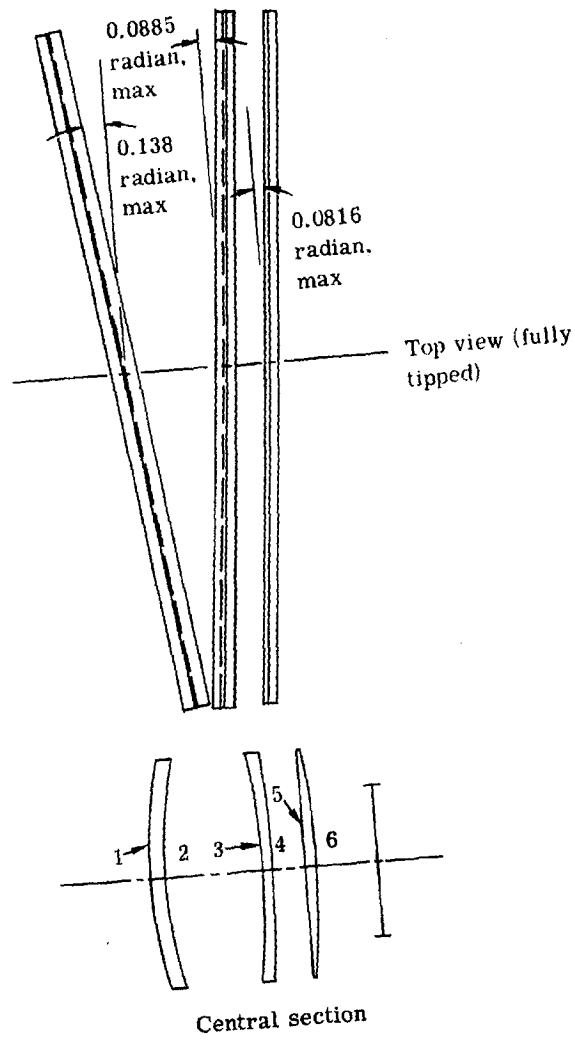


Fig. 4-1 — Side oblique viewing mode

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CONTROL SYSTEM  
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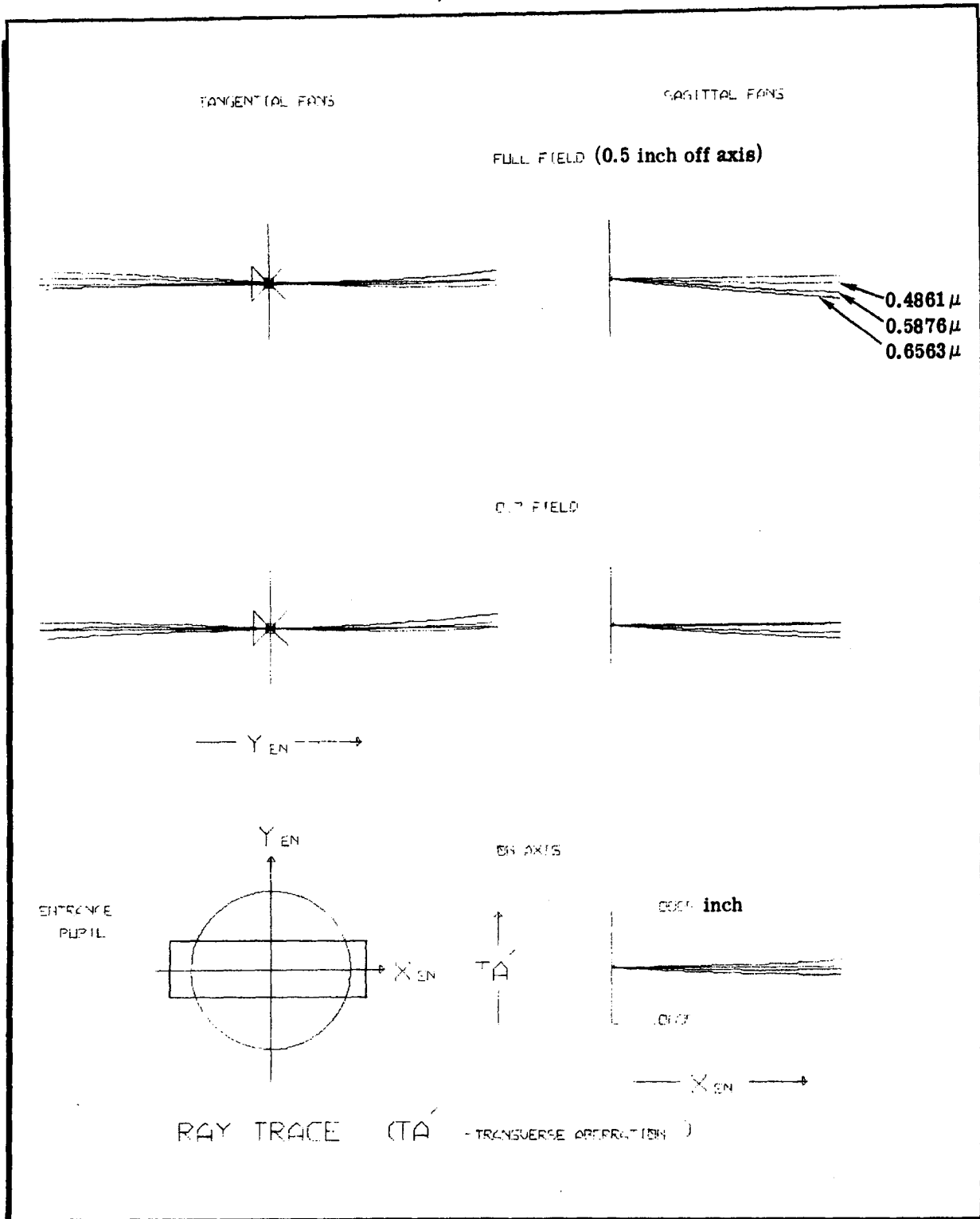
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Surface No.	Radius, inches	Thickness, inches	Medium
1	8.190	0.2202	BK-7
2	7.704	1.5696	Air
3	-10.814	0.1404	BK-7
4	-20.666	0.4821	Air
5	98.5113	0.1510	BK-7
6	-13.879	0.901	Air

Fig. 4-2 — Cylindrical optics

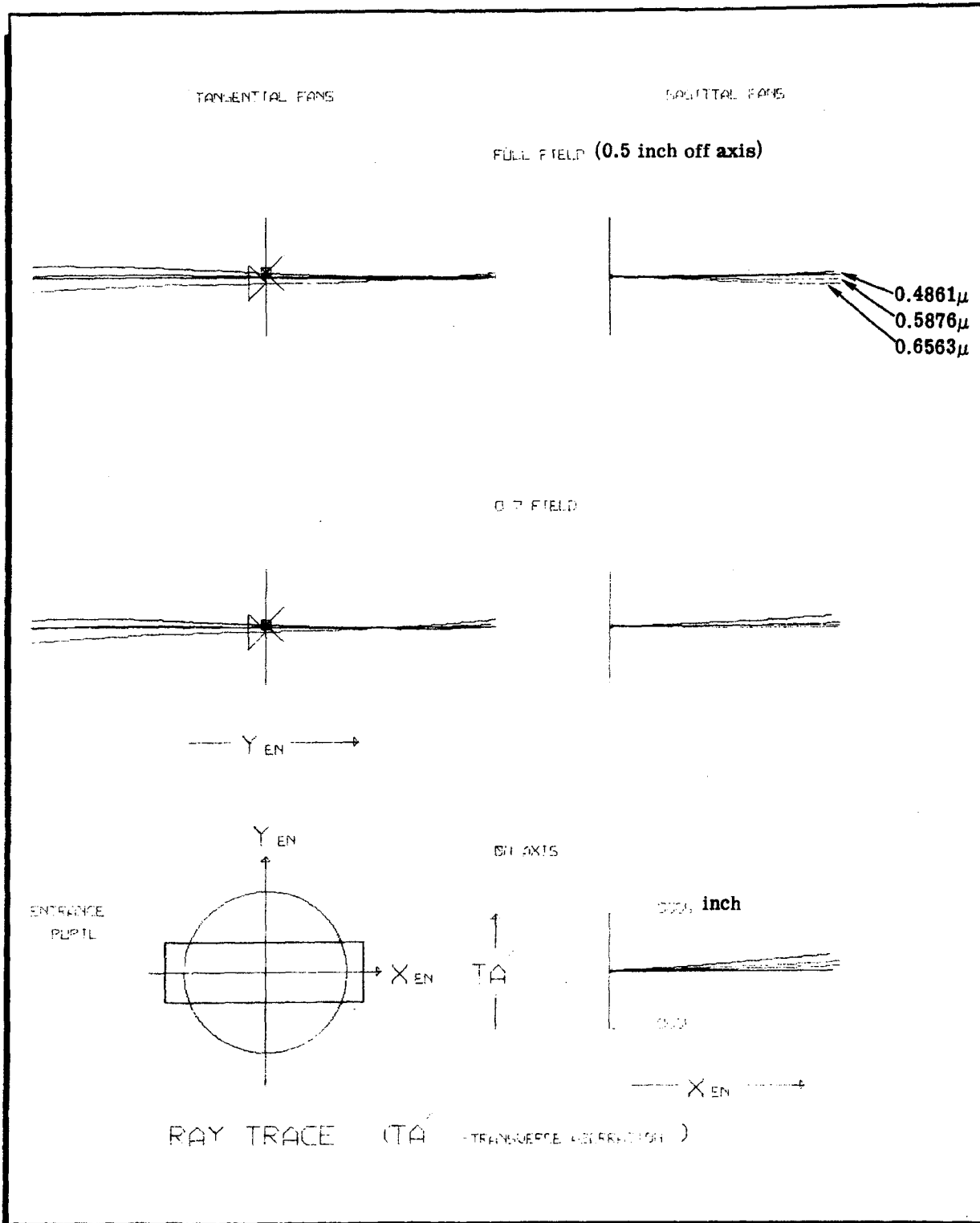
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REPRODUCTION OF ORIGINAL DATA

Fig. 4-3 — Ray trace of three-cylinder design, plus or minus 0.0 percent case

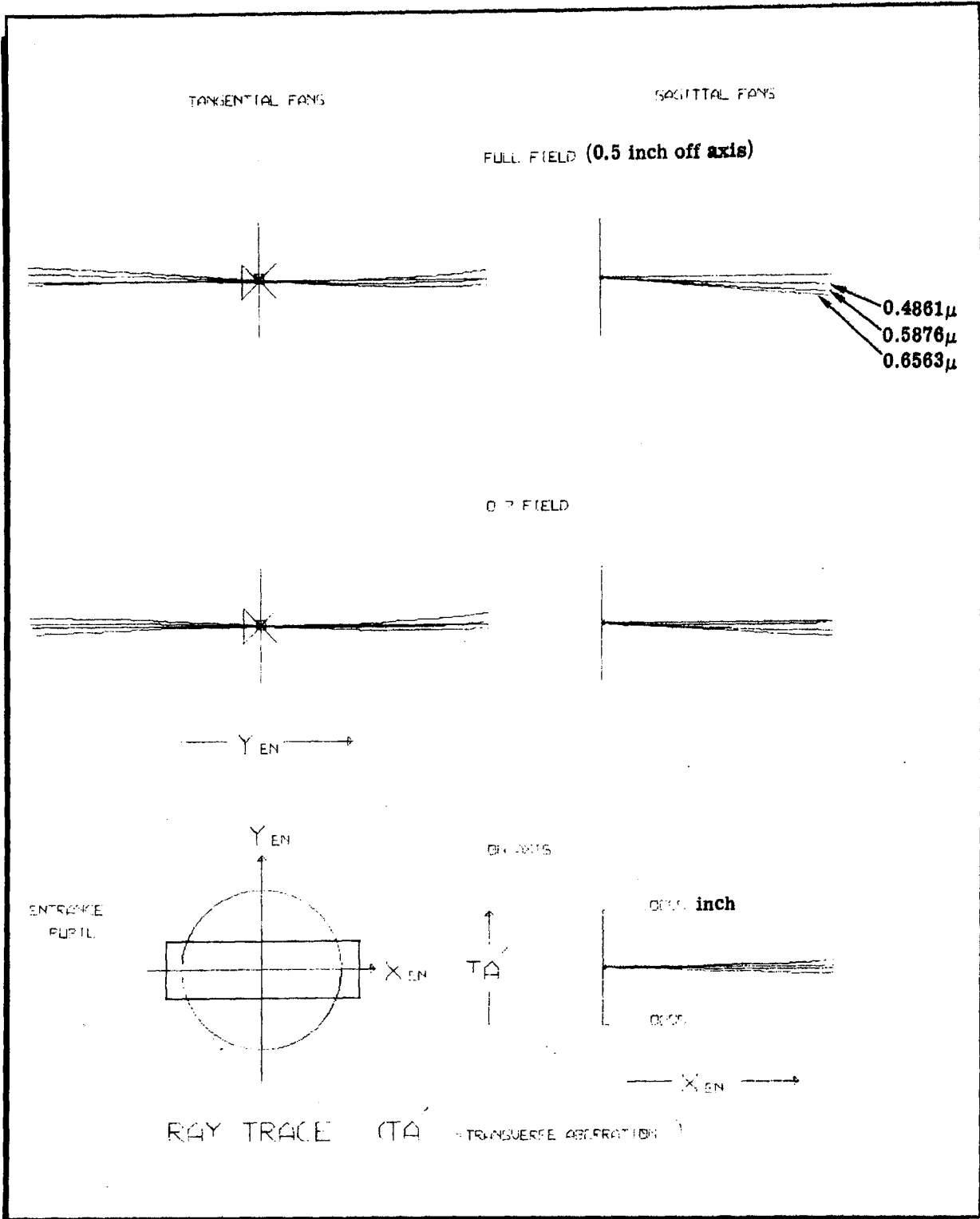
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REPRODUCTION OF ORIGINAL DATA

Fig. 4-4 — Ray trace of three-cylinder design, plus or minus 1.0 percent case, 0.99 magnification position



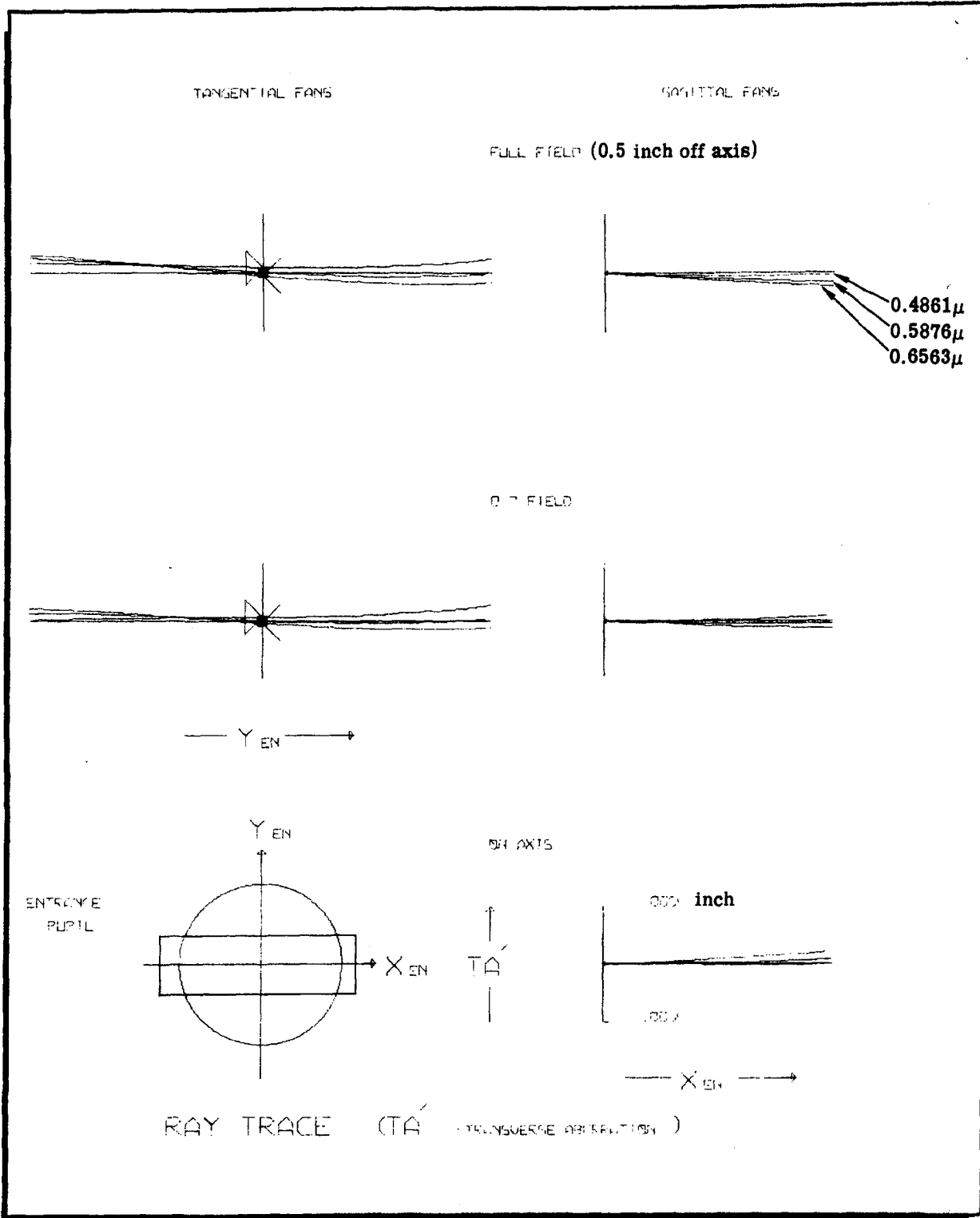


REPRODUCTION OF ORIGINAL DATA

Fig. 4-5 — Ray trace of three-cylinder design, plus or minus 1.0 percent case, 1.0 magnification position

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REPRODUCTION OF ORIGINAL DATA

Fig. 4-6 — Ray trace of three-cylinder design, plus or minus 1.0 percent case, 1.01 magnification position

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