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PRELIMINARY

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REAPER ENGINEERING ANALYSIS REPORT

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29 ~~January~~ DEC 1967

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Figure 1.1-1. Reaper System

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1.0 INTRODUCTION

1.1 Scope

This report describes the engineering development of an electromagnetic reconnaissance system, designated "Reaper." The subject matter is organized in the following manner. First, a system description and analysis presents the details of system development. System components are then described. Design analyses in the areas of mechanical design, radio-frequency interference, test, and reliability follow the component descriptions. Ground support test equipment is described in general terms.

Previously published analyses are not included in this report. Reference is made to Technical Description Report for Setter IB System, Document No. 52000-R378, dated 10 January 1967 for information relative to previously developed systems.

Figure 1.1-1 illustrates system hardware.

1.2 Summary

Reaper is an advanced electromagnetic-emitter locating system designed to be operated from an earth-orbiting platform. The equipment mates with an Agena vehicle and system interface is compatible with Payload Vehicle Digital Command Programmer, Type 20, as defined by LMSC Specification No. AA11654-3.

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Normal dwell time is such that emitters in general service are analyzed four times in the time required for the system field-of-view to pass over a target. The number of emitters and the duration of the emitter pulse repetition interval determine whether a 2-, 3-, or 4-pulse analysis will be made.

Two major modes of operation are provided. The electronic order-of-battle mode provides emitter direction-finding and parameter measurements of frequency, pulse width, pulse repetition interval and pulse amplitude. The technical-intelligence mode provides specific comparisons of processed data to stored data, enables a stop-scan condition, and supplies a pre-detected output for analog recording.

Frequency range of the system is from 1800 MHz to 3300 MHz. Frequency sampling is accomplished in increments of 2.5 MHz.

Two dwell modes are provided. In the normal dwell mode, four successive pulses with an interval of 5.28 ms or less are processed in a single dwell time. Normal dwell time is such that at least two "looks" are completed in the time required for the system field of view to pass over a target.

An alternate dwell mode provides a dwell time twice that of the normal mode. The long dwell time enables analysis of special emitters which have long pulse repetition times.

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The system operates at an altitude of 268 nautical miles and an orbit inclination of 75°. Vehicle orientation is such that the Y-axis of the field-of-view is in the direction of flight. Under normal flight conditions, the cross-track field-of-view is at least 160 nautical miles wide and the in-track field-of-view is large enough to provide two scans of each target in normal target density environments.

Orbital lifetime of the system is six months under normal programming conditions. Normal programming consists of 90 hours of intermittent operation, maximum, per month with a 30-minute, maximum, operating period per orbit.

2.0 SYSTEM DESCRIPTION

The Reaper system is an advanced electromagnetic emitter location system designed to be operated from an orbiting platform as part of the Strawman payload. The system is principally a precision direction-finding payload with the added capability of precise measurement of the emitter pulse parameters of frequency, pulse width, pulse repetition interval, and pulse amplitude. The system's normal Electronic Order of Battle (EOB) capability is further enhanced by a programmable technical intelligence (TI) capability.

2.1 EOB Functions

The system gathers parameter data on electromagnetic signals recieved over the RF range of 1800-3300 MHz, processes the data into digital form and transfers it to a core storage unit in the payload vehicle. The following paragraphs describe the exact frequency coverage, receiver sensitivity, ground coverage, signal processing and confirm-inhibit criteria. A block diagram of the system is shown in Figure 2.1-1.

2.1.1 Frequency Coverage

2.1.1.1 Normal Scan

The system local oscillator is sequentially stepped through the RF range in 2.5 MHz steps from the low frequency limit to the high frequency limit. Digital logic circuitry controls the stepping (scanning) and causes the receiver to dwell at each step for a certain period of time. During each

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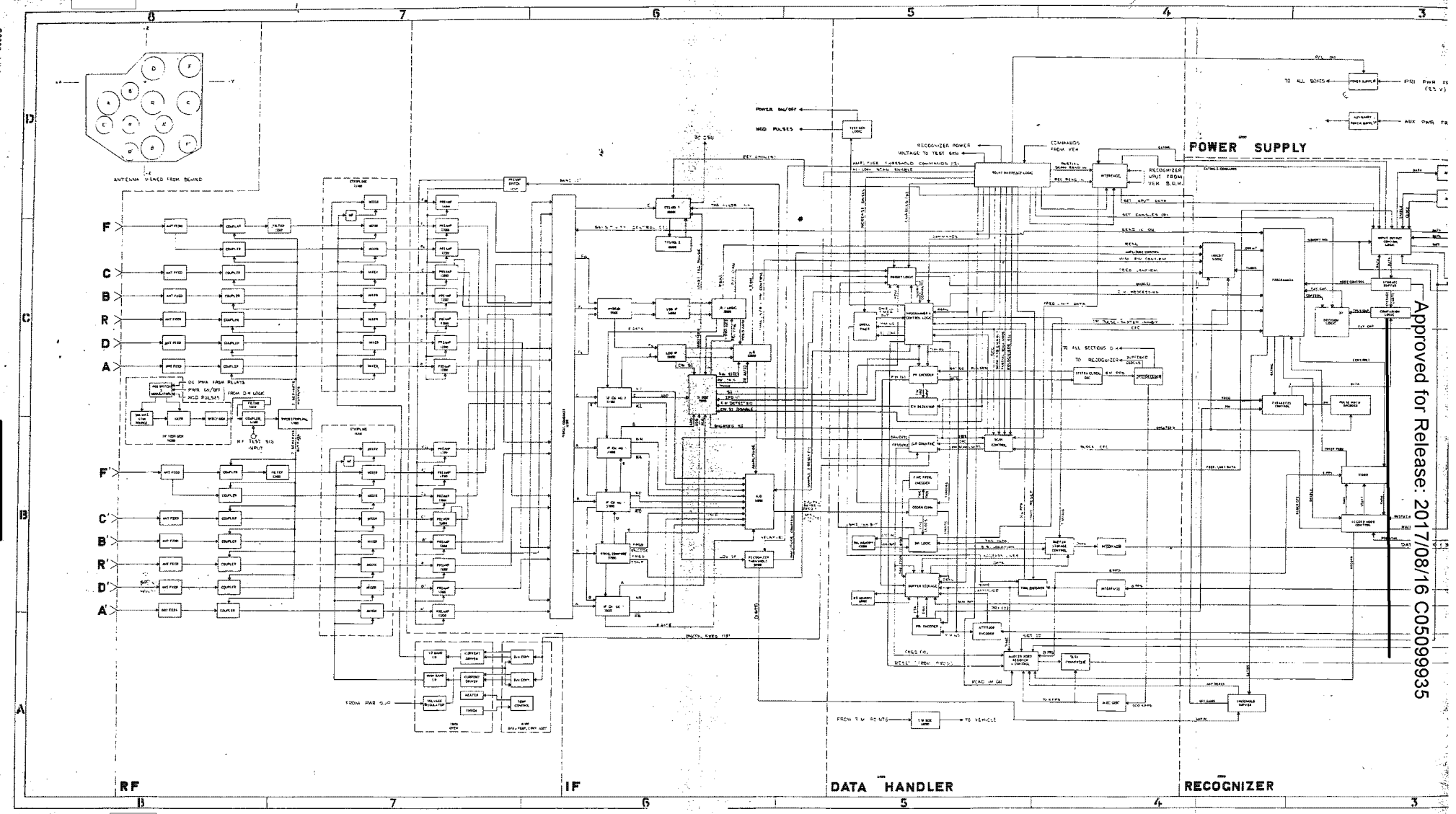

FIGURE 2.1-1. SY

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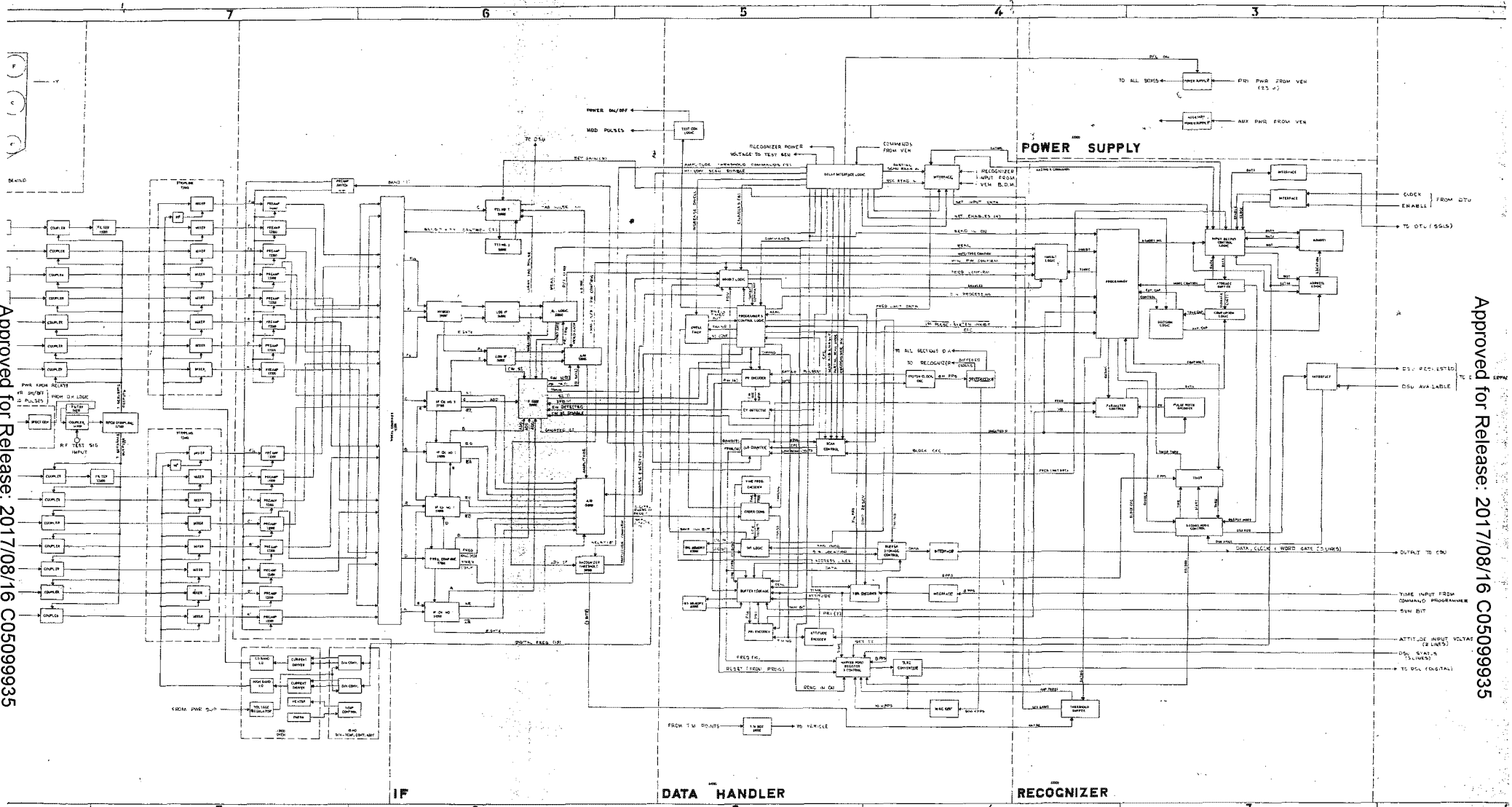

FIGURE 2.1-1. SYSTEM BLOCK DIAGRAM

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dwell period, the system accepts and processes those signals which meet the confirm-inhibit criteria described in paragraph 2.1.4. The resulting RF coverage is shown in Figure 2.1-2.

The dwell period at each frequency step is a function of the number of received signals. If no confirmed signals are received in the basic dwell period (search time) of 6.14 milliseconds, the local oscillator is moved to the next higher step and a new dwell started. If a confirmed signal is received during the search time, the dwell is lengthened to 22.5 milliseconds to allow additional pulses to be processed.

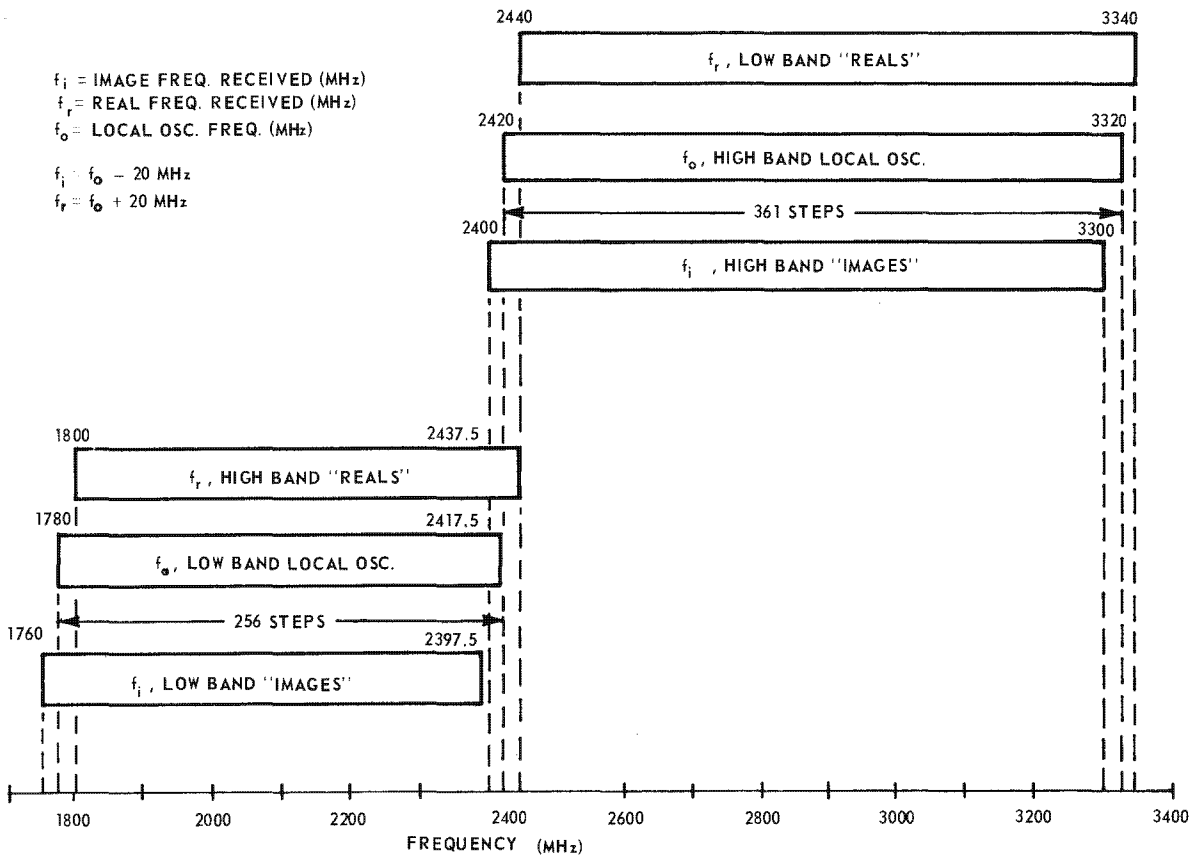

FIGURE 2.1-2 FREQUENCY COVERAGE

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The variation in dwell time results in a variable scan time to cover the RF range. Figure 2.1-2 shows the variation in scan time as a function of the number of steps yielding at least one confirmed pulse. An alternate dwell mode is available by command with a search time of 22.5 milliseconds extended to 45 milliseconds with a confirmed pulse. The scan time resulting from the alternate dwell is also shown in Figure 2.1-3.

2.1.1.2 Partial Scan

An alternate frequency scan mode is available, by command, to allow covering only one or two segments of the RF range and not scanning the remainder. The segment limits are stored in a memory and can be reprogrammed on orbit. Any two segments of the "real" range shown in Figure 2.1-2 can be selected in the partial scan mode, within the restrictions given in paragraph 2.3.1.1.5.

2.1.2 Ground Coverage

The system sorts signals by location and only accepts for Electronic Order of Battle (EOB) processing those from locations within a rectangular field-of-view centered about the vehicle nadir. The field-of-view varies in size with signal frequency as illustrated in Figure 2.1-4. As shown in the illustration, the rectangular field-of-view is surrounded by an inhibit circle which prevents EOB processing of signals received from large angles off the vehicle vertical axis. Either function can be selected by command.

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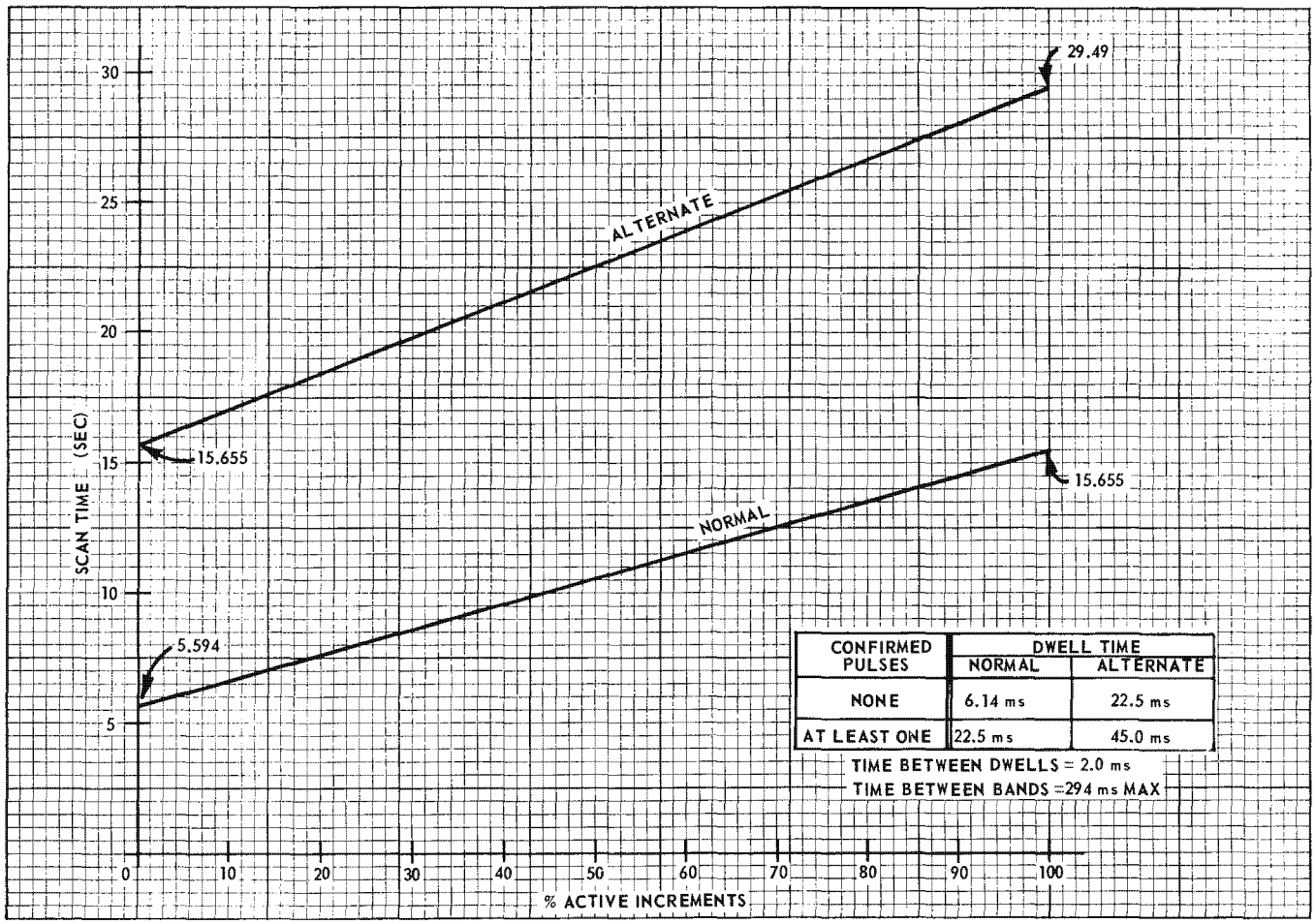

FIGURE 2.1-3 SCAN TIME

2.1.3 Sensitivity

Figure 2.1-5 shows the typical minimum effective radiated power required for EOB processing as a function of distance from the nadir. This value can be adjusted downward (less sensitive) in two 5-db steps by command.

2.1.4 Signal Processing

2.1.4.1 Processing Sequence

During a dwell period, if a signal (pulse or CW)

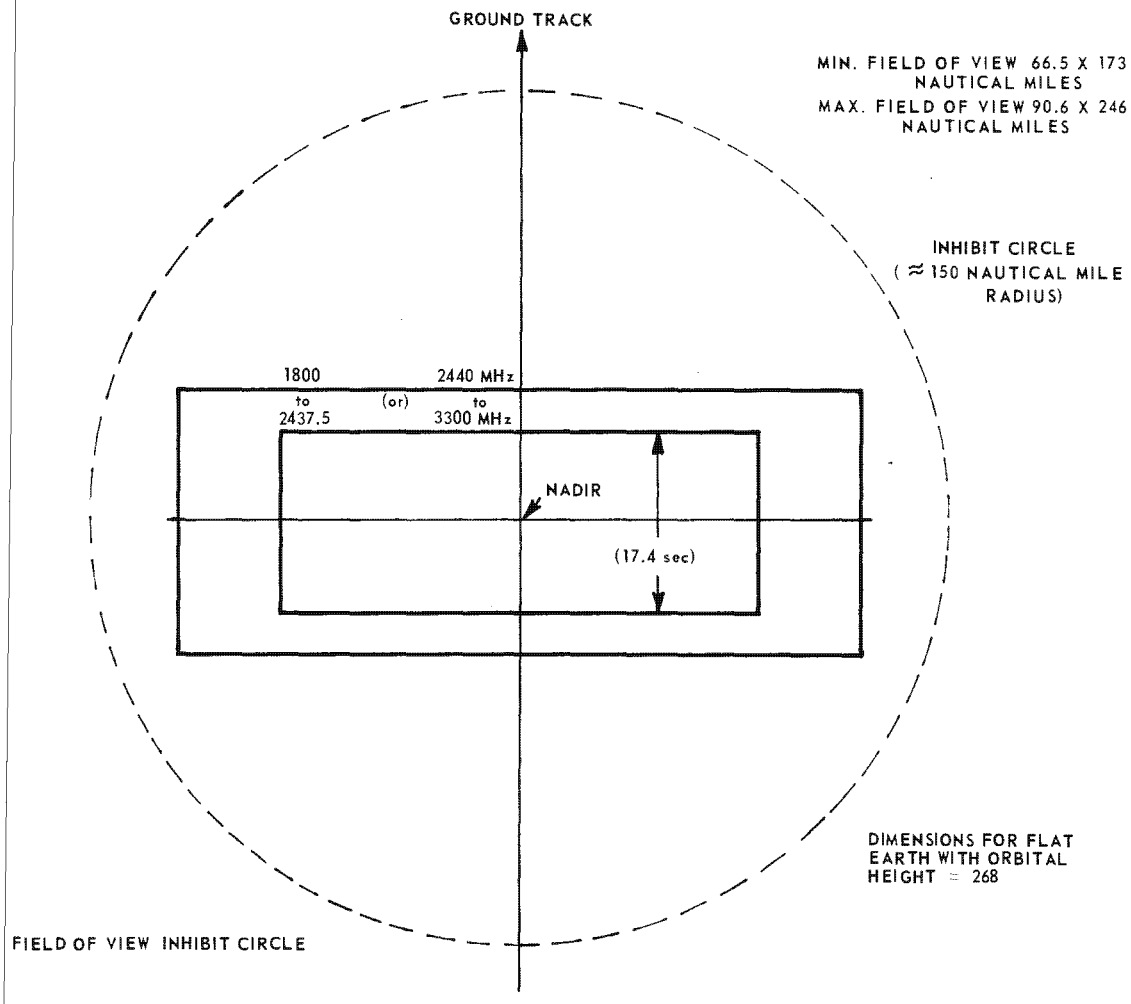

FIGURE 2.1-4 FIELD-OF-VIEW INHIBIT CIRCLE

is detected above the processing threshold, analog measurements of the signal amplitude, frequency, width, repetition rate and angle of arrival are initiated, and digital processing begins. Encoding of the analog data proceeds while the confirm-inhibit decisions are made to establish that the signal is one for which output data is desired. When the analog measurements are completed, the associated circuitry is blanked from accepting further signals until digital processing is com-

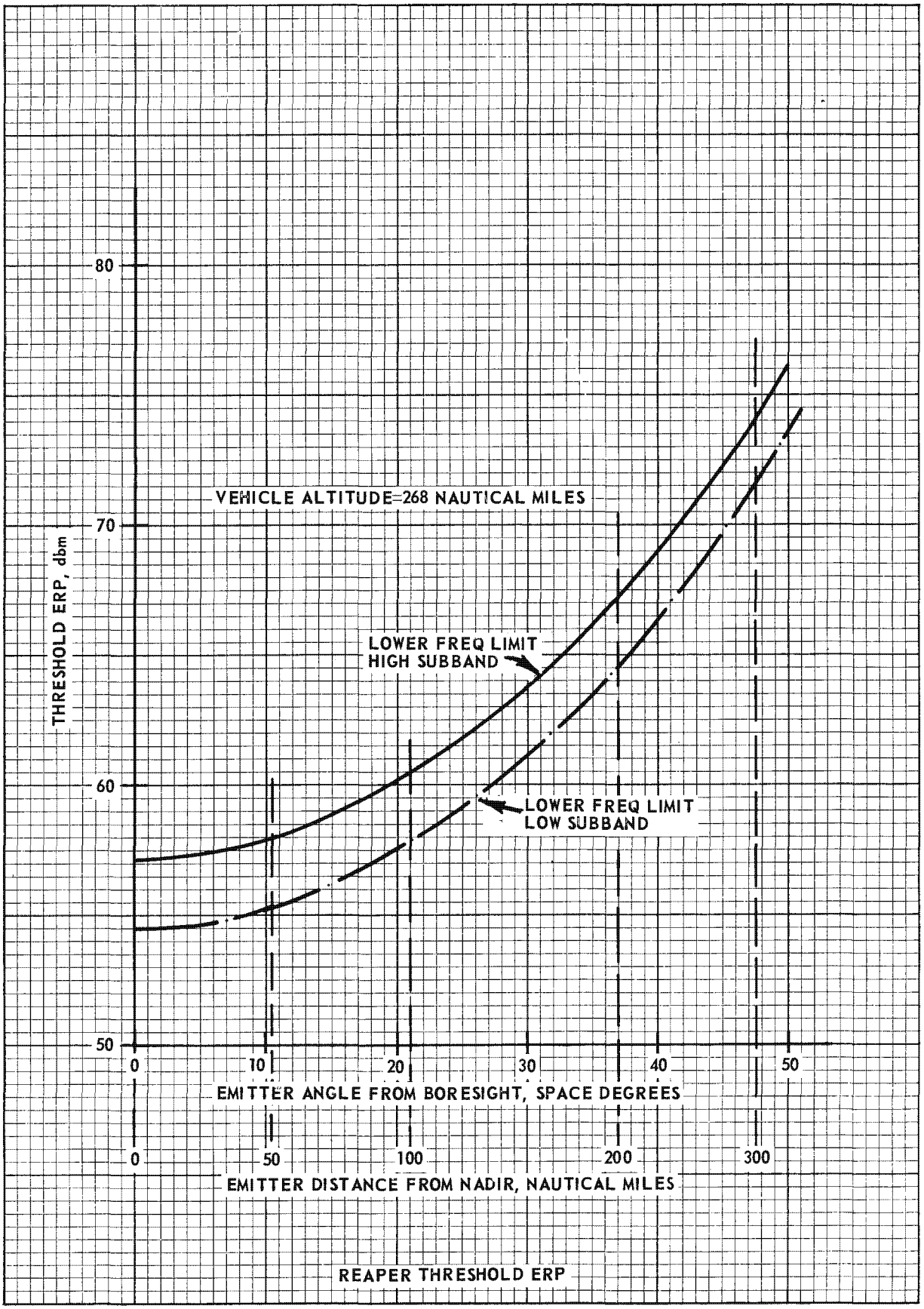

FIGURE 2.1-5 THRESHOLD ERP

If an inhibit decision is made, digital processing stops, the digital circuitry is reset, the analog circuitry unblanked and the dwell continues. If the signal is not inhibited, the set of measured data is temporarily stored in a memory while other signals are processed.

If two, three, or four sets of data are taken from the same location during a dwell, the sets are grouped into a digital word and transferred to the vehicle storage. If only one set of data is taken on a signal, the data is discarded.

CW signals are processed by automatically resetting when the "pulse width" is measured and found to be greater than 24 microseconds. Pulse signals can be detected in the presence of CW by an automatic threshold adjustment which allows the pulse to be processed if it is at least 15 db above the CW level.

2.1.4.2 Confirm-Inhibit Decisions

The following functions are accomplished on each detected signal to eliminate undesired data and inaccurate measurements. Each of these functions can be separately disabled by command.

a) Minimum Threshold Confirm - Establishes that the signal being processed is above the minimum amplitude level required for accurate parameter measurements.

b) Frequency Confirm - Establishes that the signal is within the center portion (20 $\pm$ 1.5 MHz)

of the receiver IF bandwidth.

c) Real/Image Confirm - Establishes that the signal is a real or that it is an image.

d) Minimum Pulse-Width Confirm - Establishes that the signal duration is equal to or greater than 0.4 microseconds.

e) Pulse-Count Inhibit - Allows a target from a particular direction to be processed only four times (four pulses) during a dwell.

f) Field-of-View Inhibit - Limits signal processing to those signals received from within the rectangular field of view.

g) Amplitude-Ratio Inhibit - Inhibits processing of signals arriving at large angles off boresight.

2.2 Technical Intelligence Functions

The system can be commanded to operate in a recognition mode while operating in parallel with the normal EOB processing. The purpose of the recognition mode is to detect and identify signals having parameters within certain ranges and interrupt the frequency scan to enable predetection recording of these signals on the vehicle DSU. In the recognition mode, basic operation is controlled by the EOB frequency scan. No change in normal EOB operation takes place until a signal is recognized.

2.2.1 Recognition Mode Signal Processing

At each frequency step (dwell), signals being processed by the EOB circuitry are also processed by the recognition circuitry. The EOB confirm-inhibit decisions of paragraph 2.1.4.2 are used to limit the amount of data available for recognition. The amount of data is restricted further by an additional minimum amplitude threshold which is commandable to one of four positions always at or above the EOB minimum threshold. Data from signals which meet the confirm-inhibit requirements are compared to parameter data stored in a P/L memory. The parameter data consists of eight sets with each set containing the information shown in Table 2.2-1. Each set is separately enabled by command and the entire memory contents can be reloaded in flight.

TABLE 2.2-1 RECOGNIZER SET DATA

	LSB	Limits	No. of Bits
Horizon or FOV mode:	-	-	1
Signal Parameters:			
Frequency	5 MHz	1,800 MHz	9
		3,300 MHz	9
Pulse Width	250 nsec.	0.4 usec	4
		4 usec	4
PRI	64	100 usec	7
		8,192 usec	7
Record Mode:			3

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Signal data is compared sequentially to parameters from each of the enabled stored sets. If a set is enabled in the horizon-to-horizon mode, only frequency ("reals" only) and pulse width are compared. In the field-of-view mode, pulse repetition interval is also compared. If a match is achieved between stored and measured data, the EOB scan operation is interrupted and the output mode specified in the matched set's data is executed. Table 2.2-2 shows the six output modes which can be selected.

TABLE 2.2-2 RECOGNIZER OUTPUT MODES

MODE	WAIT TIME*	RECORD TIME
1	0	2 SEC
2	0	4 SEC
3	0	8 SEC
4	60 SEC	4 SEC
5	60 SEC	8 SEC
6	60 SEC	300 SEC

*If DSU not available.

2.2.2 Predetected Signal Output

A predetected signal output is available at the vehicle interface for analog recording. The predetected signal preserves the RF signal characteristics within the limitations of the local oscillator and receiver bandwidth. The amplitude response is automatically adapted when a recognition

is achieved to fit the matched signal's amplitude into the vehicle recorder's useful dynamic range as shown in Figure 2.2-1. Two reference tones (46.875 kHz and 6.0 MHz) are added to the predetected output. Each signal not generating an amplitude ratio inhibit is followed by a tag pulse as a coarse sorting aid. Figure 2.2-2 illustrates the predetected bandwidth, tones and tag pulse characteristics.

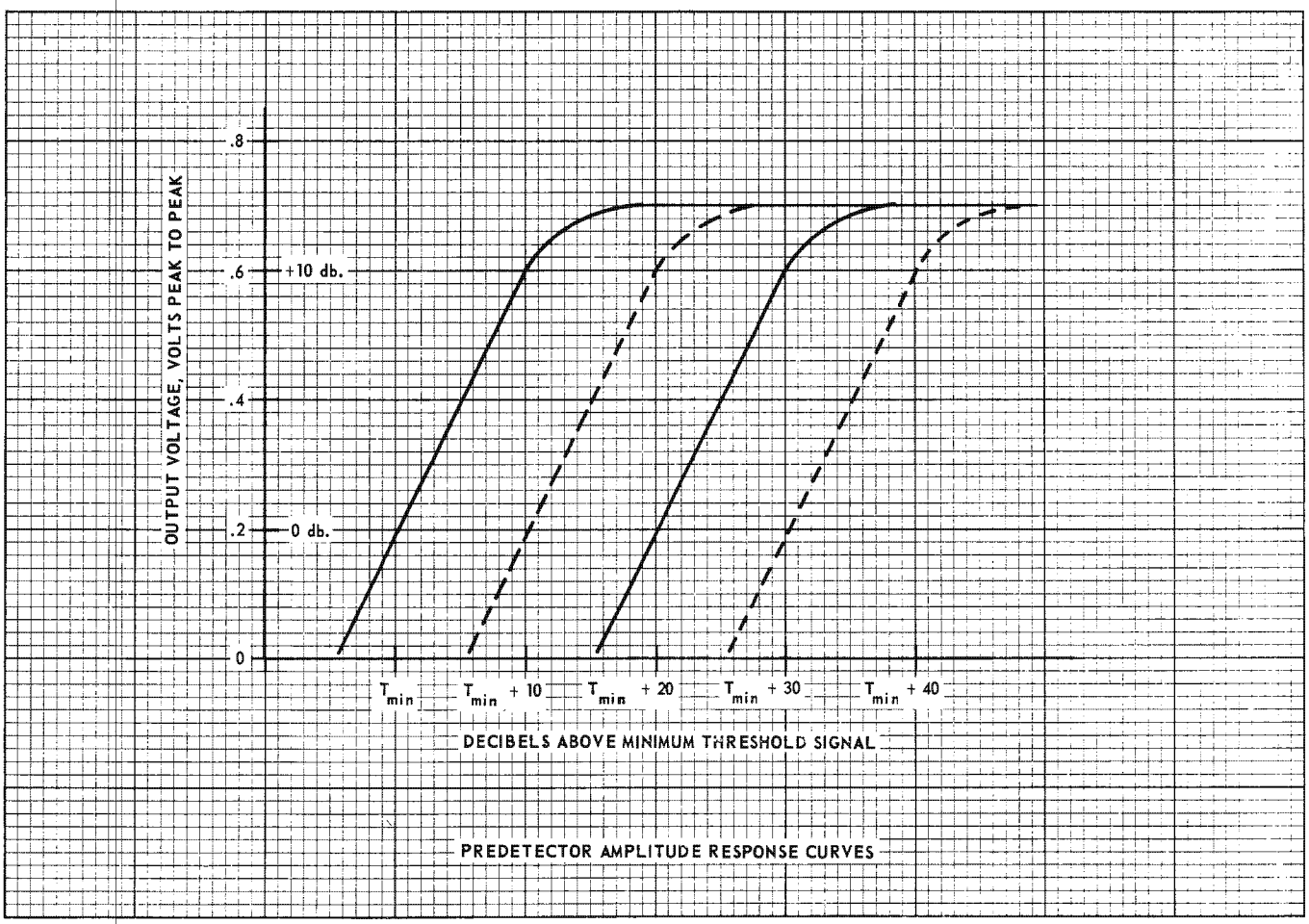
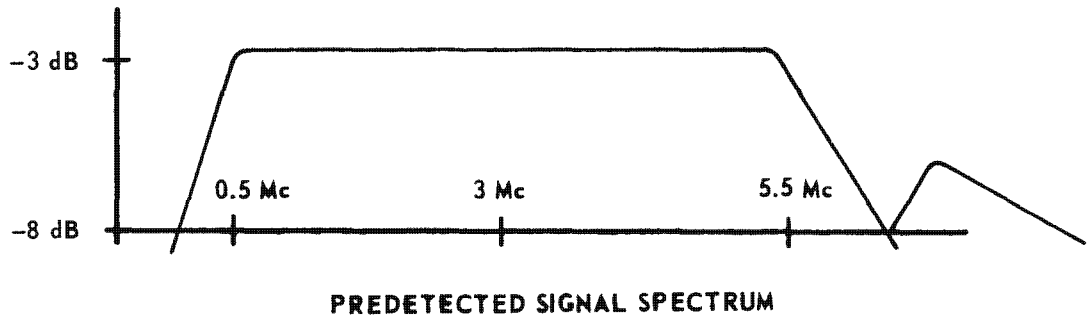
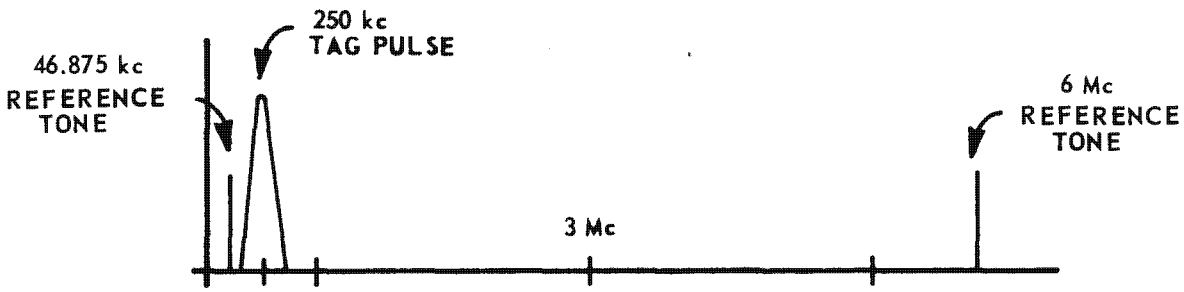


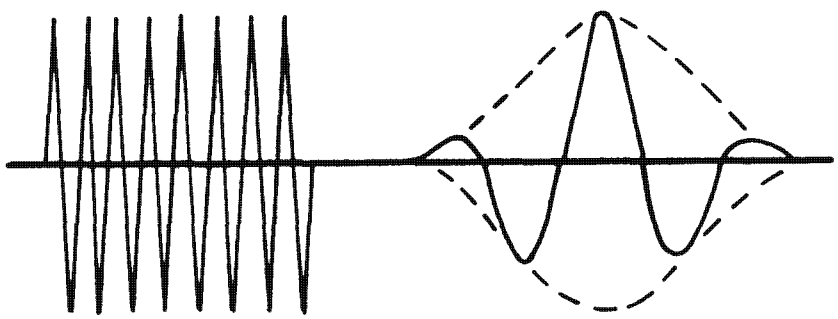
FIGURE 2.2-1 PREDETECTOR AMPLITUDE RESPONSE CURVES 50X1



PREDETECTED SIGNAL SPECTRUM



REFERENCE TONES & TAG PULSE SPECTRUM



3 Mc PREDETECTED SIGNAL TAG PULSE

FIGURE 2.2-2 PREDETECTOR SIGNAL CHARACTERISTICS

2.2.3 Marker Word

Digital marker words are output to the digital channel of the vehicle analog recorder to aid in sorting and identifying predetected signals. The marker words are generated at the rate of 8 per second synchronized to the vehicle clock and are output during the recording time after a match, or if the vehicle recorder is actuated. The marker word contains the data described in paragraph 2.4.2. The "Amplitude Threshold" data specifies the predetected signal's amplitude characteristics (refer to Figure 2.2-1), the "Set ID" identifies the stored set matched, and the "Frequency" corresponds to the local oscillator frequency.

2.3 Operation

This section describes the system's operation in various commandable modes. The operational modes are summarized in Table 2.3-1. Table 2.3-4 contains a complete list of commands and associated "R" numbers. Tables 2.3-2 and 2.3-3 contain a brief summary of command restrictions. Each command function is described in detail below.

2.3.1 EOB Readin

The Reaper system's normal data processing mode is described as "EOB Readin." Operation is controlled and may be modified by command as described in the following paragraphs.

TABLE 2.3-1 OPERATIONAL MODES*

MODE	OPERATION
1.	Normal (EOB) Data Processing "EOB READIN"
2.	Normal (EOB/TI) Data Processing "EOB/TI READIN"
3.	Recognizer Memory Load
4.	Partial Scan Memory Load
5.	Memory Readout

*All operate mode commands, R13, R49, R61, R51, must be mutually exclusive.

TABLE 2.3-2 COMMAND RESTRICTION SUMMARY

Function	Command
Partial Scan "A" On/Off	(R3/R4)
Partial Scan "B" On/Off	(R59/R60)
Disable Upper Frequency Band	(R15)
Disable Lower Frequency Band	(R16)
Enable Upper & Lower Frequency Band	(R17)
Disable Memories (SWI & Buffer)	(R18)
Reset for Commands R18-R25	
IF Memories Have Been Disabled	(R26)
Recognizer Enable/Disable	(R9/R10)

TABLE 2.3-3 COMMANDS WITH NO RESTRICTIONS

Function	Commands
Increase/Decrease Dwell Time	(R1/R2)
Disable FOV	(R19)
Disable T_{min} Confirm	(R20)
Disable T_{max} Inhibit	(R21)
Disable A/R Inhibit	(R22)
Disable Real/Image Confirm	(R23)
Disable Minimum PW Confirm	(R24)
Disable Frequency Confirm	(R25)
Enable/Disable CW-SI Ckt.	(R27/R28)
Time Reset	(R58)
Enable/Disable Recognizer Buffer	(R30/R29)

2.3.1.1 EOB Readin Command Functions and Restrictions

2.3.1.1.1 Payload On (R11)

Function - This command actuates the system primary power supply to supply power supply to supply power to all circuits not supplied from the auxiliary power supply. Recognizer Enable (R9) must be issued to supply power to recognition circuits.

Restrictions - All operate modes (Readin, Recognizer input, Partial Scan Input, and Recognizer Partial Scan Readout) shall be disabled before

TABLE 2.3-4. SYSTEM COMMANDS

COMMAND	FUNCTION	COMMAND	FUNCTION
R1	Increase Dwell Time	R29	Disable Recognizer Buffer
R2	Decrease Dwell Time	R30	Enable Recognizer Buffer
R3	Partial Frequency Scan A On	R31	Enable RF Calibrator
R4	Partial Frequency Scan A Off	R32	Disable RF Calibrator
R5	Threshold Control A	R33	Enable Set A
R6	Threshold Control $\overline{A}$	R34	Disable Set A
R7	Threshold Control B	R35	Enable Set B
R8	Threshold Control $\overline{B}$	R36	Disable Set B
R9	Recognizer Enable	R37	Enable Set C
R10	Recognizer Disable	R38	Disable Set C
R11	Payload On	R39	Enable Set D
R12	Payload Off	R40	Disable Set D
R13	Readin On	R41	Enable Set E
R14	Readin Off	R42	Disable Set E
R15	Disable Upper Frequency Band	R43	Enable Set F
R16	Disable Lower Frequency Band	R44	Disable Set F
R17	Enable Upper & Lower Frequency Band	R45	Enable Set G
		R46	Disable Set G
R18	Disable Memories	R47	Enable Set H
R19	Disable FOV Inhibit	R48	Disable Set H
R20	Disable Tmin Confirm	R49	Enable Recognizer Input Mode
R21	Disable Tmax Inhibit		
R22	Disable A/R Inhibit	R50	Disable Recognizer/Partial Scan Input Mode
R23	Disable Real/Image Confirm		
R24	Disable P.W. Confirm	R51	Enable Recognizer/Partial Scan Readout
R25	Disable Frequency Confirm		
R26	Reset R18 through R25	R52	Disable Recognizer/Partial Scan Readout
R27	Disable C.W. - S.I.		
R28	Enable C.W. - S.I.	R53	Recognizer Threshold Bit A

TABLE 2.3-4. SYSTEM COMMANDS (CONT'D)

COMMAND	FUNCTION	COMMAND	FUNCTION
R54	Recognizer Threshold Bit B		
R55	Spare		
R56	Spare		
R57	Spare		
R58	Time Reset		
R59	Partial Scan B On		
R60	Partial Scan B Off		
R61	Enable Partial Scan Input Mode		
R62	Recognizer Threshold Bit $\overline{A}$		
R63	Recognizer Threshold Bit $\overline{B}$		

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issuing R11. After issuing R11, a minimum delay of one second shall be provided before enabling the payload in any operate mode.

2.3.1.1.2 Payload Off (R12)

Function - P/L OFF Command deactuates the primary power supply.

Restrictions - All operate modes shall have been OFF for a minimum of 500 milliseconds before issuing Payload-OFF Command.

2.3.1.1.3 Increase Dwell Time (R1)

Function - Increase Dwell time causes the system to dwell for 22.5 milliseconds in frequency steps with no signal present and to dwell for 45 milliseconds in frequency steps with confirmed signals. This will increase the time required to scan the band. See Figure 2.1-3.

Restrictions - None.

2.3.1.1.4 Decrease Dwell Time (R2)

Function - Decrease Dwell Time causes the system to dwell for 6.14 milliseconds in frequency steps with no signal and for 22.5 milliseconds in frequency steps with confirmed signals.

Restrictions - None.

2.3.1.1.5 Partial Scan A ON (R3)

Function - This command modifies EOB Readin opera-

tion to provide a scan of part of the RF range based on limits stored in the partial scan memory for Partial Scan A.

Restrictions - Partial Scan A On shall not be issued while in the Readin Mode. Some caution is required to achieve correct operation with R3 issued if the upper or lower limit of Partial Scan A is near 2,440 MHz. For instance, if the upper limit of Partial Scan A is 2,435 MHz, only the lower RF range (See Figure 2.1-2, "reals" only) need be enabled. But, if the upper limit is 2,440 MHz, the upper RF range must also be enabled because that is the first (lowest) step in the upper range. Similarly, if the lower limit of Partial Scan A is 2,435 MHz, both the upper and lower RF ranges must be enabled. Refer to paragraph 2.4.3 for restrictions on the Partial Scan memory contents.

2.3.1.1.6 Partial Scan A OFF (R4)

Function - R4 resets R3 command.

Restrictions - R4 should not be issued while in the Readin Mode. Loss of Partial Scan memory contents or Data Handler lock up may result.

2.3.1.1.7 Partial Scan B ON (R59)

Function - This command provides a scan of Partial Band B based on limits stored in the partial scan memory.

Restrictions - Same as specified in paragraph 2.3.1.1.5.

2.3.1.1.8 Partial Scan B OFF (R60)

Function - R60 resets R59 command.

Restrictions - Same as for R4.

2.3.1.1.9 Threshold Controls (R5, 6, 7, and 8)

Function - These commands control the system threshold by switching in attenuators after the IF preamplifier. The following table specifies the system sensitivity (at the antennas, 23° off boresight) for a given command combination.

Sensitivity	Commands Issued*			
	A (R5)	$\overline{A}$ (R6)	B (R7)	$\overline{B}$ (R8)
-93 dbm	0	1	0	1
-88 dbm	0	1	1	0
-83 dbm	1	0	0	1

* 0 - not issued
1 - issued
All other combinations invalid.

Restrictions - The combination of R5 and R7 simultaneously or in sequence without R6 or R8 intervening will cause a loss of data.

2.3.1.1.10 Readin ON (R13)

Function - R13 enables the payload in the EOB Readin Mode. EOB Readin Mode operation will be as modified by additional commands such as Dwell Increase/Decrease, Partial Frequency Scans, Threshold Controls, Recognizer Enable, etc.

Restrictions - R13 shall not be commanded simultaneously with the memory load or readout modes. A minimum delay of 100 milliseconds is required between R13 and any other operate command.

2.3.1.1.11 Readin OFF (R14)

Function - R14 stops Readin Mode operation.

Restrictions - R14 shall occur a minimum of 500 milliseconds before R12 (P/L OFF). If the Recognizer is ON, then R14 shall be issued before Recognizer Disable (R10), and then R10 shall be issued before P/L OFF (R12).

2.3.1.1.12 Disable Upper Frequency Band (R15)

Function - R15 disables the high band and allows processing of the low band (1800 MHz to

2437.5 MHz) only.

Restrictions - R15 shall not be issued while in the Readin Mode.

2.3.1.1.13 Disable Lower Frequency Band (R16)

Function - R16 disables the lower frequency band and allows processing of the high band (2440 MHz to 3300 MHz) only.

Restrictions - R16 shall not be issued while in the Readin Mode.

2.3.1.1.14 Enable Upper & Lower Frequency Band (R17)

Function - R17 enables the full frequency range to be scanned normally.

Restrictions - R17 shall not be issued while in the Readin Mode.

2.3.1.1.15 Disable Memories (R18)

Function - The Disable Memories command disables the SWI Memory and the Buffer Storage Memory circuits in case of a memory failure. EOB Readin operation will continue with single-pulse confirm criteria.

Restrictions - Data will be lost if R18 is issued during Readin operation.

2.3.1.1.16 Disable FOV (R19)

Function - The Disable FOV command causes the system to ignore the rectangular field-of-view

inhibit-confirm and allows processing of signals out to the A/R inhibit circle during EOB Readin Operation.

Restrictions - None.

2.3.1.1.17 Disable Tmin (R20)

Function - The Disable Tmin Command allows the system to process signals below the minimum sensitivity level during EOB Readin operation. Information from these low level signals will be degraded.

Restrictions - None.

2.3.1.1.18 Disable Tmax (R21)

Function - The Disable Tmax Command allows the system to process signals above the receiver dynamic range. Data from these high level signals will be degraded.

Restrictions - None.

2.3.1.1.19 Disable A/R Inhibit (R22)

Function - The Disable A/R Inhibit Command allows the system to accept information that is outside the amplitude ratio circle. See Figure 2.1-4. Location information may be degraded.

Restrictions - None.

2.3.1.1.20 Disable Real/Image Confirm (R23)

Function - The Disable Real/Image Confirm Command

causes the system to disregard the Real/Image Confirm circuits. Signal frequency and location data is degraded.

Restrictions - None.

2.3.1.1.21 Disable Min. PW Confirm (R24)

Function - This command allows the system to process pulses of less than the minimum pulse width (0.4 usec). Data from these narrow pulses will be degraded.

Restrictions - None

2.3.1.1.22 Disable Frequency Confirm (R25)

Function - The Disable Frequency Confirm causes the system to disregard the Frequency Confirm criteria and allows processing of signals outside the 3 MHz confirm band. Data from these signals will be degraded.

Restrictions - None.

2.3.1.1.23 Reset Commands R18 through R25 (R26)

Function - This command resets commands R18 to R25.

Restrictions - R26 shall not be used to reset R18 (Disable Memories) if the system is in the Readin Mode.

2.3.1.1.24 Disable CW - SI Circuits (R27)

Function - This command causes the CW - SI Circuits to be disabled.

Restrictions - None.

2.3.1.1.25 Enable CW - SI Circuits (R28)

Function - This command enables the CW - SI circuits.

Restrictions - None.

2.3.1.1.26 Enable RF Calibrator (R31)

Function - This command causes internally generated RF signals to be inserted into the receiver on a periodic basis during EOB Readin operation for monitoring payload performance.

Restrictions - None.

2.3.1.1.27 Disable RF Calibrate Circuitry (R32)

Function - R32 disables the RF calibrate circuitry.

Restrictions - None.

2.3.1.1.28 Time Reset (R58)

Function - The time reset command resets the time counter.

Restrictions - None.

2.3.1.2 Operational Sequences

The following sequences describe the command sequences required for controlling the system in the EOB Readin modes. They do not include timing and commands for the CSU or DSU. All sequences are referred to an arbitrary time, "t." Refer to paragraph 2.3.2 for proper sequences with the recognizer enabled.

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2.3.1.2.1 Initial Sequence

The following commands should be programmed to precede the first Readin period to set the system for normal operation.

Payload Off (R12)

Recognizer Disable (R10)

Readin Off (R14)

Partial Scan A Off (R4)

Partial Scan B Off (R60)

Disable Recognizer/Partial Scan Input Mode (R50)

Disable Recognizer/Partial Scan Readout (R52)

Enable Upper & Lower Frequency Bands (R17)

Reset R18 through R25 (R26)

Enable CW - SI (R28)

Enable Recognizer Buffer (R30)

Enable RF Calibrator (R31)

2.3.1.2.2 Turn-On Sequence

t = 0 Payload On (R11)

t = 1.0 sec Mode Selection (to be issued as a function of operational requirements and payload performance):

Normal Commands

Increase/Decrease Dwell Time (R1/R2)

Threshold Control A or $\overline{A}$ (R5/R6)

Threshold Control B or $\overline{B}$ (R7/R8)

Partial Frequency Scan A On/Off (R3/R4)

Recognizer Disable (R10)

Alternate Disable/Enable Upper Freq. Band (R15/R17)

Disable/Enable Lower Freq. Band (R16/R17)

t = 1.1 sec Readin On (R13)

(System processes data until Readin Off issued)

2.3.1.2.3 Turn-Off Sequence

t = 0 sec Readin Off (R14)

t = 0.1 sec Partial Frequency Scan A Off (R14)

Partial Frequency Scan B Off (R60)

Recognizer Disable (R10)

t = 0.5 sec Payload Off (R12)

2.3.2 EOB/TI Readin

The EOB/TI Mode allows the system Recognizer to stop the LO scan and initiate predetection recording of incoming signals if a match of an incoming signal's parameters against a set of stored parameters is made. System operation in the EOB/TI mode is as described previously in paragraph 2.2 with the following commands used to control the Recognizer.

2.3.2.1 TI Command Functions and Restrictions

2.3.2.1.1 Recognizer Enable (R9)

Function - The Recognizer Enable allows the Recognizer to start comparison of incoming signals against stored sets of parameters. This signal actually supplies power to the Recognizer circuits. (Predetection circuit

power is supplied by R11.)

Restrictions - The Recognizer Enable Command shall be delayed from the Payload On Command (R11) by a minimum of 1 second and must precede Readin On (R13), Enable Recognizer/Partial Scan Readout Command (R51) and Enable Recognizer Input Mode Command (R49) by a minimum of 100 milliseconds.

2.3.2.1.2 Recognizer Disable (R10)

Function - The Recognizer Disable command disables the Recognizer by removing power from the Recognizer circuits.

Restrictions - Recognizer Disable (R10) shall be issued a minimum of 100 milliseconds before a Payload Off (R12). Also, in order to allow proper logic control of the memories it shall not be issued during any operate mode or for 100 milliseconds after the termination of an operate mode by Readin Off Command (R14), Disable Recognizer/Partial Scan Input Mode Command (R50), or Disable Recognizer/Partial Scan Readout (R52).

2.3.2.1.3 Disable Recognizer Buffer (R29)

Function - The Disable Recognizer Buffer (R29) blocks signal flow through the buffer ampli-

fiers between the Recognizer and the system Data Handler. This command is a failure mode command to be used in case of Recognizer failure to prevent degraded performance of the EOB circuits.

Restrictions - None.

2.3.2.1.4 Enable Recognizer Buffer (R30)

Function - R30 enables the Recognizer buffer amplifiers and allows normal Recognizer operation.

Restrictions - None.

2.3.2.1.5 Set Enables - Disables (R33 through R48)

Function - The eight sets, A through H, of the Recognizer are separately enabled and disabled through these commands. This allows individual sets to be enabled at specific times (location) during a flight.

Restrictions - No more than four (4) sets shall be enabled if the frequency limits stored in the sets match at any one frequency step. Otherwise, all sets can be enabled simultaneously.

2.3.2.1.6 Recognizer Threshold (R58, R59, R62, R63)

Function - The Recognizer minimum amplitude threshold level can be changed by these commands. These levels are relative to the EOB threshold. Table 2.3.2-1 specifies the minimum level described by the commands.

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TABLE 2.3.2-1 RECOGNIZER THRESHOLD

MINIMUM ACCEPTABLE LEVEL	COMMANDS*			
	$\overline{A}$ (R62)	B (R53)	E (R63)	B (R54)
Tmin	1	0	1	0
Tmin + 5 db	1	0	0	1
Tmin + 10 db	0	1	1	0
Tmin + 15 db	0	1	0	1

*All other command states are invalid.

2.3.2.2 Operational Sequences

To operate the system with the Recognizer enabled (EOB/TI Readin) the following sequences apply.

2.3.2.2.1 Turn-On Sequence

t = 0 Payload On (R11)

t = 1.0 Sec Mode Selection (To be issued as a function of operational requirements and system performance):

Recognizer Enable (R9)

Increase/Decrease Dwell Time (R1/R2)

Set EOB Threshold. Refer to paragraph 1.3.1.1.9. Partial Freq. Scan A On/Off (R3/R4)

Partial Freq. Scan B On/Off (R59/R60)

Set Recognizer Threshold. Refer to paragraph 2.3.2.1.6.

Disable/Enable Upper Freq. Band (R15/R17)

Disable/Enable Lower Freq. Band (R16/R17)

t = 1.1 Sec Readin On (R13)

(The system will process data in the EOB/TI Readin Mode until R15 is issued.

2.3.2.2.2 Turn-Off Sequence

t = 0 Readin Off (R14)

t = 0.1 Sec Recognizer Disable (R10)

Partial Freq. Scan A Off (R4)

Partial Freq. Scan B Off (R60)

t = 0.5 Sec Payload Off (R12)

2.3.3 Memory Load

The system has two memories that can be loaded with information from the vehicle Command Programmer Binary Digital Module. The following commands and command sequences apply.

2.3.3.1 Memory Load Commands

2.3.3.1.1 Enable Recognizer Input Mode (R49)

Function - This command sets the system to receive the data from the Binary Digital Module for loading the Recognizer memory.

Restrictions - The Recognizer shall be enabled (R9) at least 100 milliseconds before entering this

mode. This mode shall not occur simultaneously with any other operational mode. Command R49 shall be separated by a minimum time of 100 milliseconds from any other operational command.

2.3.3.1.2 Enable Partial Scan Input Mode (R61)

Function - This command sets the system to receive data from the Binary Digital Module for loading the Partial Scan Memory.

Restrictions - This mode shall not occur simultaneously with any other operate mode. Command R61 shall be separated by a minimum time of 100 milliseconds from any other operate mode command.

2.3.3.1.3 Disable Recognizer/Partial Scan Input Mode (R50)

Function - This command resets the Recognizer Input Mode (R49) and the Partial Scan Input Mode (R61).

Restrictions - This command shall occur a minimum of 100 milliseconds before any of the following commands: Recognizer Disable (R10), Read-in On (R13), Enable Recognizer/Partial Scan Readout (R51).

2.3.3.2 Operation Sequence for Memory Loads

2.3.3.2.1 Partial Scan Memory Load

t = 0 Payload On (R11)

t = 1 Sec Enable Partial Scan Input Mode (R61)

Load Memory with 36 bits. See paragraph 2.4.3 for word format.

t = x + 0 Sec Disable Recognizer/Partial Scan Input Mode (R350)

t = x + 0.1 Sec Execute commands to turn off or go to another operate mode.

2.3.3.2.2 Recognizer Memory Load

t = 0 Payload On (R11)

t = 1 Sec Recognizer Enable (R9)

t = 1.1 Sec Enable Recognizer Input Mode (R49)

Load Memory with 448 bits. See paragraph 2.4.3 for word format.

t = x + 0 Sec Disable Recognizer/Partial Scan Input Mode (R50)

t = x + 0.1 Sec Execute commands to turn off or to enable another operate mode.

2.3.4 Memory Readout

The Recognizer and Partial Scan memories are readout together using the following sequences.

2.3.4.1 Memory Readout Commands

2.3.4.1.1 Enable Recognizer/Partial Scan Readout (R51)

Function - This command enables the system to first readout the Recognizer and then the Partial Scan Memories when the proper word gate and clock signals are received from the

SGLS. The readout is nondestructive.

Restrictions - The Recognizer shall be enabled at least 100 ms before this command. A minimum of 100 ms time separation between R51 and any other operate mode is required.

2.3.4.1.2 Disable Recognizer/Partial Scan Readout

Function - This command disables the Recognizer/Partial Scan Readout Mode.

Restrictions - This command shall precede Recognizer Disable (R10) by a minimum of 100 milliseconds.

2.3.4.2 Operational Sequence

t = 0 Payload On (R11)*

t = 1.0 Sec Recognizer Enable (R9)

t = 1.1 Sec Enable Recognizer/Partial Scan Readout (R51)

(Readout Data to SGLS. Refer to paragraph 4.3 for word format)

t = x + 0 Sec Disable Recognizer/Partial Scan Readout (R52)

t = x + 0.1 Sec Recognizer Disable (R10)

t = x + 0.2 Sec Payload Off (R12)

*Ordinarily the Readout Mode would follow a Readin Mode and power would still be on and the Recognizer enabled. Then R51 would be programmed a minimum of 100 milliseconds after R50 (Disable Recognizer/Partial Scan Input Mode).

2.4 Digital Data Word Formats

The digital data output from the system consists of 182-bit words (192-bits from the CSU). A 48-bit digital marker word is sent to the DSU. The Recognizer readin word is a 448-bit digital word. The partial scan readin word is a 36-bit digital word. The Recognizer/Partial Scan readout word is a 484-bit word which has the codes inverted from those which were read in (i.e. A "0" input = A "1" output).

2.4.1 EOB Digital Data

The encoded parameters within the 182-bit words are arranged according to the two basic structures shown in Tables 2.4-1 and 2.4-2. The start, stop, and time-attitude words (SSTA) make up the status type words. The intercept data words make up the other type of 182-bit words. Unless otherwise noted, the least significant digit of each code is on the right when the bits of the code are numbered from left to right. Details of the digital codes used in each type of word are contained in The Ground Data Handling Requirement Report for the Reaper Payload, LTVE Document No. 4124-11184.

2.4.1.1 Start, Stop and Time-Attitude (SSTA) Words

SSTA words contain status information about the system and vehicle. A Start word is generated when R13 (Readin On) is issued and a Stop word is generated when R14 (Readin Off)

TABLE 2.4-1. INTERCEPT WORD FORMAT

1 Word	(MSB)	49	(MSB)
2 ID		50 Amp. #1	
3	(LSB)	51	
4	(LSB)	52	(LSB)
5		53	
6		54 δ RC	
7		55	
8		56	
9		57 δ AR	
10 Time		58	D/F #1
11		59	(3 LSB)
12		60 δ RD	
13		61	
14		62	
15		63 δ BR	
16		64	
17		65 Parity	
18		66	(MSB)
19		67	
20	(MSB)	68	
21 CW-SI Operation		69	
22		70	
23 δ RC		71	
24		72 PRI 1-2	
25 δ AR	D/F #1	73	
26		74	
27 δ RD	(2 MSB)	75	
28		76	
29 δ BR		77	
30 High-Low Band		78	(LSB)
31	(MSB)	79 Real/Image #2	
32		80 IF Freq. #2	
33		81	
34		82	(MSB)
35 LO Frequency		83	
36		84 PW #2	
37		85	
38		86	
39	(LSB)	87	(LSB)
40 Real/Image #1		88	(MSB)
41 IF Freq. #1		89 AMP. #2	
42		90	
43	(MSB)	91	(LSB)
44		92	
45		93 δ RC	
46 PW #1		94	
47		95	
48	(LSB)	96 δ AR	
		97	D/F #2
		98	(3 LSB)
		99 δ RD	
		100	
		101	
		102 δ BR	
		103	
		104 Parity	
		105	(MSB)
		106	
		107	
		108	
		109	
		110	
		111 PRI 2-3	
		112	
		113	
		114	
		115	
		116	
		117	(LSB)
		118 Real/Image #3	
		119 IF Freq. #3	
		120	
		121	(MSB)
		122	
		123 PW #3	
		124	
		125	
		126	(LSB)
		127	(MSB)
		128	
		129 AMP. #3	
		130	(LSB)
		131	
		132 δ RC	
		133	
		134	
		135 δ AR	D/F #3
		136	
		137	(3 LSB)
		138 δ RD	
		139	
		140	
		141 δ BR	
		142	
		143 Parity	
		144	(MSB)
		145	
		146	
		147	
		148	
		149	
		150 PRI 3-4	
		151	
		152	
		153	
		154	
		155	
		156	(LSB)
		157 Real/Image #4	
		158 IF Freq. #4	
		159	
		160	(MSB)
		161	
		162	
		163 PW #4	
		164	
		165	(LSB)
		166	(MSB)
		167 AMP. #4	
		168	
		169	(LSB)
		170	
		171 δ RC	
		172	
		173	
		174 δ AR	
		175	D/F #4
		176	(3 LSB)
		177 δ RD	
		178	
		179	
		180 δ BR	
		181	
		182 Parity	

TABLE 2.4-2. STATUS WORD FORMAT

1	Word (MSB)	47	Roll	93	Pitch	139	Zero
2	ID	48	↓	94	↓	140	↓
3	(LSB)	49	↓	95	Pitch (LSB)	141	↓
4	Time (LSB)	50	Roll (LSB)	96	Roll (MSB)	142	Zero
5	↑	51	Sun Bit	97	↑	143	Parity
6	↑	52	Zero	98	↑	144	Partial Scan "A" On
7	↑	53	↑	99	↑	145	Threshold Control #1
8	↑	54	↑	100	↑	146	Threshold Control #2
9	↑	55	↑	101	↑	147	Recognizer Enabled
10	↑	56	↑	102	Roll (LSB)	148	Upper Freq. Band Enabled
11	↑	57	↑	103	Sun Bit	149	Lower Freq. Band Enabled
12	↑	58	↑	104	Parity	150	RF Cal. Enabled
13	↑	59	↑	105	Word (MSB)	151	Tmin. Confirm Enabled
14	↑	60	↑	106	ID	152	Tmax. Inhibit Enabled
15	↑	61	↑	107	(LSB)	153	A/R Inhibit Enabled
16	↑	62	↑	108	Time (LSB)	154	R/I Confirm Enabled
17	↑	63	↑	109	↑	155	PW Confirm Enabled
18	↑	64	Zero	110	↑	156	Freq. Confirm Enabled
19	↑	65	Parity	111	↑	157	Spare T/M
20	↑	66	Zero	112	↑	158	Recog. Buffer Disabled
21	↑	67	↑	113	↑	159	Set "A" Disabled
22	↑	68	↑	114	↑	160	Set "B" Disabled
23	↑	69	↑	115	↑	161	Set "C" Disabled
24	↑	70	↑	116	↑	162	Set "D" Disabled
25	↑	71	↑	117	↑	163	Set "E" Disabled
26	Time (MSB)	72	↑	118	↑	164	Set "F" Disabled
27	CW-SI Cmd. Enable	73	↑	119	↑	165	Set "G" Disabled
28	Recog. Bit	74	↑	120	↑	166	Set "H" Disabled
29	Memories Disabled	75	↑	121	↑	167	Recog. Input Mode Enabled
30	FOV Inhibit Enabled	76	↑	122	↑	168	Recog./P.S. Readout Enabled
31	Zero	77	↑	123	↑	169	Recog. Threshold Bit A
32	↑	78	Zero	124	↑	170	Recog. Threshold Bit B
33	↑	79	CW-SI Cmd. Enable	125	↑	171	Partial Scan Readin Disabled
34	Zero	80	Recog. Bit	126	↑	172	Spare T/M
35	Readin On	81	Memories Disabled	127	↑	173	Time Reset Enabled
36	Dwell Time Min.	82	FOV Inhibit Enabled	128	↑	174	Partial Scan B On
37	Pitch (MSB)	83	Zero	129	↑	175	Spare T/M
38	↑	84	↑	130	Time (MSB)	176	↑
39	↑	85	↑	131	Zero	177	↑
40	↑	86	Zero	132	↑	178	↑
41	↑	87	Readin On	133	↑	179	↑
42	↑	88	Dwell Time Min.	134	↑	180	↑
43	Pitch (LSB)	89	Pitch (MSB)	135	↑	181	Spare T/M
44	Roll (MSB)	90	↑	136	↑	182	Parity
45	↑	91	↑	137	↑		
46	Roll	92	Pitch	138	Zero		

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is issued. Time-attitude words are automatically generated at 16-second intervals while the system is in the EOB Readin Mode. Each of these words contain time, vehicle pitch and roll data, and payload command status information.

2.4.1.2 Intercept Data Words

One intercept data word is generated for each signal processed by the system. Each intercept data word contains the set of measurements from 2, 3, or 4 pulses from the signal.

2.4.2 TI Marker Words

Marker words will be recorded on the digital track of the DSU if the recorder is actuated. The words will be recorded at a rate of eight per second. The marker word will contain information on DSU status, amplitude threshold, frequency, set ID, and time. The encoded parameters within the marker word are arranged as shown in Table 2.4-3.

2.4.3 Memory Load and Readout Formats

The following word formats have been established for the data to be read into and out of the recognizer and partial scan memories. In all cases the MSB of each parameter corresponds to the lowest numbered bit. The words are to be read in or read out with bit number one first. Detail code information is contained in the Ground Data Handling Requirements Report for the Reaper Payload, LTVE Document No, 4124-11184. Word format is summarized in Table 2.4-4.

TABLE 2.4-3 MARKER WORD FORMAT

BIT NO.	CONTENTS	BIT NO.	CONTENTS
1	Spare	24	(LSB)
2	DSU	25	
3	Status	26	
4		27	
5		28	
6	Amplitude	29	
7	Threshold	30	
8	DSU	31	
9	Status	32	
10	Stop Scan	33	Time
11	(LSB)	34	
12	Set ID	35	
13	(MSB)	36	
14		37	
15		38	
16		39	
17		40	
18	Frequency	41	
19		42	
20		43	
21		44	
22		45	
23		46	(MSB)
		47	Parity
		48	Reaper "0"

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TABLE 2.4-4. RECOGNIZER WORD FORMAT

BIT NUMBER(S)								Sub-Word Content
Set A	Set B	Set C	Set D	Set E	Set F	Set G	Set H	
1-9	57-65	113-121	169-177	225-233	281-289	337-345	393-401	Frequency - Lower Limit
10-14	66-70	122-126	178-182	234-238	290-294	346-350	402-406	Logical Zeros
15-23	71-79	127-135	183-191	239-247	295-303	351-359	407-415	Frequency - Upper Limit
24-25	80-81	136-137	192-193	248-249	304-305	360-361	416-417	Logical Zeros
26-28	82-84	138-140	194-196	250-252	306-308	362-364	418-420	Set Identification
29-32	85-88	141-142	197-198	253-254	309-310	365-366	421-422	PW - Lower Limit
33-36	89-92	143-148	199-204	255-260	311-316	367-372	423-428	PW - Upper Limit
37	93	149	205	261	317	373	429	Recognizer Input Mode
38-40	94-96	150-152	206-208	262-264	318-320	374-376	430-432	Recognizer Output Mode
41-42	97-98	153-154	209-210	265-266	321-322	377-378	433-434	Logical Zeros
43-49	99-105	155-161	211-217	267-273	323-329	379-385	435-441	PRI - Lower Limit
50-56	106-112	162-168	218-224	274-280	330-336	386-392	442-448	PRI - Upper Limit

2.5. Performance Specifications Summary

This section presents a summary of the EOB/TI performance specification of the Reaper system. Nominal flight conditions are an altitude of 268 nm, an orbit inclination of 75°, and an orientation such that the payload field-of-view y-axis points in the direction of flight. No part of the vehicle nor its payloads shall extend beyond the plane of the Reaper antennas' radiating apertures.

2.5.1 Frqequency Coverage

The Reaper system provides:

(a) A frequency range (RF range) from 1800 MHz to 3300 MHz.

(b) A confirm band (IF range processed or confirmed at any frequency step) of a nominal 3 MHz.

(c) A frequency step (basic scan increment) of 2.5 ± 0.5 MHz.

(d) Two partial frequency band scans over any non-overlapping segments (5 Mc resolution) of the RF range.

2.5.2 Field-of-View

Under the nominal flight conditions, the minimum cross-track field-of-view (FOV) is 160 nm and the in-track FOV is such as to provide a minimum of two looks at each target with a normal dwell time.

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2.5.3 D/F Accuracy

The system is capable of locating an emitter within a circle of 7.5 n.mi. radius with 95% confidence. This accuracy is specified for data taken uniformly over the frequency band and the field-of-view. The accuracy specification allows optimizing the combination of coarse and fine phase readings and averaging the phase information from at least eight pulses during the ground data processing. The above accuracy is for the Reaper system only and does not allow for vehicle errors such as pitch, roll, yaw, and time from the vehicle clock.

2.5.4 Scan Parameters

Two dwell modes are provided. Dwell time is defined as the time that the system searches at each frequency step.

2.5.4.1 Normal Dwell Mode

The normal dwell mode provides a dwell time such that four successive pulses with a PRI of 5.28 milliseconds or less can be processed in a single dwell. The dwell time is adaptive. If no signals are found on a particular local oscillator stop, the dwell lasts for only 6.14 milliseconds. If one or more intercepts are confirmed, the dwell time is extended to 22.5 milliseconds.

2.5.4.2 Alternate Dwell Mode

An alternate dwell mode enabled by command provides a dwell time twice that of the normal mode with one or more confirmed intercepts.

2.5.5 Sensitivity

The maximum sensitivity (minimum threshold) is -93 dbm at angles to the cross-track edge of the FOV or 23°, whichever is less. Threshold is defined as the pulse amplitude below which a logic decision is made to inhibit the pulse and is referred to the input to the system antennas. The threshold is variable upward in two 5 db ± 1 db steps by vehicle command.

2.5.6 Dynamic Range

The system accepts and processes signals over a 40 db minimum range upward from minimum threshold (-93 dbm).

2.5.7 Recognizer

The system is capable of accepting and storing digital listings of parameters for matching with the parameters of incoming signals. The stored parameter listings may be reprogrammed with new values on orbit. The parameter listings are compared to incoming signal parameters when the payload recognizer is enabled. Each listing may be programmed to examine signals arriving from any direction or to examine only those signals which appear within the field-of-view. The coverage is controlled by a preprogrammed bit in the parameter set.

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2.5.7.1 Recognizer Set Inputs

The eight recognition sets are loaded by a single serial bit stream (1000 bps) from the binary digital module of the vehicle programmer. The range and bit format of the sotred parameters must correspond to those of the system.

Each of the eight sets are enabled and disabled separately by command from the vehicle programmer. No more than four sets with overlapping frequency limits may be enabled at the same time.

2.5.7.2 Output Modes

The output mode code specified with each recognition set initiates the appropriate action to alter the mode of operation when a match is achieved with that set. Output modes are given in Table 2.5-1. Protective techniques are employed to prevent a recognizer failure from affecting the EOB mode operation.

2.5.7.3 Digital Data to DSU

Digital time and frequency words are supplied to the digital track of the DSU whenever analog data is being recorded. Time frequency words are supplied at approximately 1/8-second intervals.

2.5.7.4 T/M Output

The recognizer is capable of reading out the recognizer memory to the telemetry system on command.

TABLE 2.5-1 RECOGNIZER OUTPUT MODES

MODE NO.	EXECUTION
1	Send "Begin Record" pulse to DSU. If a "DSU Available" input signal is present, the system will stop frequency scan before stepping frequency and initiate predetection recording. After recording two seconds, send "End Record" pulse to DSU and resume scan. If "DSU Not Available" signal is present, continue scan.
2	Same as 1, except 4 seconds recording time.
3	Same as 1, except 8 seconds recording time.
4	Send "Begin Record" pulse to DSU. Stop frequency scan before stepping frequency. If a "DSU Available" signal is present, initiate predetection recording. After 4 seconds, send "End Record" pulse to DSU and resume scan. If "DSU Not Available" signal is present, remain locked on frequency until "DSU Available" signal is received or until the frequency scan has been stopped for a total of 60 seconds.
5	Same as 4, except 8 seconds recording time in place of four seconds.
6	Same as 4, except 300 seconds recording time in place of four seconds.

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2.5.8 Pre-Detected Signal Output

The signal delivered to the DSU for recording contains a predetected video signal, two reference tones and a tag pulse. The tag pulse is present when the received signal is within the amplitude ratio inhibit circle.

The predetected 3-db passband output is from 0.5 to 5.5 MHz. The predetected output center frequency of 3 MHz corresponds to the system IF center frequency. The output is a sinusoidal waveform which preserves any intrapulse modulation appearing on the input signal within the bandwidth and local oscillator limitations of the system. Signals appearing in the system's IF which are more than 2.75 MHz from the IF center frequency are attenuated by at least eight db before being sent to the DSU. The predetected signal is hard limited at 0.7 volt p-p. The gain of the predetection circuits is adjusted as a function of the input power.

The gain adjustment provides for selecting one of four amplitude response curves (Predetected output amplitude vs. signal power input). This insures that the output level of any signal which is within the receiver's dynamic range and is matched to a recognizer set, will fall within the range of 0.19 volt p-p to 0.6 volt p-p. The adjustment is made once at the beginning of each record period following a recognized signal. The response curves are nominally linear up to the output level of 0.6 volt p-p.

The tag pulse is a 250 kHz sinusoid whose envelope is a cosine squared pulse with a spectrum centered at 250 kHz. Peak amplitude is 0.28, + .02, - .05 volt in amplitude. Envelope width is 5.0 ± 1 microsecond at the 50% point.

The reference tones are 6 MHz ± 5 kHz and 46.875 kHz ± 100 Hz with an adjustable amplitude and are added to the predetected video to aid in ground processing. Tone amplitude can be set during initial payload alignment to any value between 2.5 millivolts and 50 millivolts rms.

2.5.9 CW Operation

The system processes CW signals by recognizing that the signal pulse width is greater than 24 usec. An intercept word is generated with a maximum PW and a minimum PRI indication for four readings. This situation also causes the CW signal indicate circuit to be energized and the CW bit to be inserted in the subsequent data words of that dwell period. This intercept word provides four D/F phase readings and a unique data format for identification of CW signals. The CW signal indicate circuit provides the ability to compare pulse signals against the CW background and allows processing of the pulsed signal if a difference of at least 15 db is present.

2.5.10 Buffer Storage

The buffer storage provides a temporary storage to allow parallel processing of emitter signals and allows synchronization to the vehicle memory. The buffer storage is

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erased upon receipt of a payload "On" command. Individual words within the storage are erased as they are read out to vehicle memory.

2.5.11 Measurement Capabilities

2.5.11.1 Frequency Measurement

The system provides a frequency measurement resolution (encoder step) of 1 MHz and an absolute frequency accuracy (rms offset between actual and encoded frequency values) of ± 0.3%.

2.5.11.2 Frequency Repeatability

The system provides a frequency measurement repeatability of ±1 MHz for ten minutes.

2.5.11.3 Pulse Width Measurements

Signal pulse widths from 0.4 usec to 4.0 usec are measured at system threshold to an accuracy of ± 0.25 usec and to a resolution of 125 nanoseconds.

2.5.11.4 Pulse Repetition Interval Measurements

The PRI of a signal is measured over the range of 100 usec to 8000 usec with 1 usec resolution and a maximum error of ± .1% or ± 1 usec, whichever is greater.

2.5.11.5 Pulse Amplitude Measurement

Signal pulse amplitude is measured to an accuracy of ± 5.0 db with a 2.5 db resolution.

2.5.11.6 Attitude Measurement

Pitch and roll are encoded by the system from two analog voltage signals supplied by the vehicle. Voltages from -11 to -10 volts and +10 to +11 volts are encoded to an all zero code. A 7-bit code is provided and the remaining 127 codes provide 0.15748 volt increments. A relay closure or a signal similar to the signals of the command programmer is provided by the vehicle to indicate abnormal vehicle attitude which causes a "one" to be inserted in the "sun bit" position of the status words.

2.5.11.7 Time Measurement

The payload is able to accept and count 5,529,000 1/8-second timing pulses continuously before being reset. The count can be reset to zero at any time by means of command. The format and method of counting are as shown below.

No. of Bits	Timing Pulse Rate	Recycle Time
20 binary bits	8 pulses/sec	24 hours
3 binary bits	1 pulse/day	8 days

The time counter is capable of continuous operation with the payload off, providing that the timing pulse line and the 28-volt unregulated line to the payload are energized. The timing information is included in the time-frequency, intercept, and status words.

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2.5.12 Digital Word Formats

The word formats and code definitions are described in detail in The Ground Data Handling Requirements Report for the Reaper Payload, LTVE Document No. 4124-11184. The types of words provided are time-frequency words, intercept words and status words.

2.5.12.1 Time Frequency (Marker) Word

A time-frequency (marker) word is written on the digital data track of the DSU at a 10 Kc clock rate.

2.5.12.2 Intercept Word

An intercept word is generated for two to four confirmed pulses. An intercept word contains time, frequency, angle of arrival, pulse width, PRI and amplitude information. This word is 182 bits in length.

2.5.12.3 Status Word

Start words, stop words and time attitude words are status words. Time, attitude and other status information are contained in status words. This word is also 182 bits in length.

2.5.13 False Data

2.5.13.1 Spurious Rejection

The system provides 55 db rejection for spurious signals. In-band spurious signals are also rejected by phase and amplitude criteria.

2.5.13.2 Ambiguity Resolution

No more than 5% of the pulses obtained at the lowest pulse amplitude reading can be in error due to incorrect ambiguity resolution. Potentially ambiguous data is flagged for solution during ground processing. No more than 25% of the pulses obtained at the lowest pulse amplitude reading may be flagged. No data may be discarded or inhibited on the ground in order to reduce the percentage of erroneous data words due to incorrect ambiguity resolution.

2.5.13.3 Amplitude Poke-Through

No false data is obtained due to amplitude poke-through in the amplitude ratio inhibit circuitry, independent of the phase field-of-view inhibit. Demonstration of this requirement is based upon the antenna range data under conditions of high signal-to-noise ratio.

2.5.14 Orbital Lifetime

The Reaper Payload orbital lifetime will be six months under nominal programming. Nominal programming is considered to be a maximum of 90 hours intermittent operation per month with a 30-minute maximum operating period per orbit.

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3.0 SYSTEM ANALYSIS

3.1 Introduction

In this section, the fundamental characteristics of the Reaper system are discussed and analyzed. The error budget associated with each of the measurement accuracy specifications is presented and analyzed to show how the system meets each of the accuracy specifications.

3.2 Coordinate Geometry

3.2.1 Emitter Location Coordinate System

The basic coordinate system for specifying D/F information is illustrated in Figure 3.2-1. The x, y, z set of axes is a left-handed system with +z axis along the antenna array boresight axis with the x-y axes in the plane of the antenna phase centers. A sphere of unit radius is centered about the origin. The direction to an emitter on the earth is expressed as the point of intersection of the line of sight with the unit sphere. The intersection point is

$$x = \sin\theta \sin\xi \qquad (3.2\text{-}1)$$

$$y = \sin\theta \cos\xi \qquad (3.2\text{-}2)$$

$$z = \cos\theta \qquad (3.2\text{-}3)$$

where θ is the elevation angle measured from the +z axis to the line of sight, and ξ is the azimuth-angle measured from the +y axis to the projection of the line of sight into the x-y plane as viewed from above. Since there are only two independent parameters in Equations 3.2-1, 3.2-2, and 3.2-3,

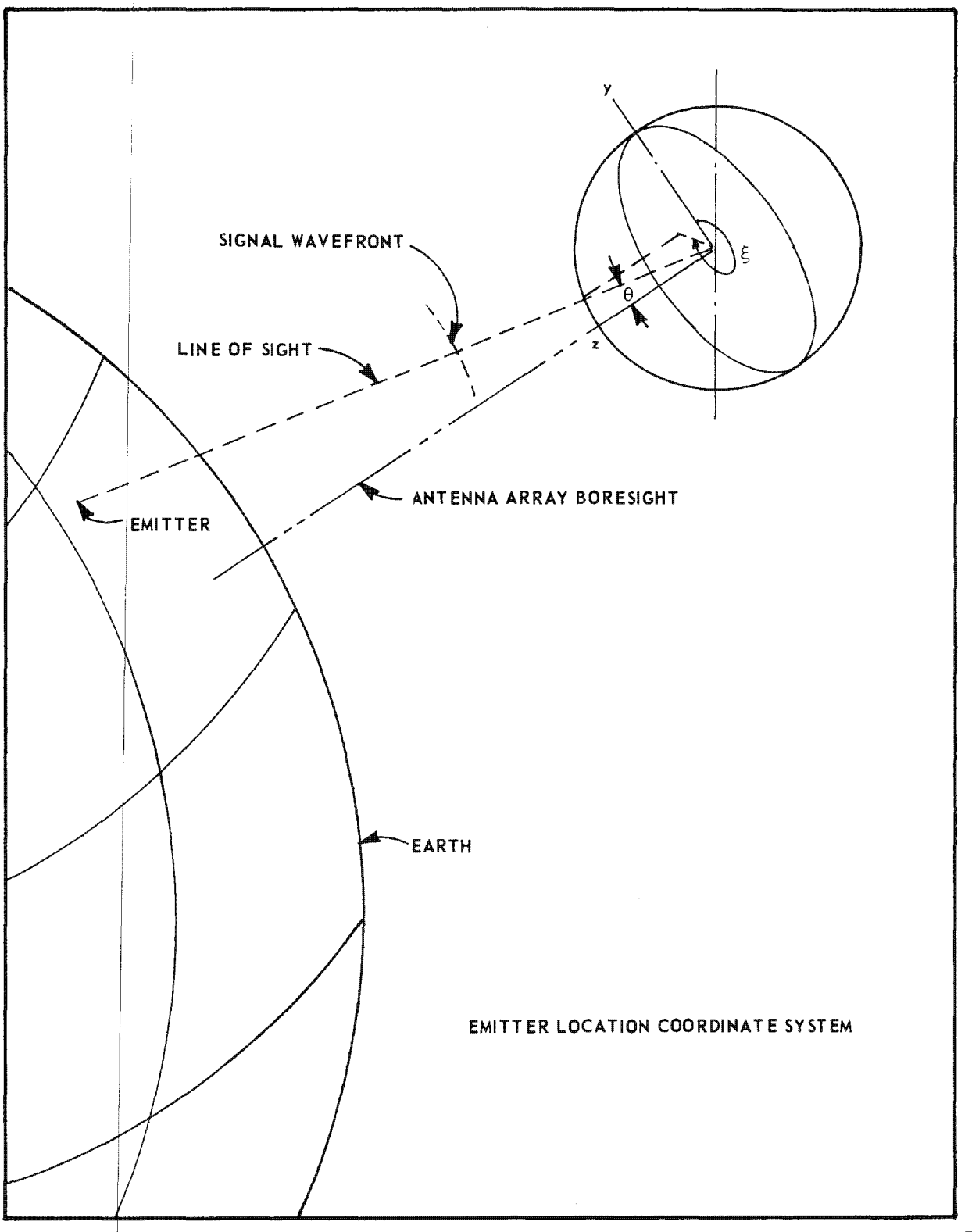

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Figure 3.2-1. Emitter Location Coordinate System

viz., θ and ξ, direction to the emitter can be represented uniquely by the quantities x and y alone. These represent the projection of the point of intersection of the unit sphere and the line of sight into the x-y plane. All possible lines of sight to emitters within $0° \leq \theta \leq 90°$ and $0° \leq \xi \leq 360°$ are represented as points in the x-y plane within a circle of unit radius. The direction of an emitter from the payload is measured by computing $\sin\theta \cos\xi$ and $\sin\theta \sin\xi$ from electrical phase information as described in paragraph 3.3.

3.2.2 Restricted Field of View

A phase field-of-view is defined in Figure 3.2-2 to limit the area of coverage. Only those lines of sight that fall within the field of view are accepted by the system. The limited coverage is established to eliminate intercepts from targets at large elevation angles where location information would be comparatively poor. Signals from outside the field of view are rejected on the basis of phase information and signal amplitude ratio data as described in paragraphs 3.3.2 and 3.4.1; those within the field of view are accepted and processed. The limits of the field of view are defined in terms of $\sin\theta \sin\xi$ and $\sin\theta \cos\xi$, the fundamental coordinates. Paragraph 3.3 discusses the relation between these coordinates and the phase quantities actually measured in the system. The field of view shown in Figure 3.2-2 represents about one percent of the total ground area in view of the

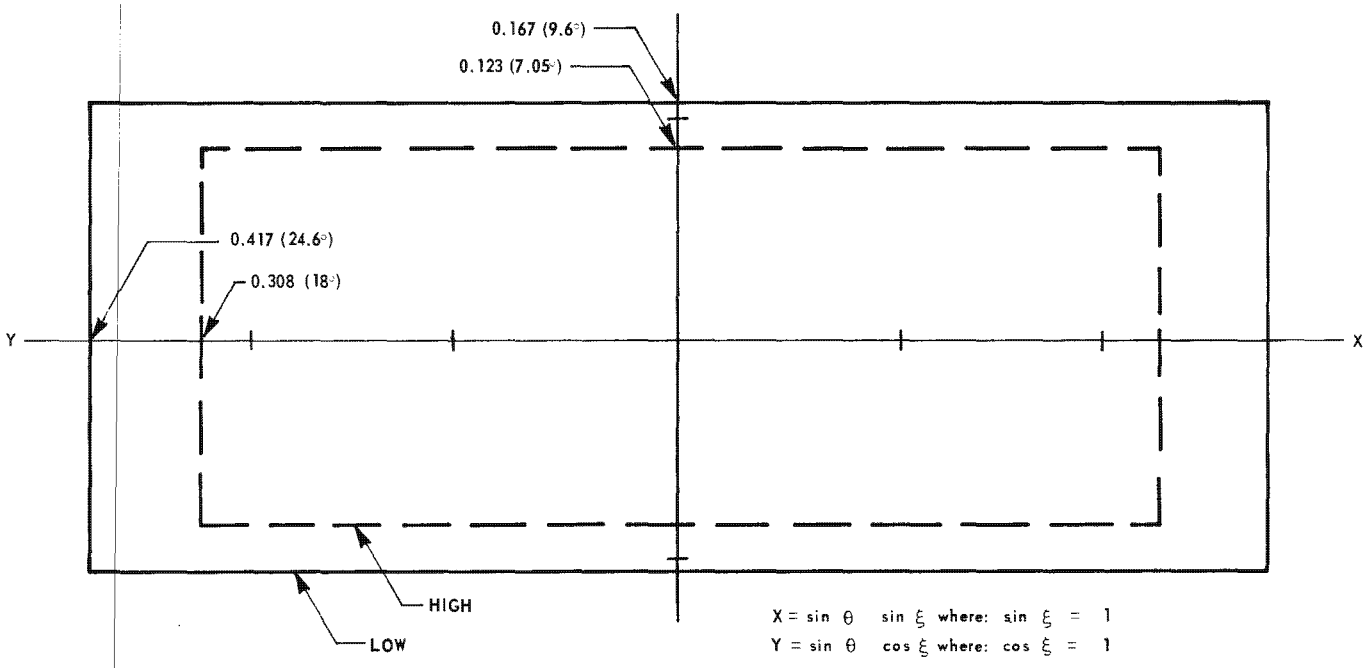

FIGURE 3.2-2 SYSTEM FIELD-OF-VIEW

vehicle at an altitude of 268 nautical miles.

3.2.3 Field-of-View Earth Coverage

On the earth's surface, the field of view has a shape determined by the curvature of the earth and the orientation of the antenna platform with respect to the earth. The payload antenna array boresight axis is a line through the nadir. For this attitude, the earth coverage pattern for a spherical earth is as shown in Figure 3.2-3 for a vehicle height of 268 nautical miles. The shape of this pattern will change considerably with vehicle height. As height is increased, the overall dimensions are increased and the corners

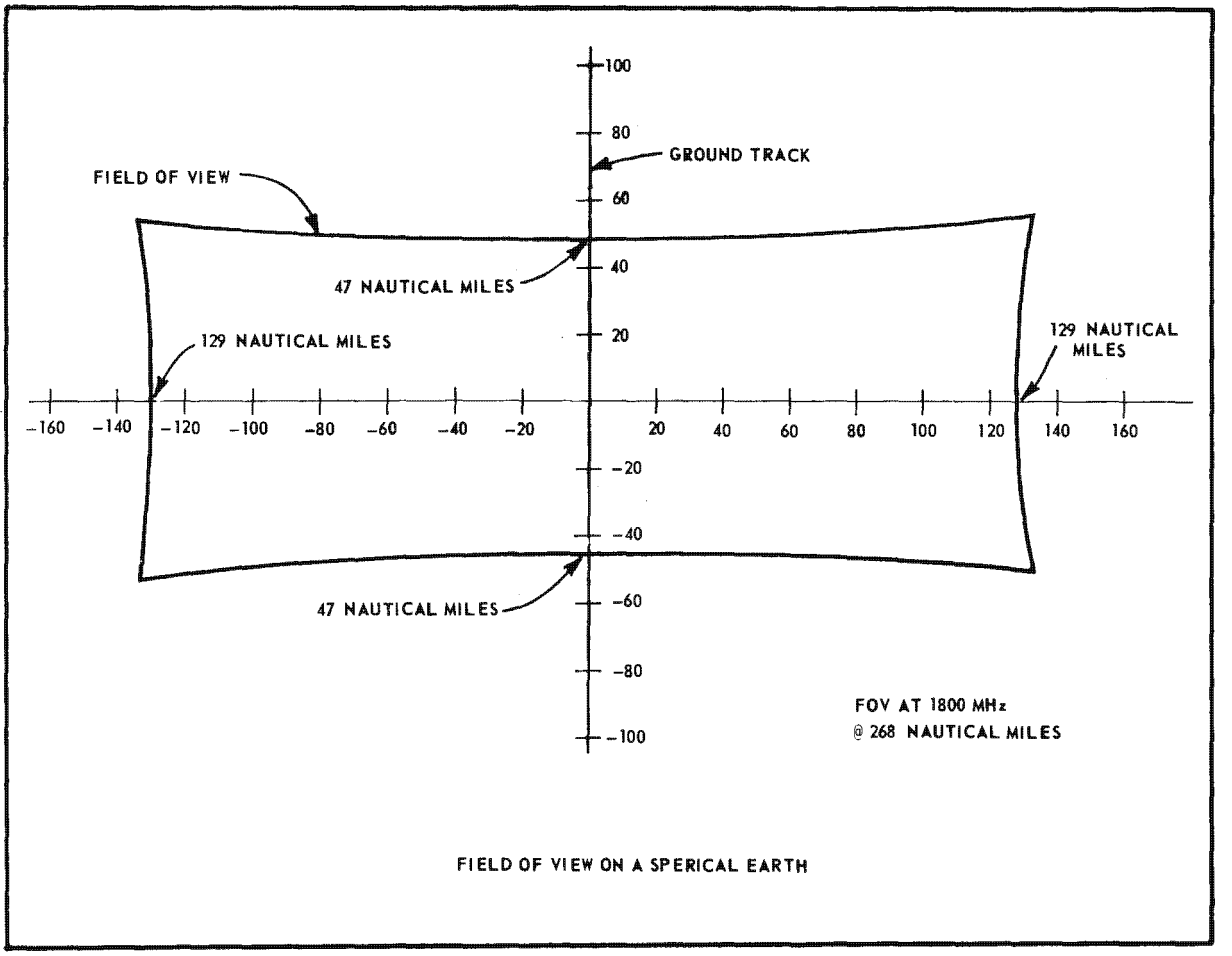

FIGURE 3.2-3 FIELD-OF-VIEW ON A SPHERICAL EARTH

become more elongated on a spherical earth.

The minimum in-track dimension of the Reaper space window was shown earlier to be 66.4 nautical miles. At an orbital altitude of 268 nautical miles the period of an earth satellite is 5663.88 mean solar seconds. Assuming one earth radius equal to 3440 nautical miles gives a satellite ground speed of 3.816 nautical miles/second. At this speed, a time span of 17.4 seconds is required for a target to pass

completely through the Reaper phase field-of-view. To satisfy the two looks per target criterion of sections 2.5.2, each scan must require no more than 8.7 seconds. Figure 3.1-2 shows that an increment activity of 33% results in an 8.7-second scan time. This means that when operating in the normal dwell mode, if 33% or less of the local oscillator steps contain targets which meet all system confirm criteria, the local oscillators will have time to scan completely through the operating range twice in the time required for a target to move completely through the in-track field-of-view.

3.3 Antenna Phase Response

3.3.1 Antenna Array Phase Relations

The antenna array from which electrical phase information is obtained consists of two sets of circularly polarized horns for each operating band as shown in Figure 3.3-1. In this illustration, the array is shown in the antenna phase-center plane (viewed from behind) which is also the x-y plane defined in paragraph 3.2.1 with the y axis in the direction of the azimuth reference line and the x axis parallel to the A-R and A'-R' antenna pair axis. Since the wave will arrive at each antenna at different times, a phase difference exists that is determined by the difference in distances that the wave must travel to reach each antenna. The differences in distance for the phase information channels are given by $d_{AR} \sin \theta \cos \xi$ for antenna pair A-R, $d_{RC} \sin \theta \sin \xi$ for

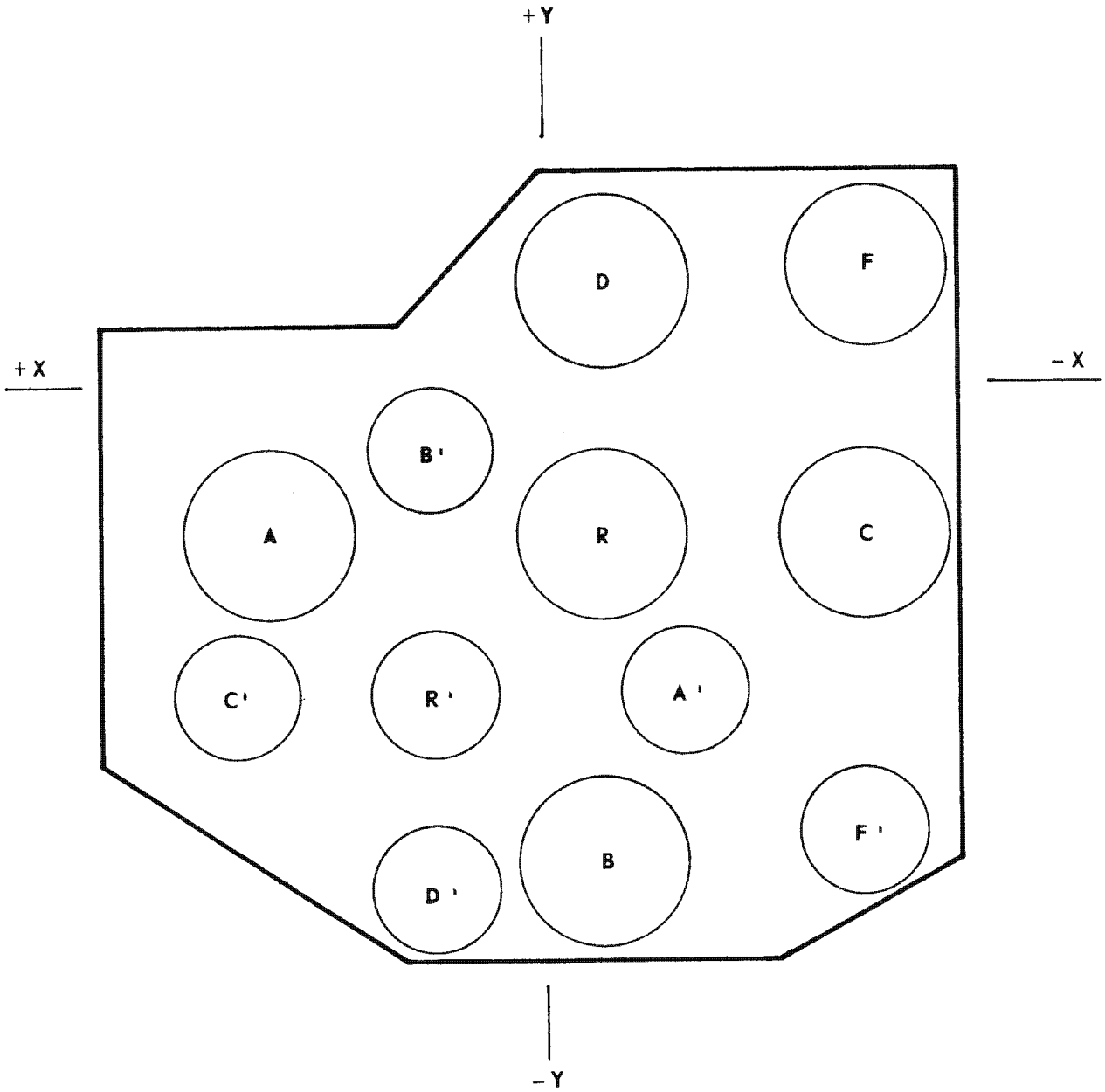

FIGURE 3.3-1 ANTENNA ARRAY

antenna pair R-C, $d_{BR} \sin\theta \cos\xi$ for antenna pair B-R, and $d_{RD} \sin\theta \sin\xi$ for antenna pair R-D. The actual electrical phase differences are then:

$$\delta AR = \frac{2\pi}{\lambda} d_{AR} \sin\theta \cos\xi \text{ radians} \qquad (3.3\text{-}1)$$

$$\delta RC = \frac{2\pi}{\lambda} d_{RC} \sin\theta \sin\xi \text{ radians} \qquad (3.3\text{-}2)$$

$$\delta BR = \frac{2\pi}{\lambda} d_{BR} \sin\theta \cos\xi \text{ radians} \qquad (3.3\text{-}3)$$

$$\delta RD = \frac{2\pi}{\lambda} d_{RD} \sin\theta \sin\xi \text{ radians} \qquad (3.3\text{-}4)$$

where $\frac{2\pi}{\lambda}$ = phase constant in radians/inch

λ = signal wavelength in inches

$d_{AR} = d_{BR}$ = antenna spacings in inches

$d_{RC} = d_{RD}$ = antenna spacing in inches

θ and ξ are the elevation and azimuth angles respectively as defined in paragraph 3.2.1.

In equations 3.3-1 through 3.3-4, $\sin\theta \cos\xi$ and $\sin\theta \sin\xi$ are the y and x coordinates, respectively, of the intersection of the line of sight with the unit sphere in the emitter location coordinate system. The emitter direction is given by the following.

$$\sin\theta \sin\xi = \frac{\lambda}{2\pi} \frac{\delta_{RC}}{d_{RC}} = \frac{\lambda}{2\pi} \frac{\delta_{RD}}{d_{RD}} \qquad (3.3\text{-}5)$$

$$\sin\theta \cos\xi = \frac{\lambda}{2\pi} \frac{\delta_{AR}}{d_{AR}} = \frac{\lambda}{2\pi} \frac{\delta_{BR}}{d_{BR}} \qquad (3.3\text{-}6)$$

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Thus, the emitter direction may be obtained from the electrical phase measurements.

For a given signal all quantities in equations 3.3-5 and 3.3-6 are constant except phase, so lines of constant phase are straight and of constant gradient within the unit circle of the x-y plane.

3.3.2 Phase Patterns in the Field-of-View

The field of view phase pattern in the x-y plane is shown in Figure 3.3-2. This phase pattern was developed from equations 3.3-5 and 3.3-6 for both coarse and fine phase, using the antenna spacings of 3.0λ for fine phase associated

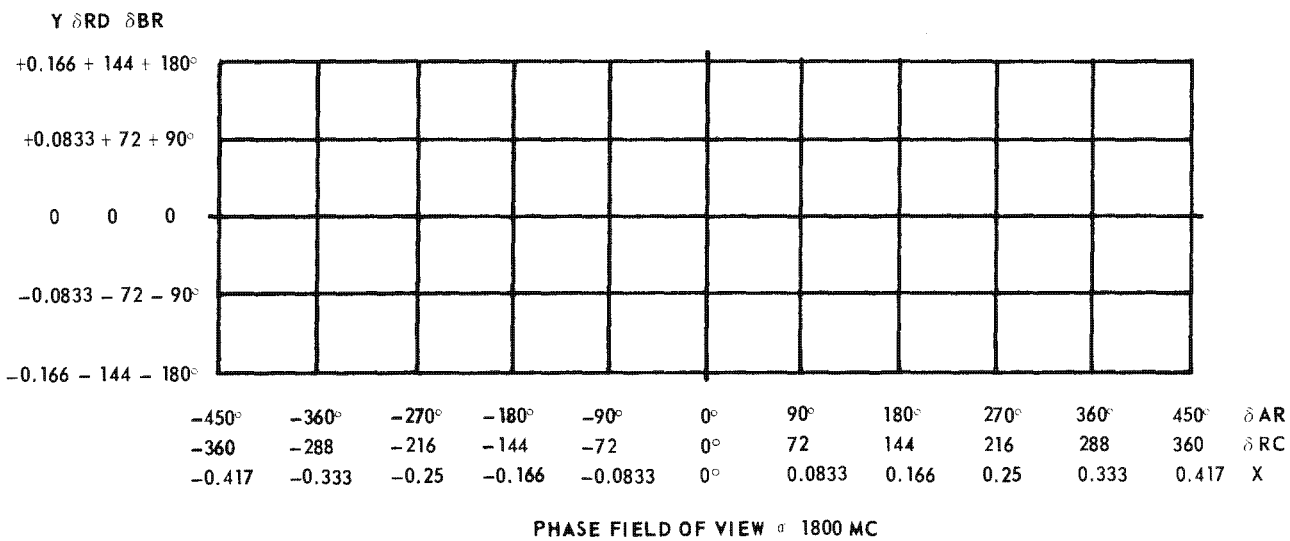

FIGURE 3.3-2 PHASE FIELD-OF-VIEW

with AR and BR, and 2.4λ for coarse phase associated with RC and RD. The constant electrical phase lines are shown with corresponding x-y coordinate values.

Ambiguities in the detected fine or coarse phase occur at intervals of 360°, due to the periodicity of the received signal. For example, the phase lines at -270°, +90°, +450° are ambiguous. These ambiguities must be removed before unambiguous emitter location can be established. The method of ambiguity removal is discussed in paragraph 3.3.3.

3.3.3 Ambiguity Removal Technique

The system resolves ambiguous target locations by utilizing both coarse and fine phase information from different antenna pairs. The fine phase readings are quantized into increments of 11.25 electrical degrees. The coarse phase readings are quantized into increments of 18 electrical degrees. Each fine phase interval is associated with a particular unambiguous group of four coarse phase intervals. In addition to normal or "undelayed" phase, the System utilizes 90° "delayed" phase which allows the phase codes to be uniquely assigned over 360° intervals. The horizon-to-horizon relationship between fine and coarse phase is shown in Figure 3.3-3.

As seen in Figure 3.3-3, there are two 360° ambiguous fine phase regions within the field of view. These ambiguities are resolved by combining the readings from the fine phase antenna pair with the readings from the coarse phase

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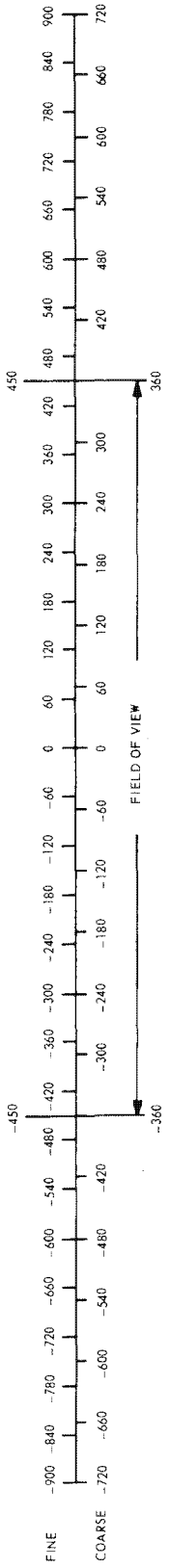

FIGURE 3.3-3. HORIZON-TO-HORIZON PHASE RELATIONSHIP

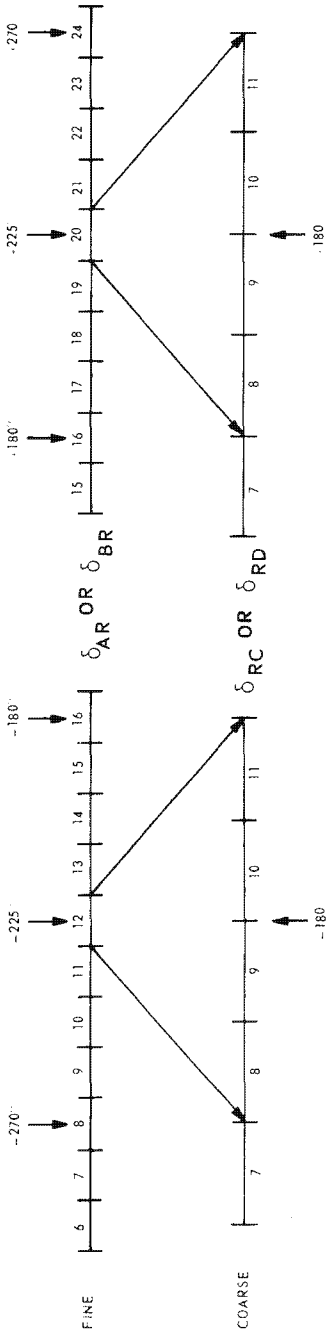

FIGURE 3.3-4. UNAMBIGUOUS PHASE GROUPING

antenna pair. Antenna spacing of 3.0λ and 2.4λ (determined at the low frequency limit of each band) for the fine and coarse phase pairs, respectively, allows phase crossover to coincide only at boresight.

Figure 3.3-4 illustrates the coding method used to resolve ambiguities. In the example shown, the -180° and +180° coarse and the -225° and +225° fine phase positions are resolved into unambiguous locations by using both the coarse and fine phase information. Horizon-to-horizon encoding intervals are shown in Table 3.3-1.

Ambiguity removal techniques are developed in greater detail in Appendix C of LTVE Document No. 52000-R378, Technical Description Report for Setter 1B System.

3.4 Antenna Amplitude Response

The ambiguity removal technique used for Reaper fails to give correct results at certain large off-boresight angles; the phase tracking error of the D/F antennas also increases at large off-boresight angles. For these reasons, a phase field-of-view is set up which prevents the system from processing signals arriving from large off-boresight angles. Signals from off-boresight angles where the ambiguity removal technique does not provide satisfactory results are inhibited on the basis of amplitude-ratio measurements.

The amplitude-ratio-inhibit function is obtained by comparing the mode 2 output of the dual-mode spiral antenna

TABLE 3.3-1

FINE PHASE POSITION HORIZON-TO-HORIZON

Fine Ø Deg. e.	Dec. Eq. of Fine Ø	Dec. Eq. of Coarse Ø	Fine Ø Deg. e.	Dec. Eq. of Fine Ø	Dec. Eq. of Coarse Ø
-900.00	16	18,19,0,1	-450.00	24	18,19,0,1
-888.75	17	18,19,0,1	-438.75	25	18,19,0,1
-877.50	18	19,0-2	-427.50	26	19,0-2
-866.25	19	19.0-2	-416.25	27	19,0-2
-855.00	20	0-3	-405.00	28	0-3
-843.75	21	0-3	-393.75	29	0-3
-832.50	22	1-4	-382.50	30	1-4
-821.25	23	1-4	-371.25	31	1-4
-810.00	24	2-5	-360.00	0	2-5
-798.75	25	2-5	-348.75	1	2-5
-787.50	26	3-6	-337.50	2	3-6
-776.25	27	3-6	-326.25	3	3-6
-765.00	28	4-7	-315.00	4	4-7
-753.75	29	4-7	-303.75	5	4-7
-742.50	30	5-8	-292.50	6	5-8
-731.25	31	5-8	-281.25	7	5-8
-720.00	0	6-9	-270.00	8	6-9
-708.75	1	6-9	-258.75	9	6-9
-697.50	2	7-10	-247.50	10	7-10
-686.25	3	7-10	-236.25	11	7-10
-675.00	4	8-11	-225.00	12	8-11
-663.75	5	8-11	-213.75	13	8-11
-652.50	6	9-12	-202.50	14	9-12
-641.25	7	9-12	-191.25	15	9-12
-630.00	8	10-13	-180.00	16	10-13
-618.75	9	10-13	-168.75	17	10-13
-607.50	10	11-14	-157.50	18	11-14
-596.25	11	11-14	-146.25	19	11-14
-585.00	12	12-15	-135.00	20	12-15
-573.75	13	12-15	-123.75	21	12-15
-562.50	14	13-16	-112.50	22	13-16
-551.25	15	13-16	-101.25	23	13-16
-540.00	16	14-17	-90.00	24	14-17
-528.75	17	14-17	-78.75	25	14-17
-517.50	18	15-18	-67.50	26	15-18
-506.25	19	15-18	-56.25	27	15-18
-495.00	20	16-19	-45.00	28	16-19
-483.75	21	16-19	-33.75	29	16-19
-472.50	22	17-19,0	-22.50	30	17-19,0
-461.25	23	17-19,0	-11.25	31	17-19,0

TABLE 3.3-1 (Cont'd)

FINE PHASE POSITION HORIZON-TO-HORIZON					
Fine Ø Deg. e.	Dec. Eq. of Fine Ø	Dec. Eq. of Coarse Ø	Fine Ø Deg. 2	Dec. Eq. of Fine Ø	Dec. Eq. of Coarse Ø
0°	0	18,19,0,1			
+11.25	1	18,19,0,1	+461.25	9	18,19,0,1
+22.50	2	19,0-2	+472.50	10	19,0-2
+33.75	3	19,0-2	+483.75	11	19,0-2
+45.00	4	0-3	+495.00	12	0-3
+56.25	5	0-3	+506.25	13	0-3
+67.50	6	1-4	+517.50	14	1-4
+78.75	7	1-4	+528.75	15	1-4
+90.00	8	2-5	+540.00	16	2-5
+101.25	9	2-5	+551.25	17	2-5
+112.50	10	3-6	+562.50	18	3-6
+123.75	11	3-6	+573.75	19	3-6
+135.00	12	4-7	+585.00	20	4-7
+146.25	13	4-7	+596.25	21	4-7
+157.50	14	5-8	+607.50	22	5-8
+168.75	15	5-8	+618.75	23	5-8
+180.00	16	6-9	+630.00	24	6-9
+191.25	17	6-9	+641.25	25	6-9
+202.50	18	7-10	+652.50	26	7-10
+213.75	19	7-10	+663.75	27	7-10
+225.00	20	8-11	+675.00	28	8-11
+236.25	21	8-11	+686.25	29	8-11
+247.50	22	9-12	+697.50	30	9-12
+258.75	23	9-12	+708.75	31	9-12
+270.00	24	10-13	+720.00	0	10-13
+281.25	25	10-13	+731.25	1	10-13
+292.50	26	11-14	+742.50	2	11-14
+303.75	27	11-14	+753.75	3	11-14
+315.00	28	12-15	+765.00	4	12-15
+326.25	29	12-15	+776.25	5	12-15
+337.50	30	13-16	+787.50	6	13-16
+348.75	31	13-16	+798.75	7	13-16
+360.00	0	14-17	+810.00	8	14-17
+371.25	1	14-17	+821.25	9	14-17
+382.50	2	15-18	+832.50	10	15-18
+393.75	3	15-18	+843.75	11	15-18
+405.00	4	16-19	+855.00	12	16-19
+416.25	5	16-19	+866.25	13	16-19
+427.50	6	17-19,0	+877.50	14	17-19,0
+438.75	7	17-19,0	+888.75	15	17-19,0
+450.00	8	18,19,0,1	+900.00	16	18,19,0,1

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to the signal in one of the conventional phase channels. The mode 2 response produces a pattern which has a null on boresight. The pattern of the phase horn is a conventional pattern, peaked on boresight. The difference in output power from the two antennas is a function of the off-boresight angle of an emitter. By sampling this difference for each received pulse, signals with large off-boresight angles-of-arrival can be detected and inhibited. Figure 3.4-1 illustrates the amplitude-ratio technique; a typical mode 2 response pattern is superimposed on the amplitude pattern of a phase horn.

3.5 Receiver Characteristics

Since the system is essentially a high frequency receiver, its ability to detect the presence of an emitter and extract information is limited by the presence of noise. Maximum sensitivity is limited by the noise produced in the system itself.

3.5.1 System Noise Figure

The overall noise figure of the Reaper receiver is determined by the noise figure of the IF preamplifier, the conversion loss and noise figure of the mixers, and the loss of the interconnecting cable between the system antennas and the mixers. These quantities are carefully controlled by in-house electrical performance specifications to yield an overall receiver noise figure of 8.5 db, measured at the input to the antenna interconnecting cable.

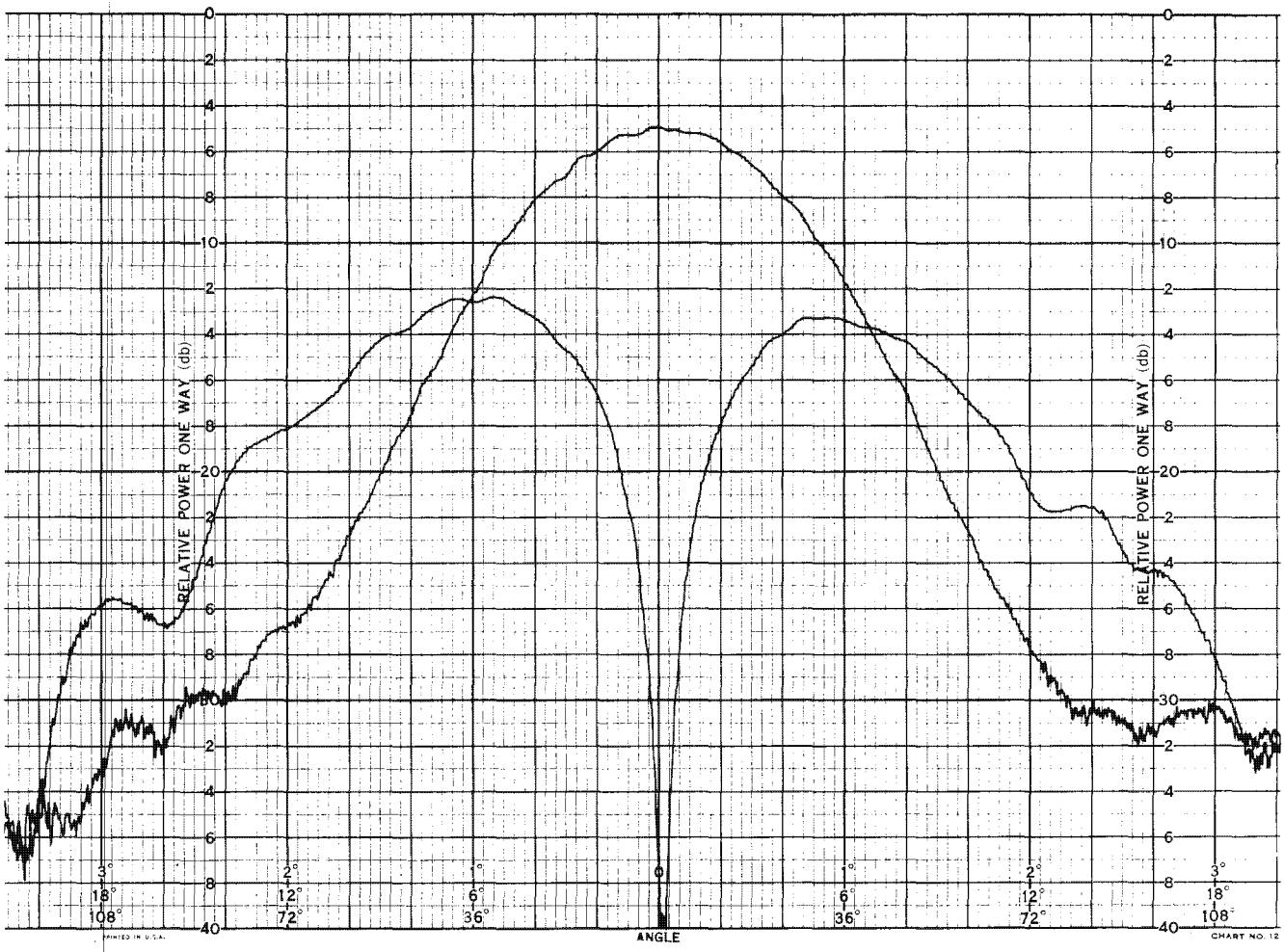

FIGURE 3.4-1 MODE 2 SPIRAL/PHASE RESPONSE

3.5.2 Equivalent Input Thermal Noise Power

The equivalent input noise power of a receiver is normally expressed in the following form.

Equivalent input noise power = N = FkTB watts

$= 4 \times 10^{-21}$ FB watts

where F = noise figure - the factor by which the equivalent input noise of the actual

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receiver exceeds that of an ideal reference.

k = 1.37 x 10^{-23} joule/°K = Boltzmann's constant.

T = absolute temperature of noise source - arbitrarily, 290°K.

B = equivalent rectangular noise bandwidth of the receiver in cycles per second.

For the Reaper receiver:

KT = -114 dbm

B = 7.32 MHz, or +8.64 db above 1 MHz

F = 8.5 db

KTBF = -96.86 dbm

The equivalent noise power referred to the input to the system receiver is -96.86 dbm.

3.5.3 Minimum Signal-to-Noise Ratio

The system is required to process a -93 dbm signal arriving from either 23 space degrees off boresight or from the edge of the phase field-of-view, whichever is less. The antenna gain at 23° off-boresight is 5 db minimum (linearly polarized signal). This yeilds a signal amplitude of -88 dbm into each receiver phase channel. The resulting signal to noise ratio is then

-88 - (-96.86) = 8.86 db

A minimum phase channel signal-to-noise ratio of 8.86 db will

be produced by any input signal which produces a minimum signal confirm decision.

3.5.4 Real/Image Signal Identification and Spurious Rejection Circuitry

The Reaper system processes both real and image signals when operating in any of the normal EOB readin modes. Real and image signals are defined in equation 3.5.4-1.

$$F\ (\text{real}) = {}^{F}\text{Local OSC} + {}^{F}\text{IF} \qquad (3.5.4\text{-}1a)$$

$$F\ (\text{image}) = {}^{F}\text{Local OSC} - {}^{F}\text{IF} \qquad (3.5.4\text{-}1b)$$

Since the phase characteristics of real and image signals are different, a signal must be identified conclusively as one or the other before valid location information can be obtained. Intermediate frequency signals can also be produced by either inband or out-of-band spurious signals which enter the mixers and heterodyne with the local oscillator. Spurious signals are not processed for EOB data and must be rejected and/or identified to prevent the EOB data from being degraded.

Spurious signals are rejected by three different techniques:

a) The system mixers have a minimum of 58-db rejection for in-band spurious signals,

b) A band pass filter is included between the F_1 antenna and the F_1 channel mixer making it impossible for an out of band signal to generate a real/image confirm pulse, and

c) The real/image circuitry shown in Figure 3.5-1 has some inherent spurious rejection capability.

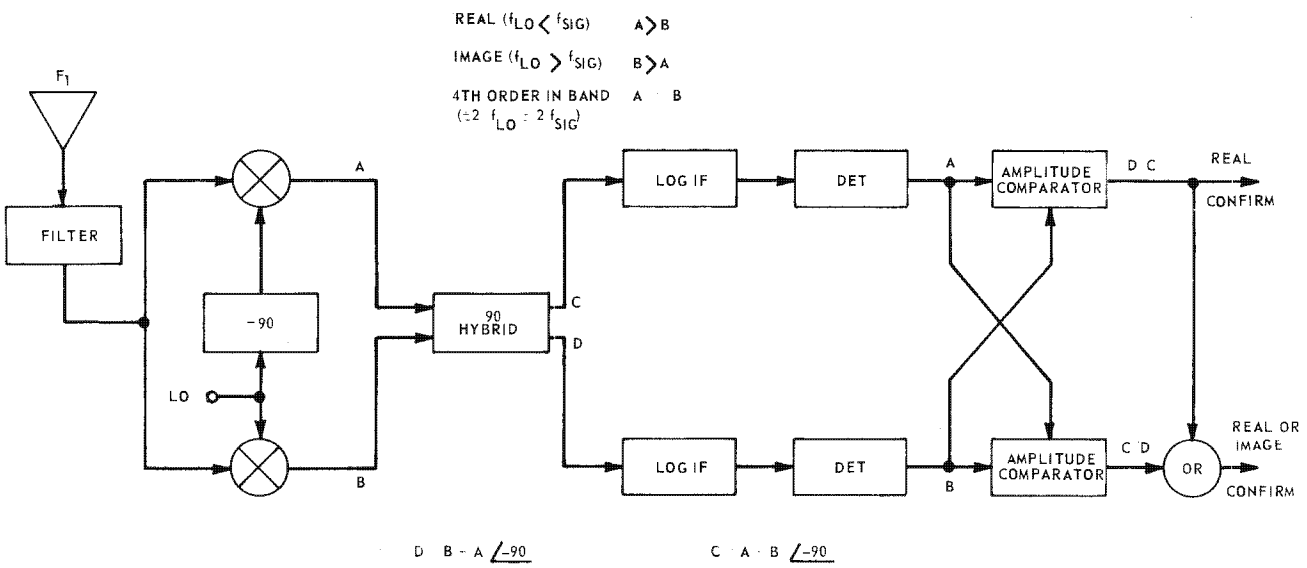

FIGURE 3.5-1. REAL/IMAGE CONFIRM LOGIC

An analysis of the real/image identification circuits performance shows that reals and images are positively identified, and the in-band spurious response is positively rejected. Due to equipment limitations a C/D or D/C ratio on the order of 15 db is the maximum attainable value, and provides quite satisfactory results. The analysis is shown below.

$A = \cos(M\omega_r t - N\omega_o t + N90)$ $\quad B = \cos(M\omega_r t - N\omega_o t)$

$C = A + B \angle -90$ $\quad D = B + A \angle -90$

$$C/D = \frac{\cos[(M\omega_r - N\omega_o)t + N90] + \cos[(M\omega_r - N\omega_o t - 90]}{\cos[(M\omega_r - N\omega_o)t] + \cos[(M\omega_r - N\omega_o + N90 - 90]}$$

$$D/C = \frac{1}{C/D}$$

If a real signal is received, M = N = +1

$$C/D = \frac{\cos[(\omega_r - \omega_o)t + 90] + \cos[(\omega_r - \omega_o)t - 90]}{\cos[(\omega_r - \omega_o)t] + \cos[(\omega_r - \omega_o)t + 90 - 90]} = 0, \quad D/C$$

If an image signal is received, M = N = -1

$$C/D = \frac{\cos[(-\omega_r + \omega_o)t - 90] + \cos[(-\omega_r + \omega_o)t - 90)]}{\cos[(-\omega_r + \omega_o)t] + \cos[(M\omega_r - N\omega_o)t - 90 - 90]} = \rightarrow \infty, \quad D/C = 0$$

If M = N = +2, a spurious signal is being received

$$C/D = \frac{\cos[(\omega_r - \omega_o)2t + 180] + \cos[(\omega_r - \omega_o)2t - 90]}{\cos[(\omega_r - \omega_o)2t] + \cos[(\omega_r - \omega_o)2t + 90]} = \frac{1 \angle 225°}{1 \angle 45°}$$

$C/D = 1$, $D/C = 1$

If M = N = -2, a spurious signal is being received

$$C/D = \frac{\cos[(\omega_o - \omega_r)2t - 180] + \cos[(\omega_o - \omega_r)2t - 90]}{\cos[(\omega_o - \omega_r)2t] + \cos[(\omega_o - \omega_r)2t - 270]} = \frac{1 \angle 225°}{1 \angle 45°}$$

$C/D = 1$, $D/C = 1$

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3.6 Error Analysis

3.6.1 Phase Error

The primary function of the payload is to accurately locate both pulsed and CW electromagnetic emitters. The location accuracy depends on phase measurement accuracy and the ability to resolve ambiguities in the phase measurements.

The phase error budget for the system is summarized in Table 3.6-1. The errors are listed by sections for convenience. For each error source a maximum error is given with the resulting rms error. The maximum error (with only one exception) is the limit value of a uniformly distributed set of errors, for which:

$$\text{rms} = \frac{\text{max. error}}{\sqrt{3}} \qquad (3.6.1\text{-}1)$$

The IF deck temperature error is assumed to have a triangular, rather than a uniform distribution. The effects of noise on phase error are reduced by averaging the location information from eight received pulses from the same location.

3.6.2 Location Accuracy

It has been shown in the addendum to the fourth Reaper design review, "Discussion of Reaper Location Error," that the radius, $\Delta L/95\%$, of a circle centered at an emitter's location within which 95% of the locations indicated by the Reaper payload will fall is given by equation 3.6.2-1.

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TABLE 3.6-1 PREDICTED ELECTRICAL PHASE ERRORS

	MAX ERRORS	RMS ERRORS	VARIANCE
ANTENNAS			
Reflections	±4.0°	2.31°	5.32
Polarization	±7.0°	4.04°	16.32
Mutual Coupling	±2.0°	1.15°	1.32
Feed Structure Phasing	±4.0°	2.31°	5.32
Mechanical Tolerances	±2.0°	1.15°	1.32
TOTAL PHASE VARIANCE DUE TO ANTENNAS			29.60
RF CIRCUITRY			
Main Stripline Phase Tracking	±5.0°	2.89°	8.33
20 db Coupler	±0.5°	.289°	.0833
TOTAL PHASE VARIANCE DUE TO RF CIRCUITS			8.4133
IF CIRCUITRY			
Frequency	±4.5°	2.60°	6.76
Dynamic Range	±3.6°	2.08°	4.33
Amplitude Unbalance	±2.8°	1.62°	2.62
Temperature	±7.3°	2.98°	8.87
TOTAL PHASE VARIANCE DUE TO IF CIRCUITS			22.58
PHASE ENCODER			
Quantizing Error (Fine)	±5.62°	3.25°	10.58
Reading Error (Fine)	±3.61°	2.08°	4.35
TOTAL PHASE VARIANCE DUE TO PHASE ENCODER			14.93
TOTAL SYSTEMATIC ERRORS		8.68°	75.52
Noise Error (Single Pulse) S/N = 8.86 db		16.3°	
Noise Error (8 Pulses averaged)		5.75°	33.1
TOTAL SYSTEMATIC AND NOISE (8 PULSES AVERAGED) PER CHANNEL		10.42°	108.62

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$$\Delta L/95\% = \frac{268 \text{ N.MI. } \tan \theta/95\%}{(\cos \theta)^2} \quad . \qquad (3.6.2\text{-}1)$$

where

$$\Delta\theta/95\% = \frac{.39 \text{ (RMS Elect Deg. Error)}}{df/\lambda \quad (1.1) \quad \cos \theta} \qquad (3.6.2\text{-}2)$$

Substituting values from Table 3.6-1 gives

$$\theta/95\% = \frac{.39 \times 10.42}{3 \quad (1.1) \quad (.92)} = 1.338 \qquad (3.6.2\text{-}3)$$

$$L/95\% = \frac{268 \tan 1.338}{(.92)^2} = 7.39 \text{ N.MI.} \qquad (3.6.2\text{-}4)$$

Equation 3.6.2-4 shows that over flat earth with coarse and fine phase readings optimally combined, a 95% confidence radial error of 7.39 nautical miles can be expected (worst case S/N ratio).

3.6.3 False Alarm Rate

If the noise entering an IF filter is assumed to be Gaussian noise, then the probability density function is given by:

$$p(v)\, dv = \frac{1}{\sqrt{2\pi \Psi_o}} \exp - \frac{-v^2}{2\Psi_o} \, dv \qquad (3.6.3\text{-}1)$$

where $p(v)dv$ is the probability of finding the noise voltage v between the values of v and v + dv, Ψ_o is the variance, or mean squared value of the noise voltage, and the mean value of Ψ_o is taken to be zero. If the IF bandwidth is small compared to the mid-frequency, the probability density of the envelope of the noise voltage output is given by equation (3.6.3-2).

$$p(R)dR = \frac{R}{\Psi_o} \exp \frac{-R^2}{2\Psi_o} dR \qquad (3.6.3\text{-}2)$$

R of equation (3.6.3-2) is the amplitude of the envelope of the filter output. Equation (3.6.4-2) is a form of the Rayleigh probability-density function.

The false alarm probability (P_{fa}) is the probability that the noise voltage envelope will exceed the voltage threshold VT and is given by equation 3.6.3-3.

$$P_{fa}(V_T < R < \infty) = \int_{V_T}^{\infty} \frac{R}{\Psi_o} \exp \frac{-R^2}{2\Psi_o} dR \qquad (3.6.3\text{-}3)$$

$$P_{fa} = \exp - \frac{V_T^2}{2\Psi_o}$$

The average time interval between threshold (V_T) crossings with a positive slope by noise alone is defined as T_{fa} and is shown in Figure 3.6-1. The average duration (T_d) of a noise pulse once the pulse has crossed the V_T threshold is approximately the reciprocal of the bandwidth B, Figure 3.6-1. In case of the envelope detector the bandwidth is B_{IF} and T_d is:

$$T_d = \frac{1}{B_{IF}} \qquad (3.6.3\text{-}4)$$

The false alarm probability P_{fa} can also be defined as the duration of time the noise envelope is actually above the V_T threshold to the total time the noise could have been above the threshold.

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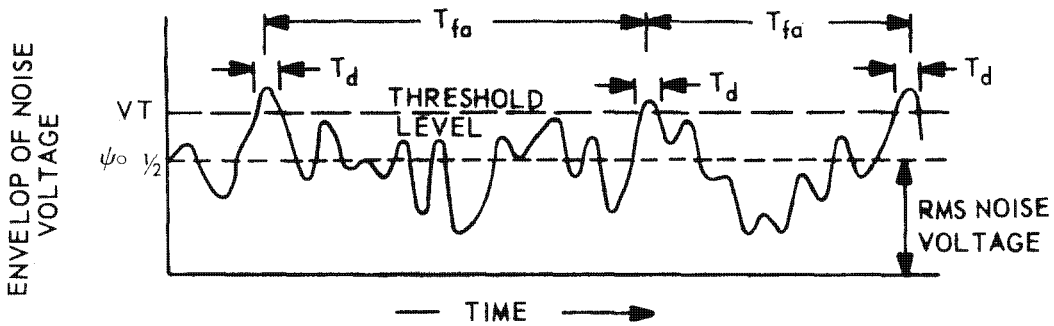

FIGURE 3.6-1 AVERAGE NOISE VOLTAGE CROSSING VS TIME

$$P_{fa} = \frac{T_d}{T_{fa}} = \frac{1}{T_{fa} B_{IF}} \qquad (3.6.3\text{-}5)$$

Equation (3.6.3-5) can be solved for the average false alarm interval (T_{fa}) and combined with equation (3.6.3-3) to give:

$$T_{fa} = \frac{1}{P_{fa} B_{IF}} = \frac{1}{B_{IF}} \exp \frac{VT^2}{2\psi_o} \qquad (3.6.3\text{-}6)$$

If the bandwidth B_{IF} of equation (3.6.3-6) is expressed in cycles per second then the average false alarm interval T_{fa} is also in seconds.

In the system receiver, four phase channels are added for signal-to-noise ratio enhancement. This yields approximately a 6-db signal-to-noise ratio improvement over that available in one phase channel alone. This means that a 14.86-db S/N ratio is available for the Tmin decision, and an 11.86-db S/N ratio is available for the signal identification

decision. The SI decision must be made sooner than the Tmin decision due to the response time of the receiver gating circuits. A relatively high SI false alarm rate is forced upon the Reaper receiver by the requirement of a relatively high single pulse probability of detection.

A probability of signal detection of 85% is felt to be the minimum acceptable value in the SI circuits. A probability of detection threshold yielding P_o = 85% on a 11.86 db signal to noise ratio signal results in a probability of false alarm of 10^{-4}. Then

$$T_{FA} = \frac{1}{P_{FA}\ B_{IF}} = \frac{1}{10^{-4} \times 6 \times 10^{6}} = 1.67 \times 10^{-3} \text{ sec}$$

and slightly more than three false alarms per 6.14 millisecond dwell can be expected. The Reaper system requires five microseconds to recover from a false alarm, therefore, fifteen microseconds (.245%) of each 6.14 millisecond dwell period is used in processing and rejecting false alarms.

A higher false alarm probability can be tolerated in each of the confirm/inhibit channels because they are gated off most of the time; the only time they are gated on is when an SI pulse is present. The resulting probability of detection is still only 85%, however, due to the lower signal to noise ratio signal from which each confirm/inhibit decision must be made. The resulting overall probability of detection is then given by equation 3.6.3-7.

$$P_D(sys) = P_D(SI) \times P_D(Tmin) \times P_D(A/R\ Inhibit) \times P_D(Freq.\ Conf.) = .85 \times .99 \times .85 \times .85 = 61.5\% \qquad (3.6.3\text{-}7)$$

The overall probability of detection increases quite rapidly as the input signal amplitude increases above Tmin.

3.6.4 Amplitude Error

The predicted amplitude errors in the Reaper System are given in Table 3.6.2. The errors are presented by section for convenience. For each error source a maximum error is listed with the associated RMS error. The RMS error (1σ) is calculated for each subassembly assuming that the given maximum error is the limiting value of a uniformly distributed set of errors.

$$RMS = \frac{\text{max. error}}{\sqrt{3}} \qquad (3.6.3\text{-}1)$$

In addition to the amplitude errors contributed by each subassembly, the accuracy of the amplitude measurement is degraded by the presence of noise. The relative RMS amplitude error assuming a worst case signal to noise ratio of 8.86 db is given by equation 3.6.3-2.

$$\delta A/A = \frac{1}{\sqrt{2S/N}} = \frac{1}{\sqrt{2\ (7.7)}} = .255, \text{ or } 1 \text{ db}$$

As may be seen from Table 3.6-2, the resulting amplitude RMS error including encoding error is 2.068 db. If the assumption is made that the central limit theorem of statistics holds for

TABLE 3.6-2 AMPLITUDE ERROR ANALYSIS

	MAX ERROR (DB)	RMS ERROR (DB)
ANTENNAS		
1. Amplitude variation with frequency (worst case, on boresight)	±1.0	± .577
2. Signal Polarization	± .5	± .289
RF SUBASSEMBLY		
1. Gain variation due to all causes	±2.0	±1.15
IF DECK		
1. Gain variation with frequency, temperature, and dynamic range	±1.75	1.01
2. Encoding Error	±1.25	.723
3. Noise Error		1.0
TOTAL 1 σ (RMS) Amplitude Measurement Error = 2.068 db		

the error tabulation of Table 3.6-2, the 5 db error specification represents the 2.42 σ point on a Gaussian distribution, and will be exceeded less than 2% of the time under worst case signal-to-noise ratio conditions.

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3.6.5 Pulse Repetition Interval Error

The pulse repetition interval (PRI) of the incoming pulse train is measured by recording the time of arrival of each pulse and subtracting the time-of-arrival (TOA) of each pulse from the TOA of the preceding pulse.

For example:

$$PRI\ (1\text{-}2) = (TOA)_2 - (TOA)_1 \qquad (3.6.4\text{-}1)$$

$$PRI\ (2\text{-}3) = (TOA)_3 - (TOA)_2 \qquad (3.6.4\text{-}1a)$$

$$PRI\ (3\text{-}4) = (TOA)_4 - (TOA)_3 \qquad (3.6.4\text{-}1b)$$

This analysis assumes that the only sources of error in this parameter are variations of SI due to noise and the quantizing error associated with the difference in arrival times. Worst case variations of SI due to the relatively low signal-to-noise ratio signal available from which to make the SI decisions are given by equation 3.6.4-2.

$$\delta t = \frac{1}{2\pi f \sqrt{2s/N}} \qquad (3.6.4\text{-}2)$$

$$= \frac{1}{2\pi \times 20 \times 10^6 \times \sqrt{2(15.4)}} = .001435 \text{ usec}$$

The RMS error resulting from measurements between two pulses of the same signal to noise ratio is

$$\sqrt{2} \times 1.435 \times 10^{-9} = 2.03 \times 10^{-9} \text{ sec.}$$

However, the 2.03×10^{-9} second noise error is insignificant compared to the $\pm \frac{1}{2}$ microsecond encoding error. The total maximum encoding error resulting from measuring the fine time

[redacted]00

of arrival of two successive pulses is 1 microsecond, the value allowed by the performance specification summarized in 2.5.11.4.

3.6.6 Pulse Width Error

The payload measures the pulse width (PW) of the incoming signal by gating an internal counter (0.125 microseconds equals one clock period). The PW counter is activated by the leading edge of the incoming SI (Signal Identification) pulse and deactivated by the trailing edge of the SI pulse. Payload measuring resolution is $\pm$ 1 clock pulse. As shown in equation 3.6.4, the maximum noise induced error from either a leading edge of one pulse to the leading edge of the following pulse, or from the leading edge of one pulse to the trailing edge of the same pulse is 2.03×10^{-9} seconds. However, considerable pulse width stretching takes place in the SI pulse width as a function of input signal amplitude. It is this pulse stretching which sets the minimum achievable pulse width error, not the combination of noise and encoding errors.

3.6.7 Frequency Error

The Reaper frequency error budget is shown in Table 3.6-3. The errors are all relatively self explanatory with the possible exception of the noise error, which will be explained in greater detail.

The Reaper IF deck obtains fine frequency information using a modified phase channel, as explained in Sections 4.5.8. A 37.5 nanosecond delay line is inserted in one input

[redacted]

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TABLE 3.6-3 REAPER FREQUENCY ERROR BUDGET (WORST CASE)

	MAX. VALUE	RMS	VARIANCE
RF SUBASSEMBLY			
1. Local Oscillator Error	+5.4	+3.12	9.72
IF DECK			
1. Reading Error	± .3	.173	.03
2. Encoding Error	± .5	.289	.0834
3. Noise Error		1.16	1.35
TOTAL		3.344	11.1834

$3.344/1800 = .186\%$

to the phase detector and the phase of the delayed IF signal compared to the phase of the undelayed IF signal. At 20 MHz, a phase shift of

$$20 \times 10^6 \times 360 \times 37.5 \times 10^{-9} = 270°$$

results. At 21 MHz, a 284° shift is produced, and a 19 MHz IF frequency yields a 256° phase shift between the two signals, yielding a frequency-phase gain of 14 electrical degrees per megahertz. But 1 σ phase errors of 16.3° are produced by an 8.86 db signal-to-noise ratio signal, so a worst case noise produced RMS frequency error of 1.16 MHz can be expected. This value is shown in Table 3.6-3. The resulting worst case RMS error of 0.186% of the received frequency is easily within the specification inhibit of 0.3%.

3.7 Reaper Effective Sensitivity To Three Emitters Of Interest As A Function Of Location

Figures 3.7-1, 3.7-2, and 3.7-3 show power into the Reaper mixer for three different hypothetical radars as a function of distance from satellite nadir. The characteristics of the radars are shown below; the transmitting antenna patterns from document AA13009, dated 29 December 1966, were used.

[redacted]

Radar A is similar to the [redacted] missile control radar used in the Soviet Union and deployed in other Soviet Bloc countries. Radar B resembles the [redacted] Communist early warning radar. The parameters of radar C resemble those of the [redacted] height finding radar used in the USSR. The curves in the three figures represent the maximum possible power input to the Reaper receiver; minor lobe peaks on the transmitter's antenna patterns were used in all cases. The curves shown are plots of equation 3.7-1.

$$P_r = P_T + G_T + G_R - P.L. \qquad (3.7\text{-}1)$$

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where

P_r = receiver power, dbm

P_T = transmitter power, dbm

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G_T = Transmitting antenna gain in the direction of the satellite, db

G_R = Reaper antenna gain in the direction of the transmitter, db

P.L. = Path loss between transmitting and receiving antennas, db

The transmitter power was selected according to radar type. G_T was read directly from the appropriate antenna pattern contained in Document AA13009. G_R was read from the appropriate Reaper antenna patterns, and P.L. was obtained from a path loss nomogram.

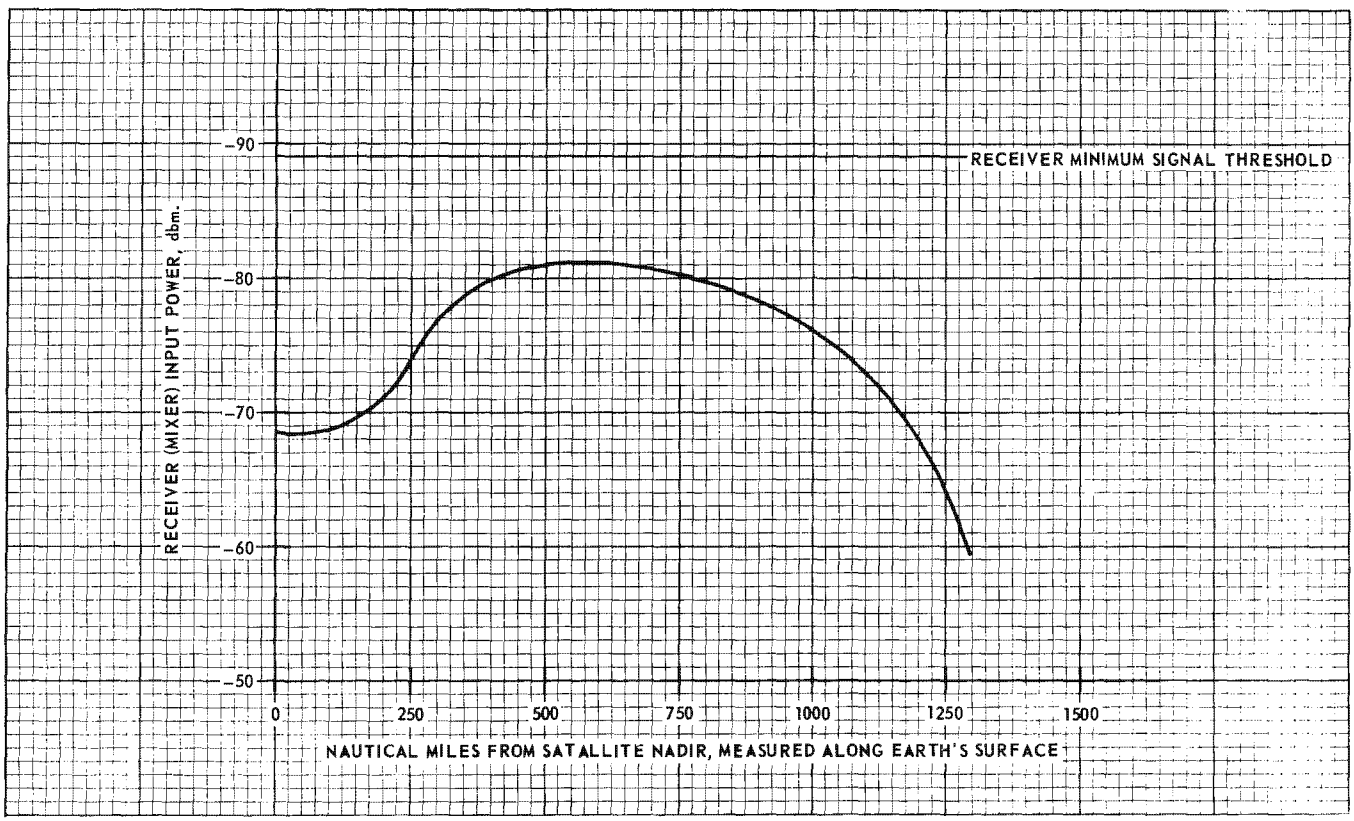

Figure 3.7-1. Receiver Input vs Distance For Type A Radar

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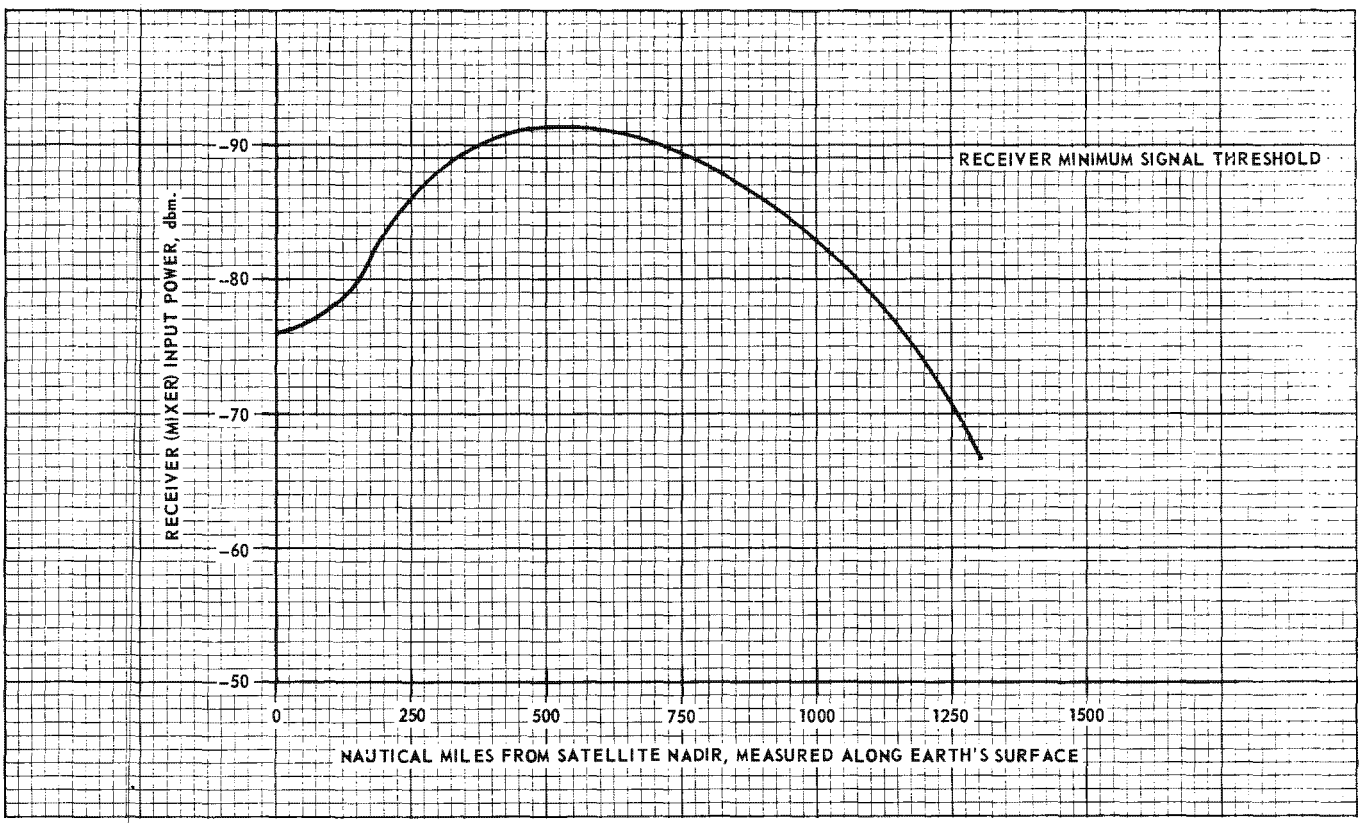
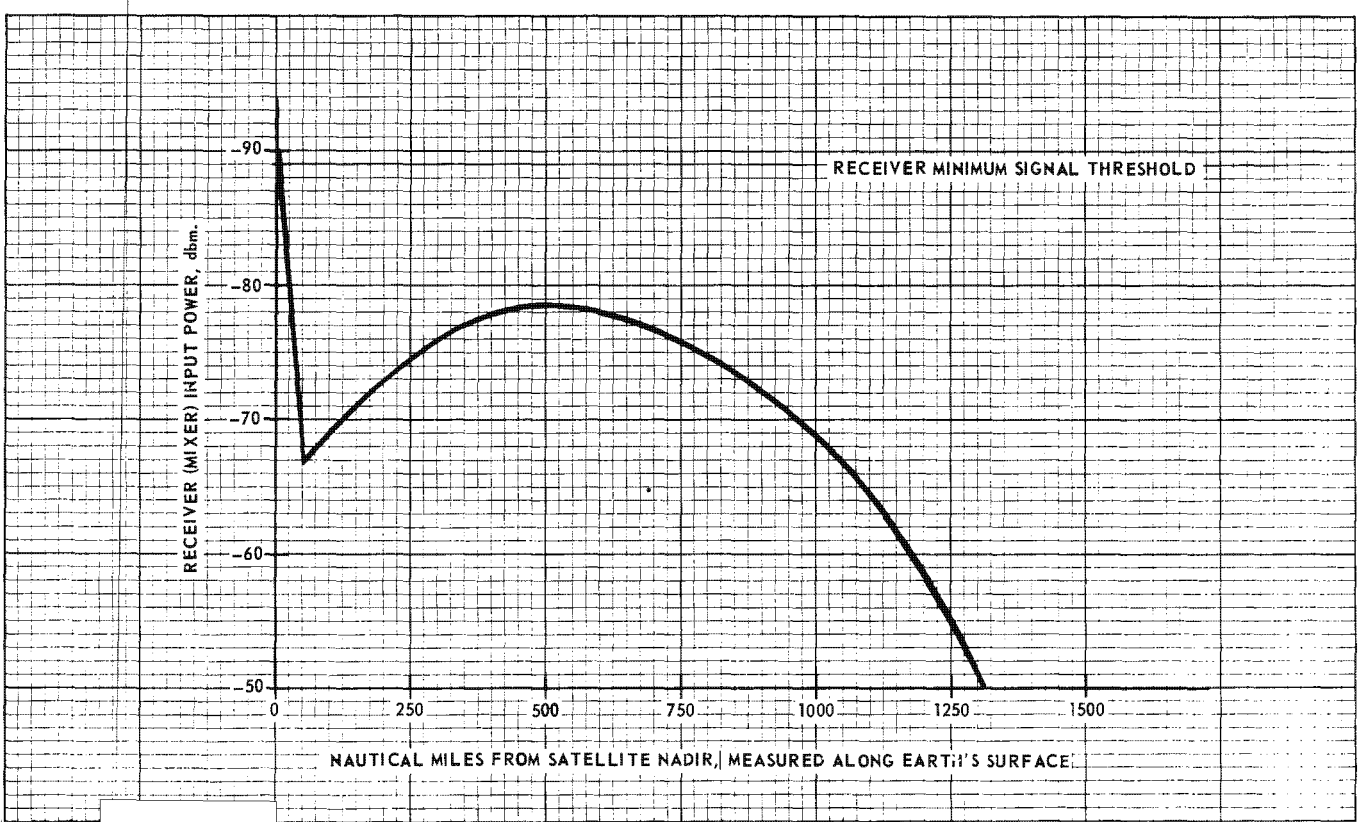


Figure 3.7-2. Receiver Input vs Distance For Type B Radar



.7-3. Receiver Input vs Distance For Type C Radar

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A constant orbit altitude of 268 nautical miles was used. The transmitting antenna was assumed to be stationary with its main lobe perpendicular to the earth radius at that point. The plane of the satellite's orbit was assumed to include the major lobe so that with the transmitter located at the satellite's horizon (approximately 1300 N.Mi. from nadir), the main transmitter lobe illuminated the satellite. The curves show that the types A and C radars can be processed all the way from the satellite nadir to the satellite horizon. The type B radar can be processed over 75% of the distance from nadir to the horizon.

4.0 DESIGN

4.1 Antennas

4.1.1 Requirements

The basic information upon which the system operates is derived initially by the antennas, making the characteristics of the antenna a vital factor in the system performance. Five antennas, in each frequency band, are used for phase information. The phase antennas of one band are frequency scaled versions of the antennas of the other band. Each band incorporates a sixth antenna which operates in two modes simultaneously. One mode supplies amplitude information to the spurious-identification channel. The other mode, in conjunction with a phase antenna, supplies amplitude information to the amplitude-ratio channel.

The antennas are circularly polarized so that they are insensitive to variations in polarization of the incident wave fronts. To achieve a uniform response in azimuth, the antennas have conically symmetrical patterns.

Amplitude-ratio requirements relates the allowable sidelobe level of the phase antennas to the pattern of the inhibit antenna over an angle of boresight ± 70 degrees. Beyond this angle, the sidelobes should be as low as achievable, consistent with other requirements, to reduce pattern degradation due to antenna environment.

4.1.2 Design Consideration

One of the primary problems in designing a cir-

cularly polarized horn antenna is that the amplitude distribution across the aperture tends to be uniform in the E plane and sinusoidal in the H plane. There is a difference in pattern characteristic in the two planes as a consequence of the difference in aperture excitation. This problem is easily overcome in a linearly polarized antenna by the simple expedient of providing different apertures in the two planes. In the case of a circularly polarized antenna, however, the problem is compounded by the fact that the aperture must be constant for any cut through it and must be different for the two polarizations.

This result was achieved by the use of radial fins (septa) within the aperture. Since the septa will short out an electric field in the radial direction and have little or no affect on fields transverse to them, it is possible to provide an aperture that is larger in theH plane than in the E plane which will be independent of the orientation of the horn.

Antenna pattern sidelobes are determined by the aperture illumination function. A uniform excitation (such as is in the E plane of a horn) results in high sidelobes; a tapered excitation (such as is in the H plane) results in a low sidelobe level. In the present case, the uniformity of the E field was somewhat alleviated by the septa since the observed sidelobe values in the E plane were below the level that would

normally be expected.

Further reduction of the sidelobes and almost complete suppression of back lobe radiation was obtained by the addition of a choke around the periphery of the horn aperture. This choke serves to suppress the currents (induced by the fringe fields) that tend to flow on the outside walls of the horn to create a back lobe and contribute to sidelobes.

Two methods of obtaining circularly polarized excitation were considered and investigated. The most common method for obtaining circular polarization is to launch a linearly polarized wave in a circular or rectangular wave guide and to convert to circular polarization by inducing a 90-degree differential phase shift in one component of the energy. This method was investigated first and found to be unusable.

The primary problem in this approach was the fact that a very limited run of waveguide was available to perform the differential phase shift. It was found that the phasing element was extremely frequency sensitive (even in terms of the frequency band of interest) because the wavelength within the guide varies appreciably for small frequency changes. This method also suffers somewhat in repeatability of the design since the adjustment of the phasing elements is fairly critical.

The second method which has been investigated for obtaining circular polarization avoids the requirement for a substantial length of waveguide by initially launching in a

circularly polarized mode. This mode is used in the system. Circular polarization is accomplished by equally dividing the signal, incorporating a 90-degree differential phase shift, and launching the two components with two orthogonal planar elements. There are two primary problems in this approach: obtaining the phase shift and power split, and the mutual coupling between the feed elements.

The first problem was solved by the use of symmetrical transmission line couplers. The second problem was solved by use of a symmetrical wave launching device. The device converts less energy into the higher order waveguide modes which provide the coupling between the orthogonal elements. Four probes, spaced at 90 degree increments around a circular wave guide provide for launching a circularly polarized mode and has a symmetry required for low mutual coupling between orthogonal pairs. Since each pair of opposite probes penetrate the wave guide wall from opposing directions, their voltages have a phase relation of 180 degrees producing addition within the wave guide.

A circularly polarized wave is excited in the circular waveguide by using four probes, 180-degree hybrid and two 90 degree couplers. Stripline construction is used to build and connect the various elements, including the probes, without utilizing many connectors and line lengths whose dimensions are critical. Stripline construction also is capable of a higher

degree of repeatability in production units.

Dual mode antennas are generally used to generate two patterns simultaneously. One pattern, the sum mode pattern, is characterized by maximum gain in the boresight direction. The other pattern, difference mode, is characterized by a null or minimum gain on axis and the maximum gain occurring at some angle between boresight and 90 degrees.

A 4-arm, cavity backed, Archimedean spiral is one of the simplest forms of the circularly polarized, dual mode antennas.

The principle problem arising with this antenna is the theoretical consideration that the radiation occurs from a one wavelength aperture at all frequencies. This imposes a natural pattern, hence a gain limitation, on the antenna restricting the use of this antenna to situations wherein the pattern and gain associated with a one wavelength aperture are suitable. This problem may be overcome to some extent by the addition of a flare to increase the capture aperture of the spiral.

The four arms of the spiral are excited with the same phase relations as described for the 4-probe veed of phase horn to generate the sum mode. For generation of the difference mode, opposite spiral arms are connected in phase with a 180 degree relation to the adjacent arms. These relations are obtained with the use of three 4-port, 180-degree hybrids

and one 90-degree, 3-db coupler. Tapered lines are utilized to match the spiral impedances to the 50 ohm transmission line components.

The gain of an antenna may be specified as a maximum gain, or the gain may be specified to be the maximum possible at some angle other than that at which the maximum gain occurs. The aperture size that gives maximum gain at 23° off boresight was determined from an analysis making use of the parabolic approximation, and an empirical relationship between gain, beamwidth and efficiency.

Pattern approximation:

$$G(\theta x) = G(0) - 3\left(\frac{\theta x}{\theta \text{ HPBW}}\right)^2$$

Gain - Beamwidth Relation:

$$G \max = \frac{K}{\theta_E \ \theta_H}$$

where:

$G(\theta x)$ is the gain at some angle in db.

$G(0)$ is the maximum gain in db.

θx is the angle at which the gain is desired.

θ HPBW is the half power beamwidth.

K is a constant related to the efficiency of the antenna

θ_E, θ_H are the half power beamwidths in the E and H planes respectively ($\theta_E = \theta_H$ for the purposes of the analysis)

G(max) is the ratio of the gain of the antenna to that of an

isotropic antenna:

$$Go = 10 \log G \max = 10 \log \frac{K}{(\theta \text{ HPBW})^2}$$

$$G(\theta) = 10 \log K - \frac{20}{2.3} \text{Ln } \theta \text{ HPBW} - 3 \left(\frac{Qx}{\theta \text{ HPBW}}\right)^2$$

$G(\theta x)$ is then maximized with respect to θ HPBW:

$$\frac{d\ G(\theta x)}{d\ \theta \text{ HPBS}} = 0 - \frac{20}{2.3} \cdot \frac{1}{\theta \text{ HPBW}} + 6 \frac{(\theta x)^2}{(\theta \text{ HPBW})^3} = 0$$

$$\theta^2 \text{ HPBW} = \frac{6(\theta x)^2}{20} \quad 2.3 = 6.9\ (\theta x)^2$$

By substitution:

$$G(0) = 10 \log \frac{K}{0.69(\theta x)^2}$$

Let K = 32000:

$$G(0) = 10 \log \frac{32000}{0.69}(46)^2 = 13.42 \text{ db}$$

By substitution:

$$G(23) = 13.42 - 3\left(\frac{1}{.69}\right) = 9.08 \text{ db}$$

There is a loss of 3 db occasioned by a circularly polarized antenna receiving linear polarization so that the useful gain at 23° is:

9.08 - 3 = 6.08 db.

To examine the physical size of the antenna, Southworth's approximate formula for conical horns is used:

$$G = 5\ \underline{D}^2$$

Where D is the diameter in the same units as wavelengths:

$$D/\lambda = \frac{22}{5} = 2.1$$

So that a conical horn of approximately 2 wavelengths

50X1

diameter at the aperture is required.

4.1.3 Development

The development of the antennas involved a considerable amount of experimental investigation. Information had been gained in past programs in regard to septa and peripheral chokes over limited bandwidths. For example it had been found that 24 septa of a certain thickness and taper provide good pattern symmetry whereas 12 septa do not. In a similar manner, it had been found that the beam shape is dependent upon the height and length of the septa, the total aperture, and the horn taper angle. Additionally, all of these factors are interrelated to a considerable degree wherein a change in one results in changes to one or more of the others. The adjustment of these elements to produce the optimum pattern over the bandwidth has been accomplished.

Figure 4.1-1 presents a set of patterns at three frequencies of the high band phase antenna. The E and H plane patterns are overlaid.

Figure 4.1-2 presents a set of patterns at three frequencies of the high band inhibit antenna, sum mode; and a similar pattern of a phase antenna overlaid. E and H planes are shown.

Figure 4.1-3 presents a set of patterns at three frequencies. The pattern of the high band inhibit antenna, difference mode, is shown with a similar pattern of a phase antenna overlaid. E and H planes are shown.

The development of the transmission line devices was accomplished in parts. The stripline 3-db, 90 degree couplers were developed. A Schiffman, 90-degree, section was then incorporated to form the 4-port, 180 degree hybrids. Probe transitions were matched to the waveguide separately. The different devices were then incorporated in a single stripline corporate feed.

4.1.4 Summary of Technical Specifications

A summary of the electrical specification is presented in Table 4.1-1. Gain is expressed in db above an istropic radiator as measured with a linearly polarized signal.

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TABLE 4.1-1 ANTENNA CHARACTERISTICS

VSWR

Phase Antenna ≤ 1.5 to 1 (50 ohm ref.)

Inhibit Antenna - Sum Mode ≤ 2 to 1 (50 ohm ref.)

Inhibit Antenna - Diff.Mode ≤ 2.5 to 1 (50 ohm ref.)

Coupler ≤ 1.3 to 1 (50 ohm ref.)

GAIN:

Phase Antenna

Hi Band

Freq mc	Gain db	Freq mc	Gain db
2440	7.5	3100	9.75
2600	8.0	3300	10.5
2950	9.0		

Lo Band

Freq mc	Gain db	Freq mc	Gain db
1800	7.5	2300	9.9
1950	8.25	2440	10.5
2100	8.9		

INHIBIT ANTENNA - SUM MODE: Gain ≤ 3 db of Phase Horn

AXIAL RATIO:

Phase Antenna ≤ 1.0 db

Inhibit Antenna - Sum Mode ≤ 1.0 db

COUPLING RATIO

All Couplers 20 db ± 1 db

TABLE 4.1-1 ANTENNA CHARACTERISTICS (CONT'D)

AMPLITUDE RATIO:

At the lowest frequency of the band, the gain of the spiral, difference mode will be equal to or less than that of the phase antenna between the angles of 0° and 27° or greater. Between the angles of 50° and 80°, the spiral will have the greater gain by 4 db or more.

At the highest frequency, the gain of the spiral, difference mode, will be equal to or less than that of the phase antenna between the angles of 0° and 20° or greater. The gain of the spiral will be greater by 4 db between the angles of 35° and 80°. Straight line interpretation will apply to frequencies within the band. The above is to apply after 3 db has been added to the spiral, difference mode, gain.

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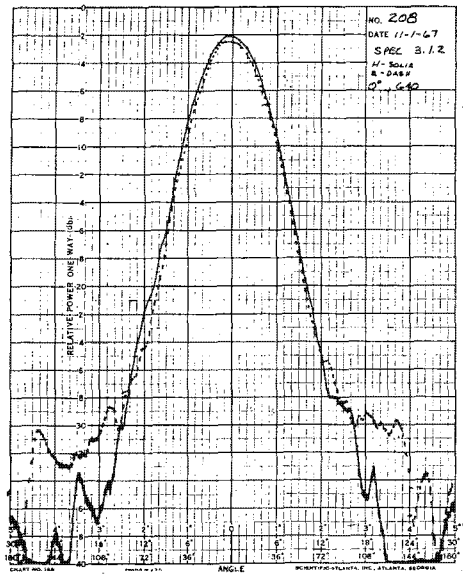
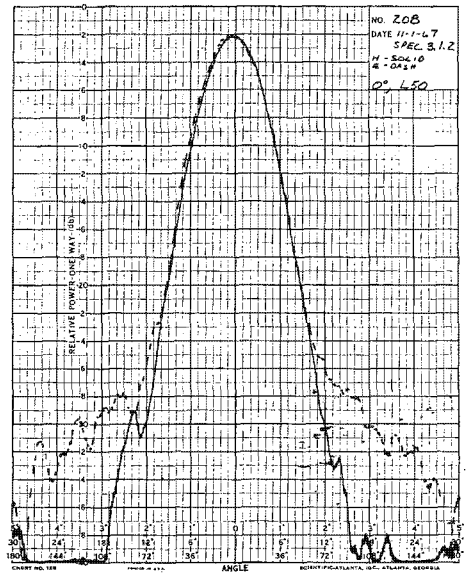
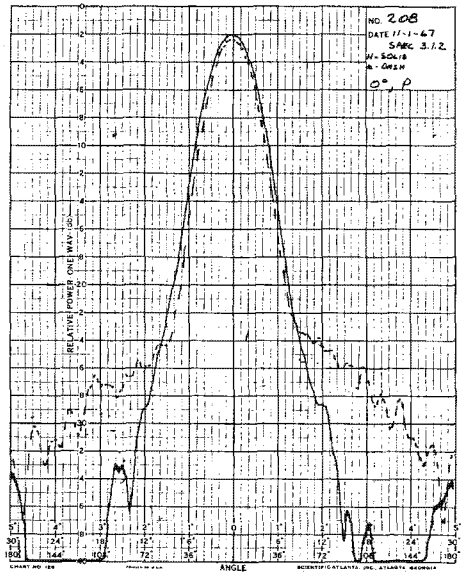


2440 MHz



2950 MHz



3300 MHz

Figure 4.1-1. E and H Plane Pattern of Phase Antennas

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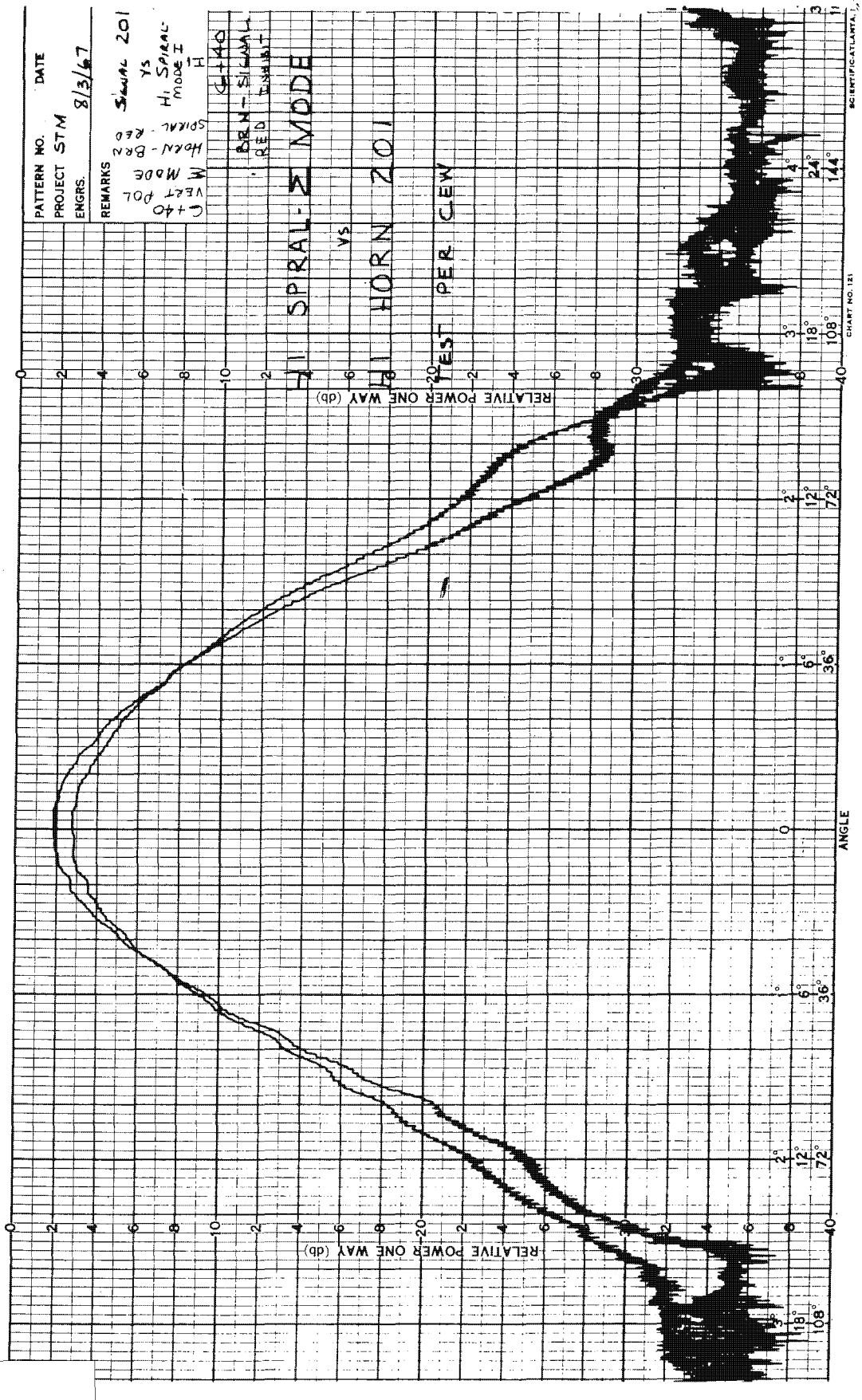


Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 1 of 6)

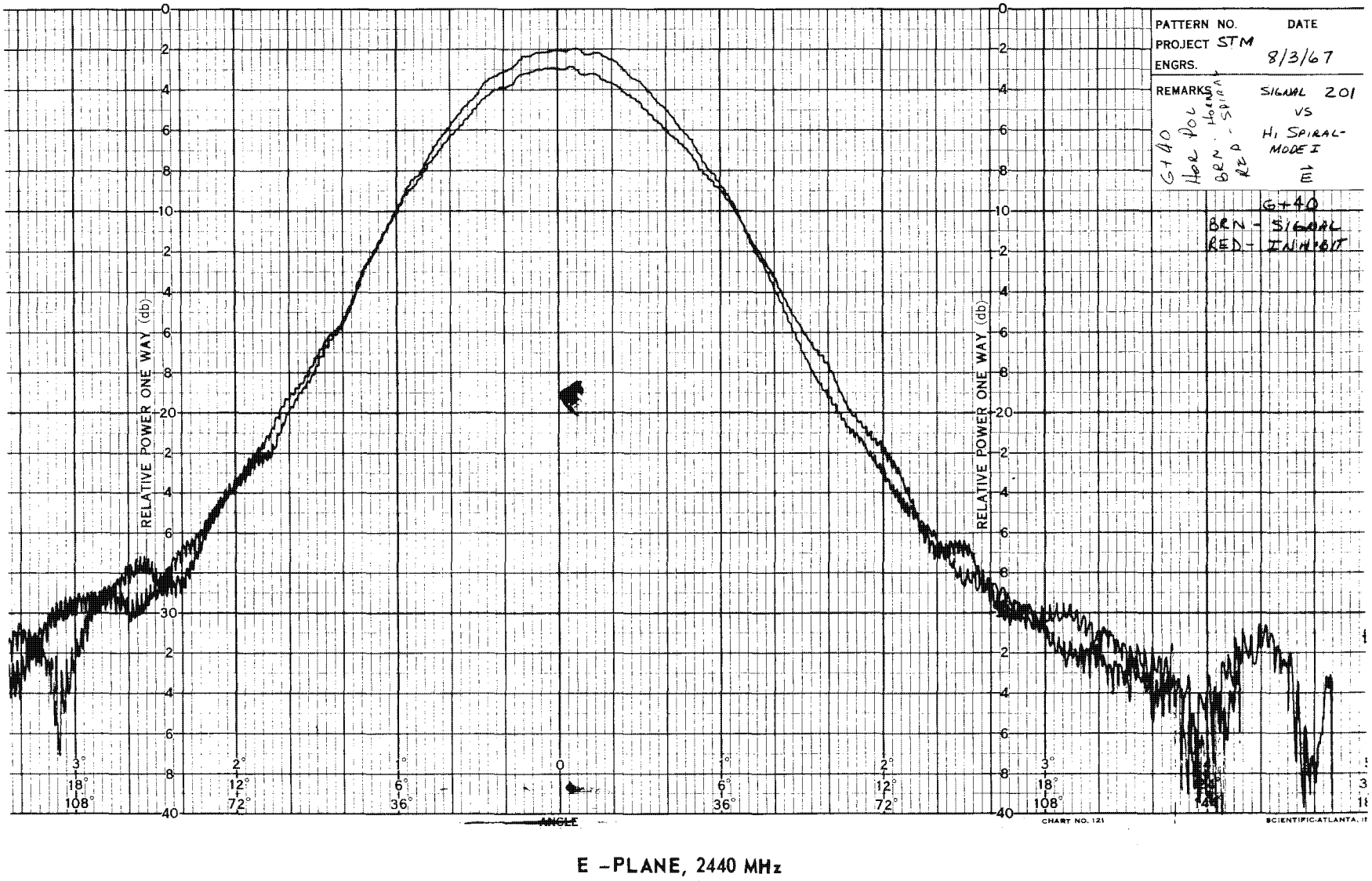
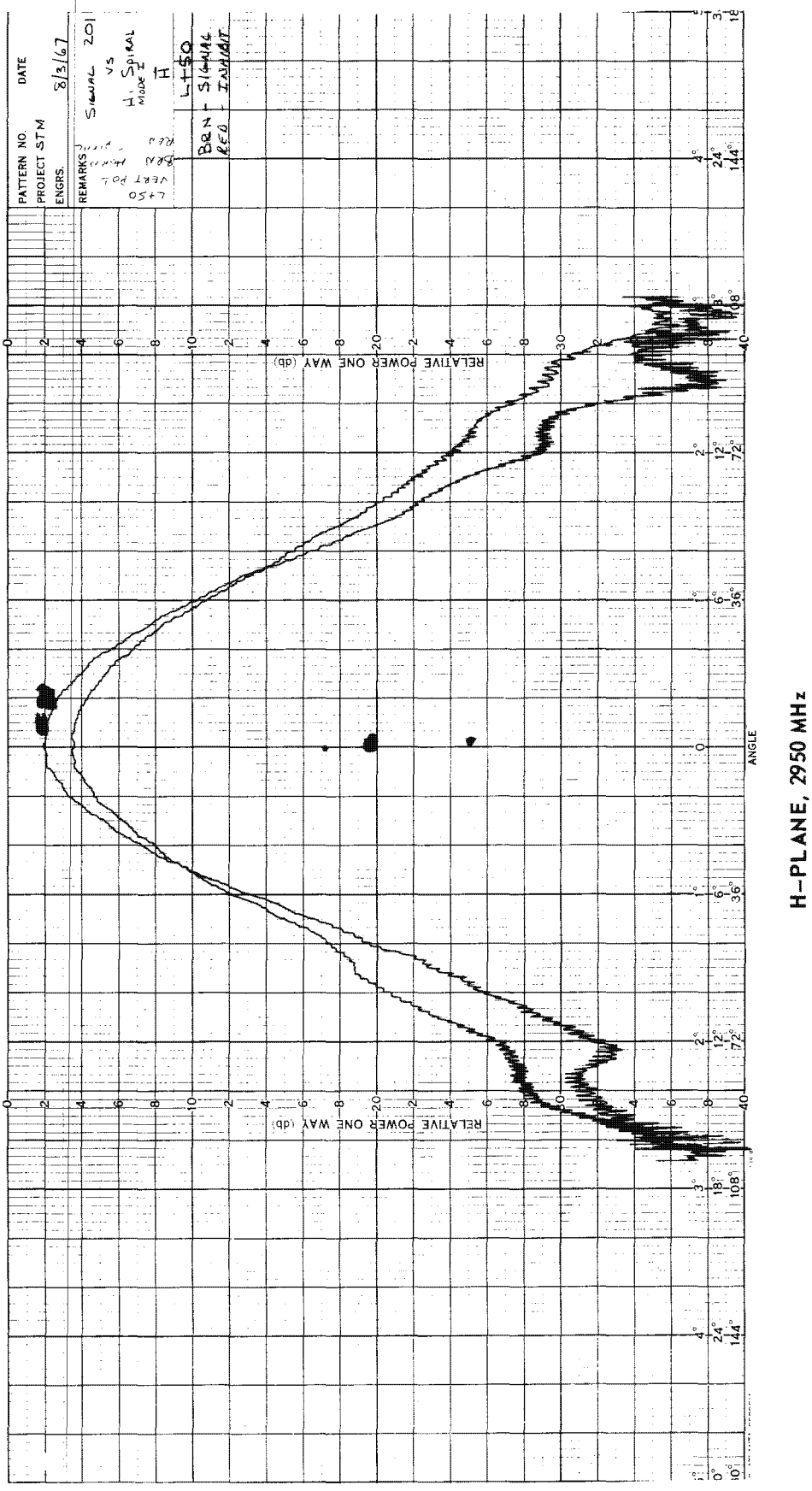


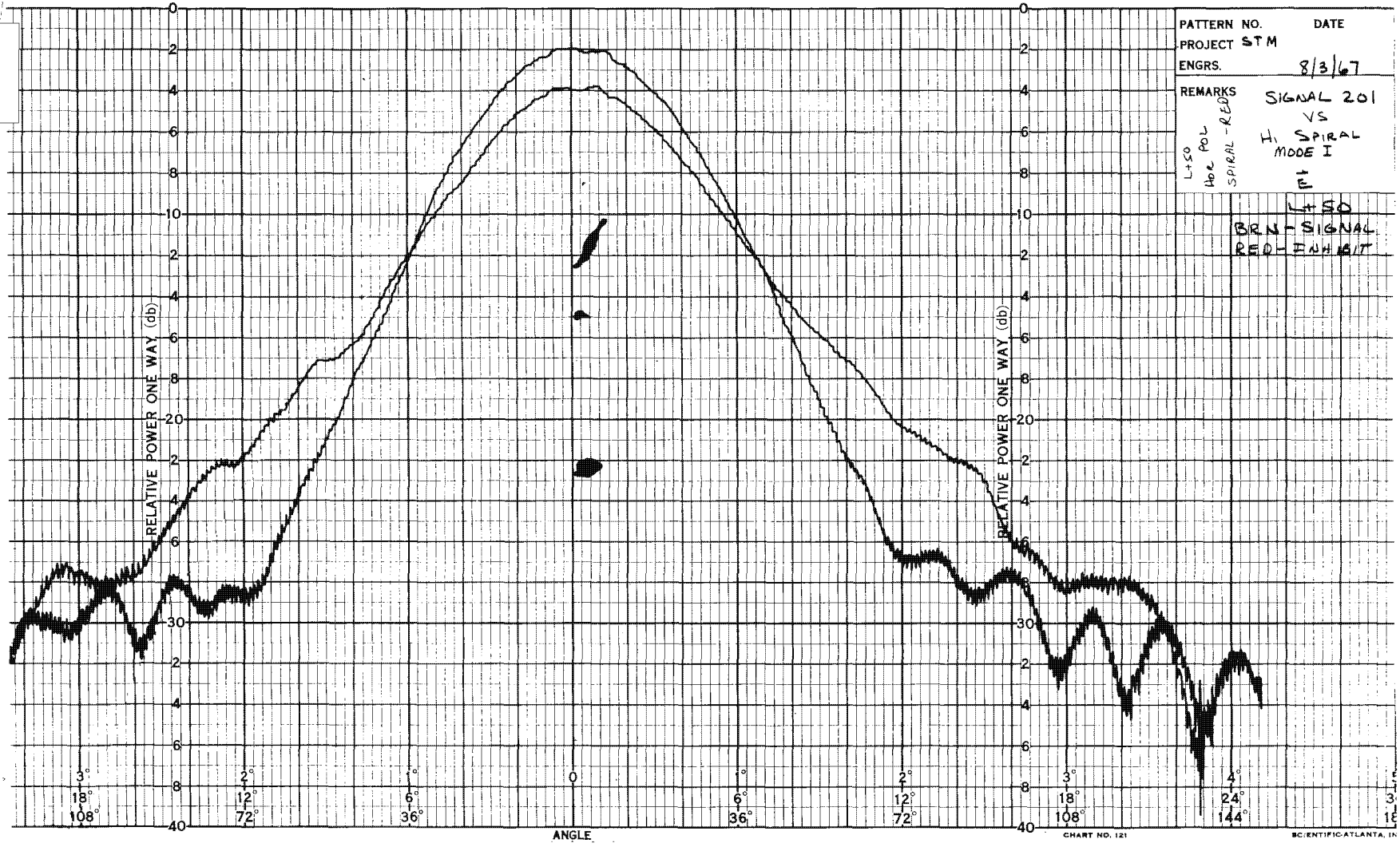
Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 2 of 6)



H-PLANE, 2950 MHz

Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 3 of 6)

50X1



E -PLANE, 2950 MHz

Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 4 of 6)

50X1

50X1

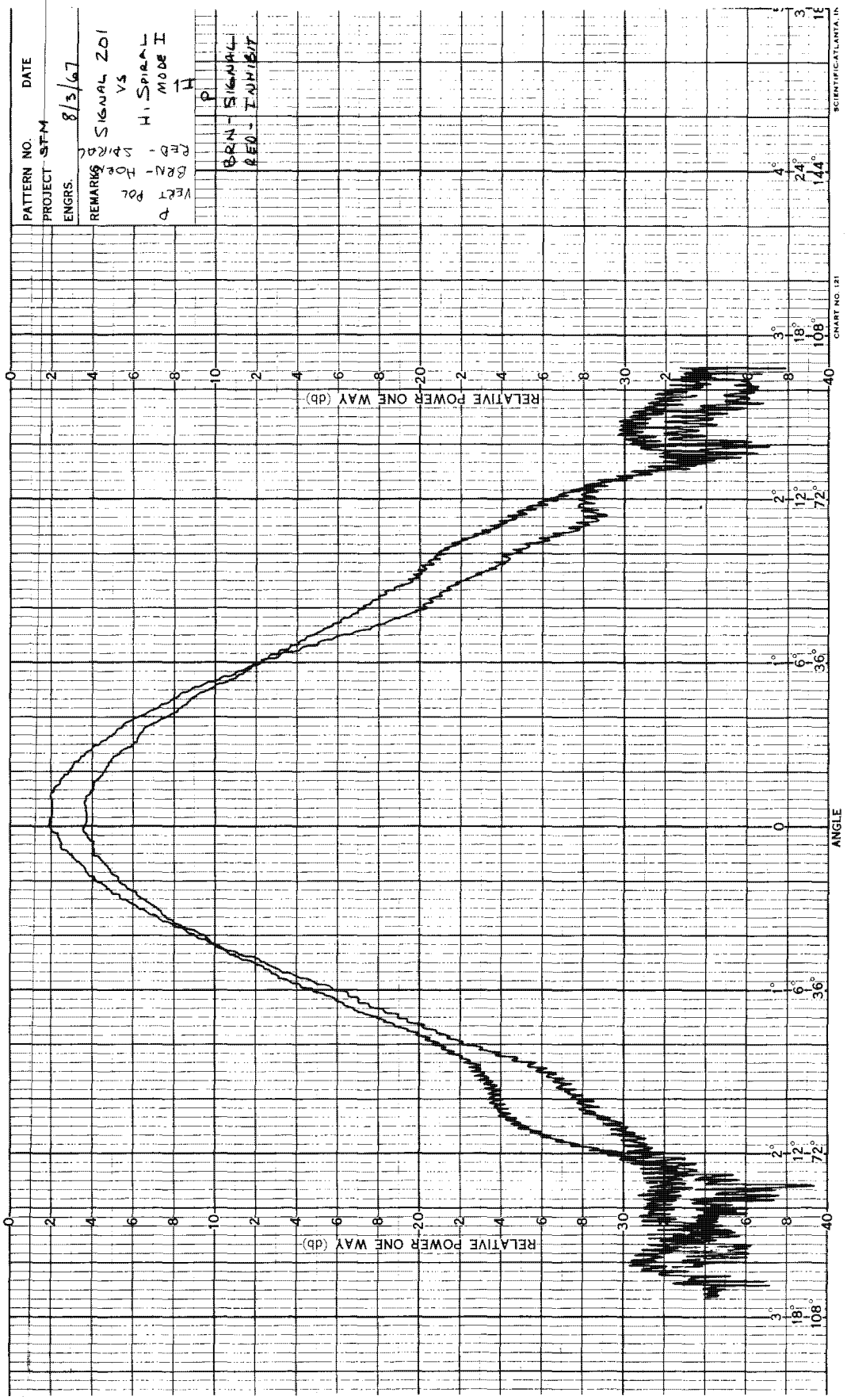
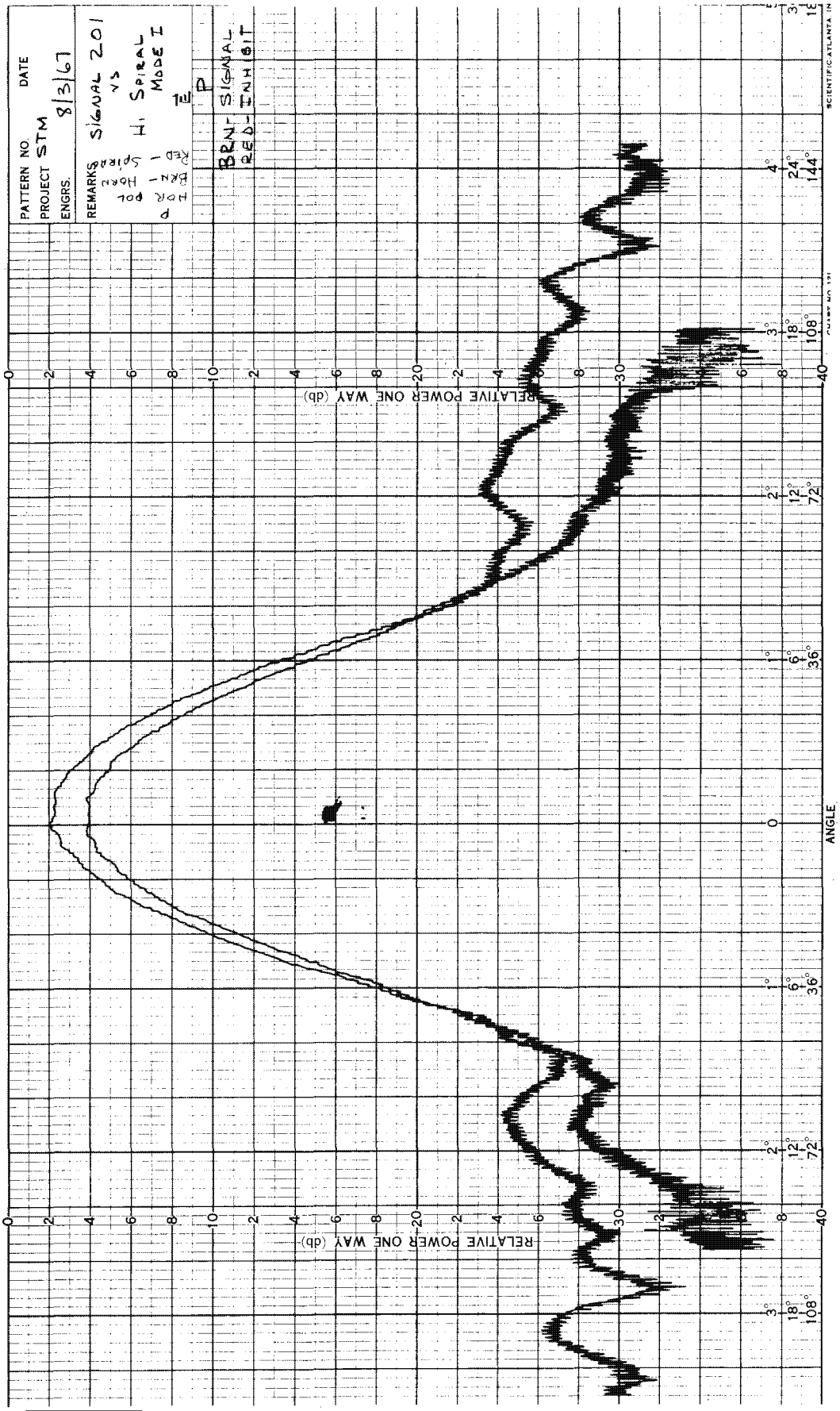


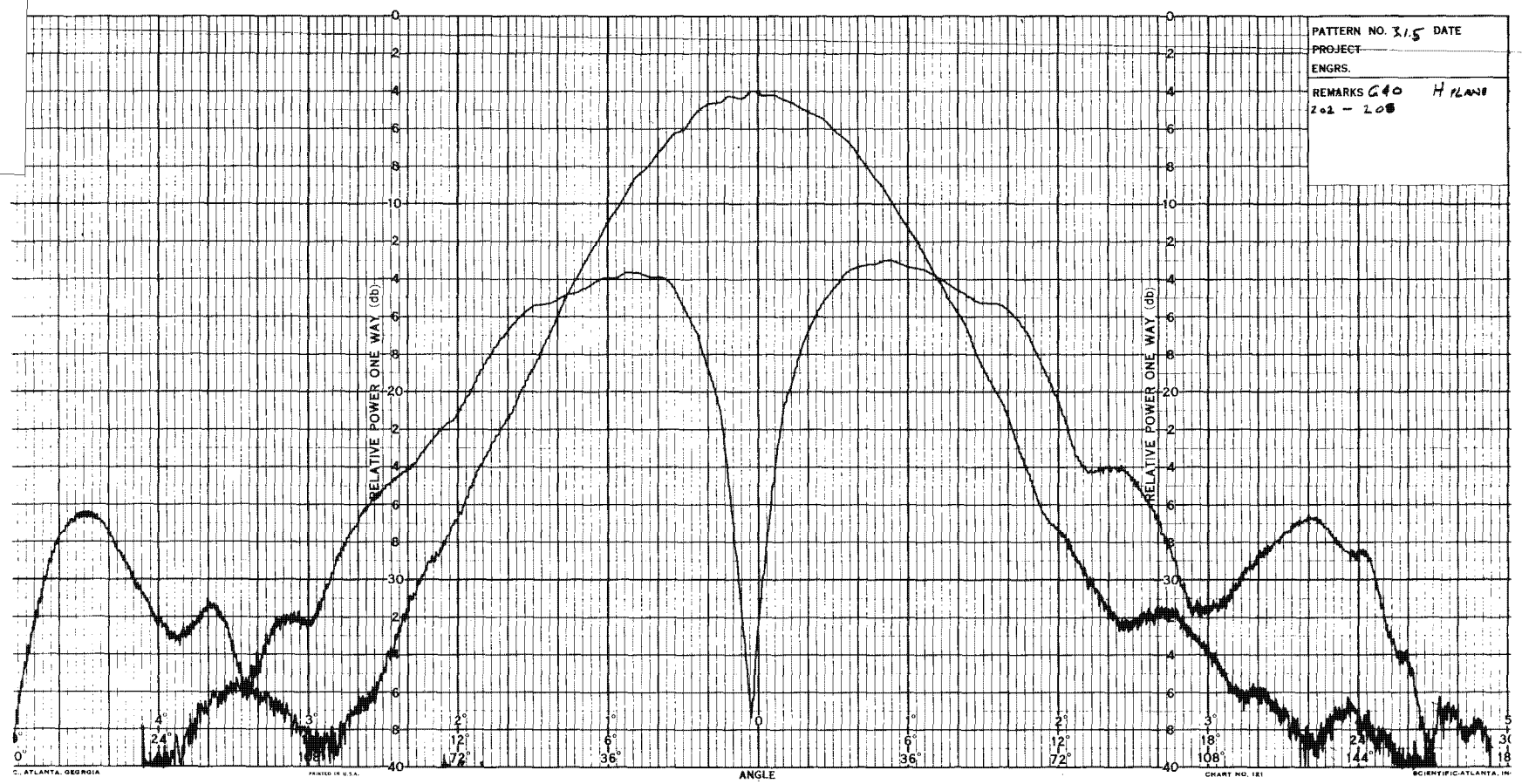
Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 5 of 6)

50X1



E-PLANE, 3300 MHz

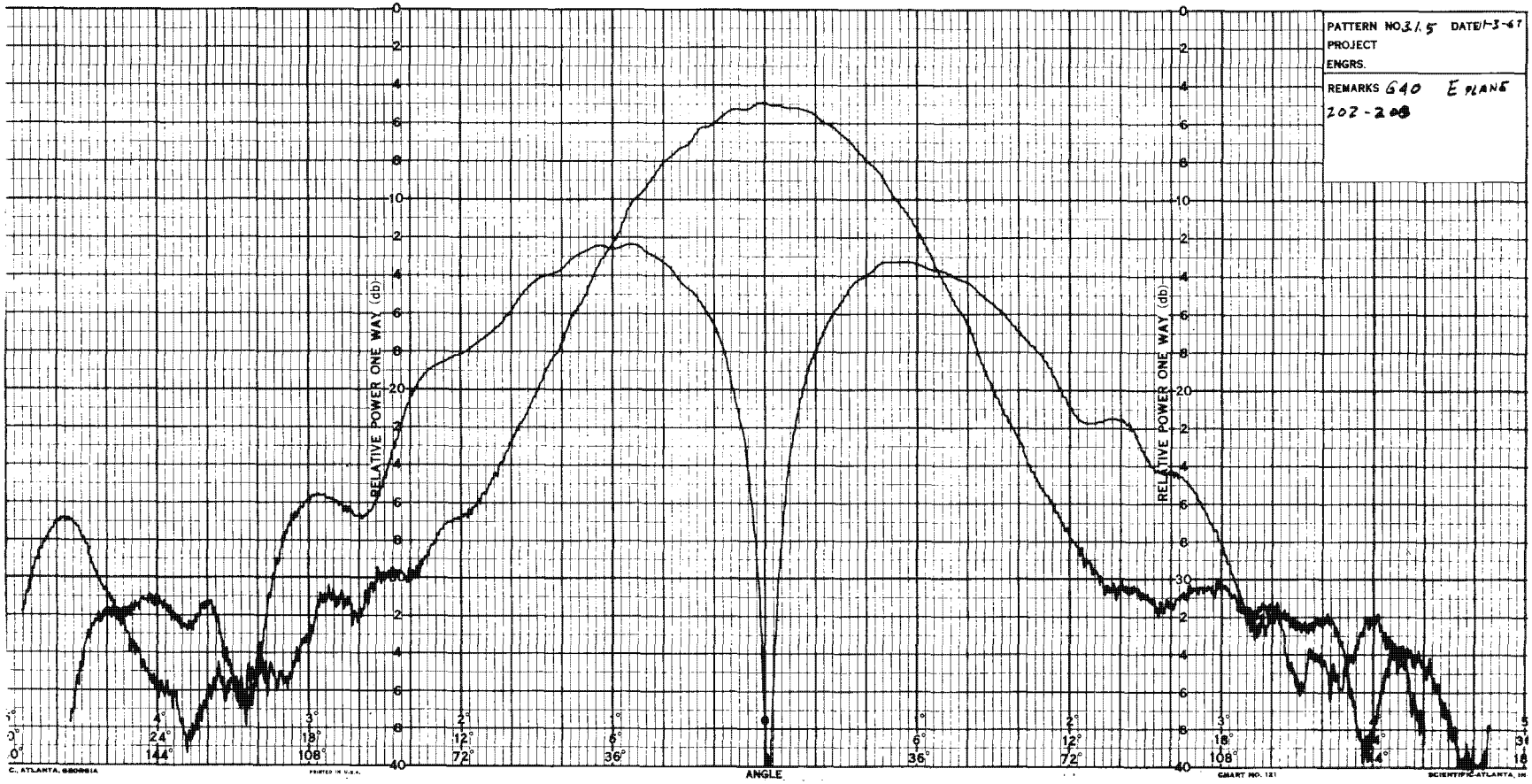
Figure 4.1-2. Spiral Sum Mode Compared to Phase Antenna (Sheet 6 of 6)



H-Plane, 2440 MHz

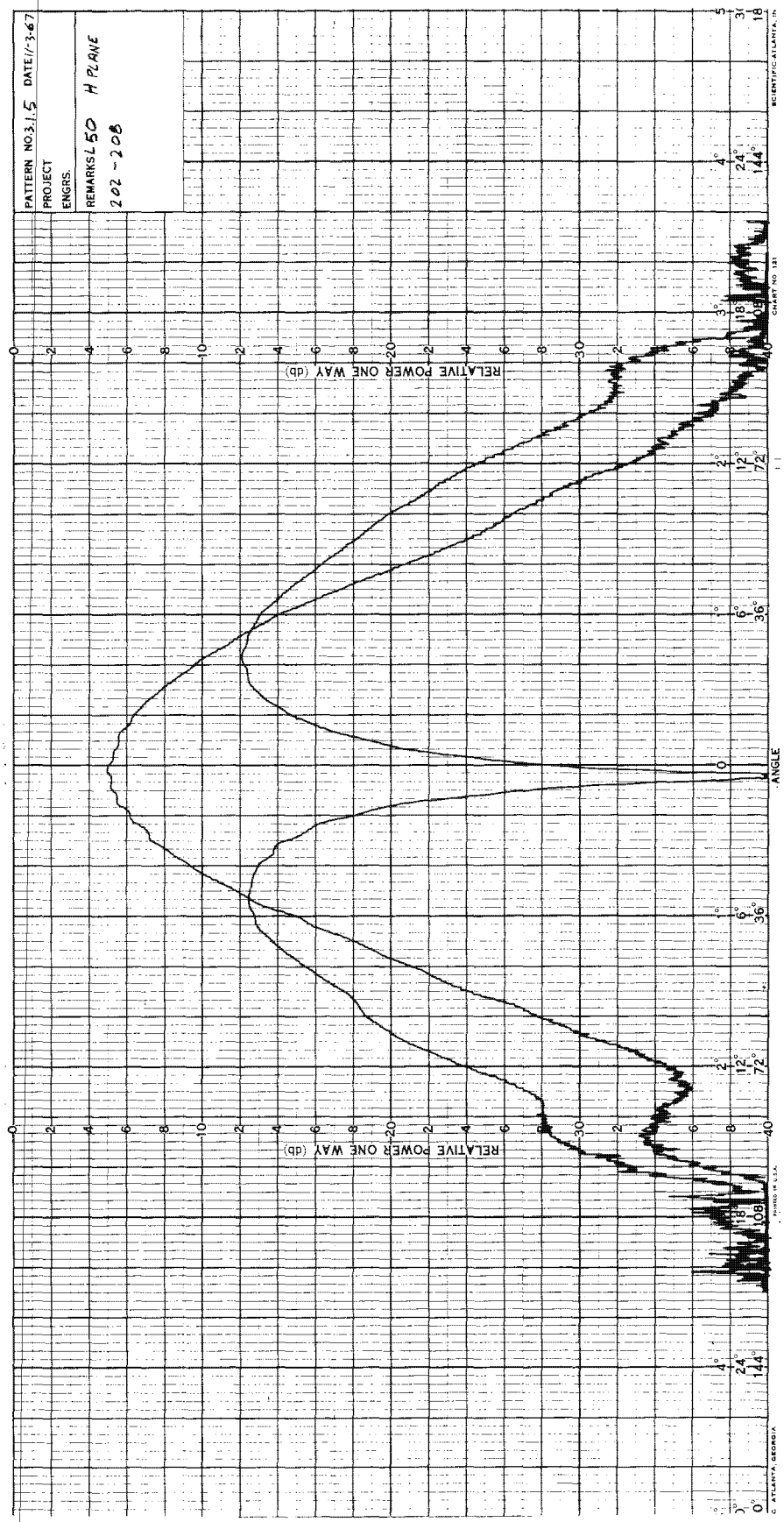
50X1

Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 1 of 6)



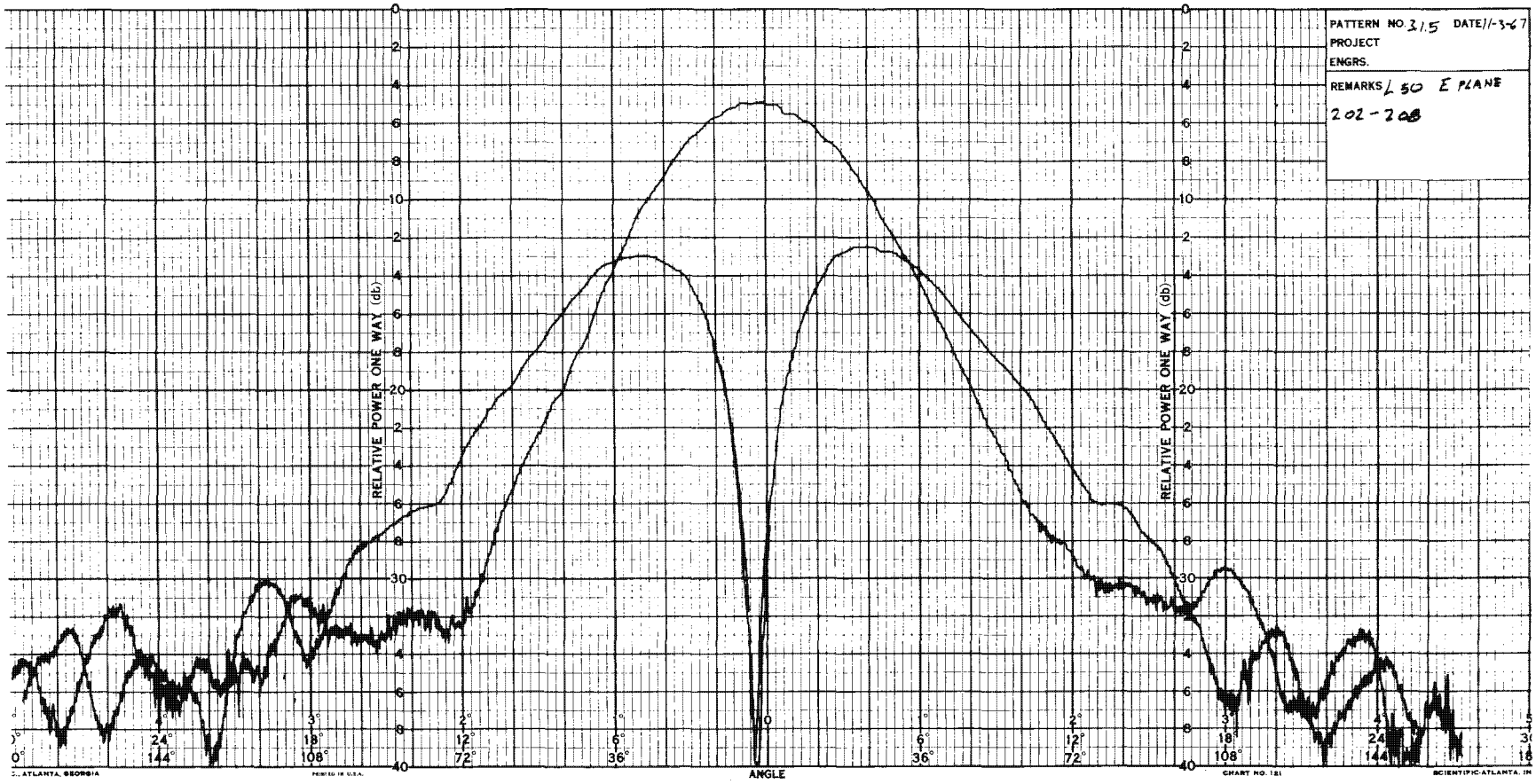
E-Plane, 2440 MHz

Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 2 of 6)



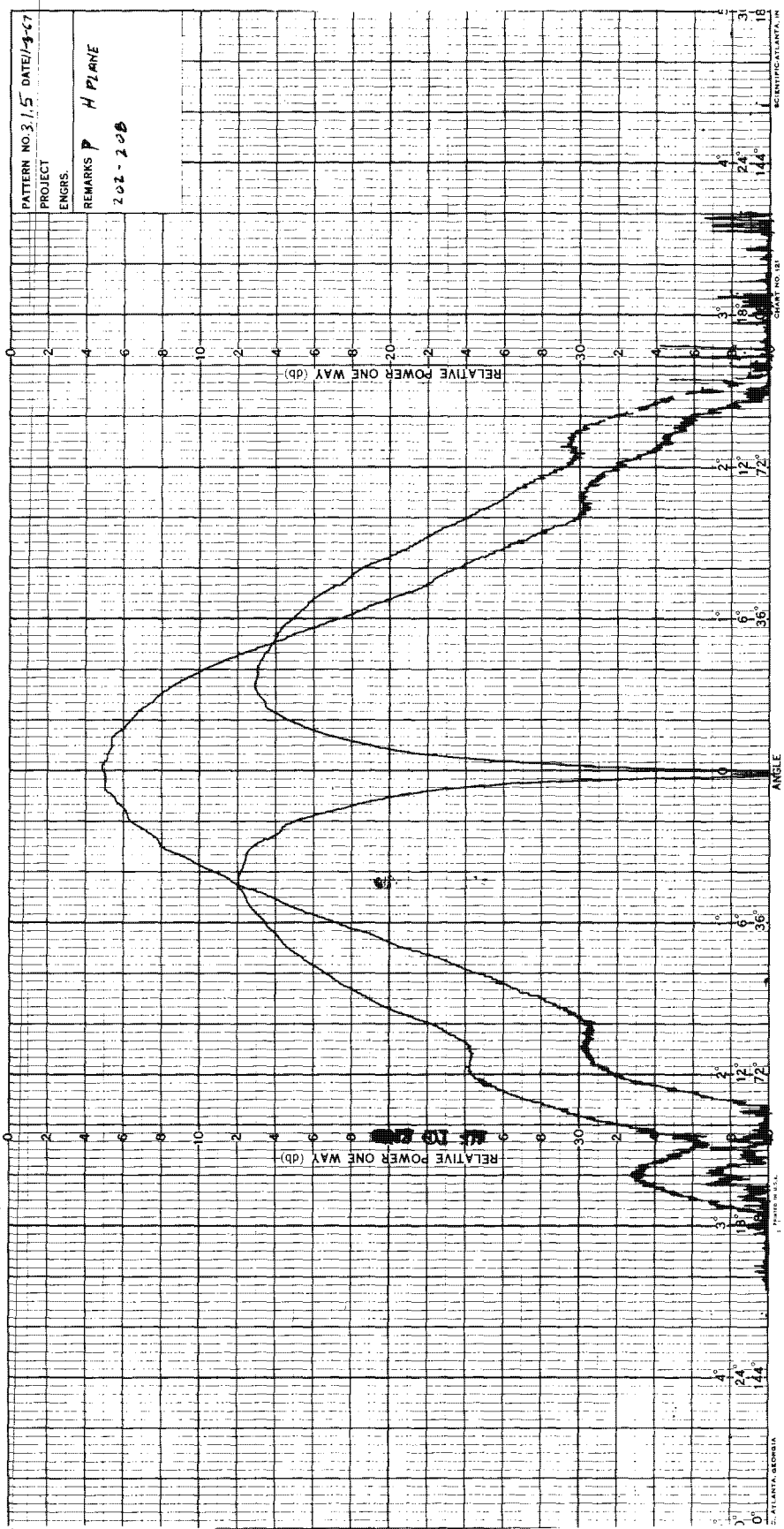
H-Plane, 2950 MHz

Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 3 of 6)



E-Plane, 2950 MHz

Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 4 of 6)



H-Plane, 3300 MHz

Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 5 of 6)

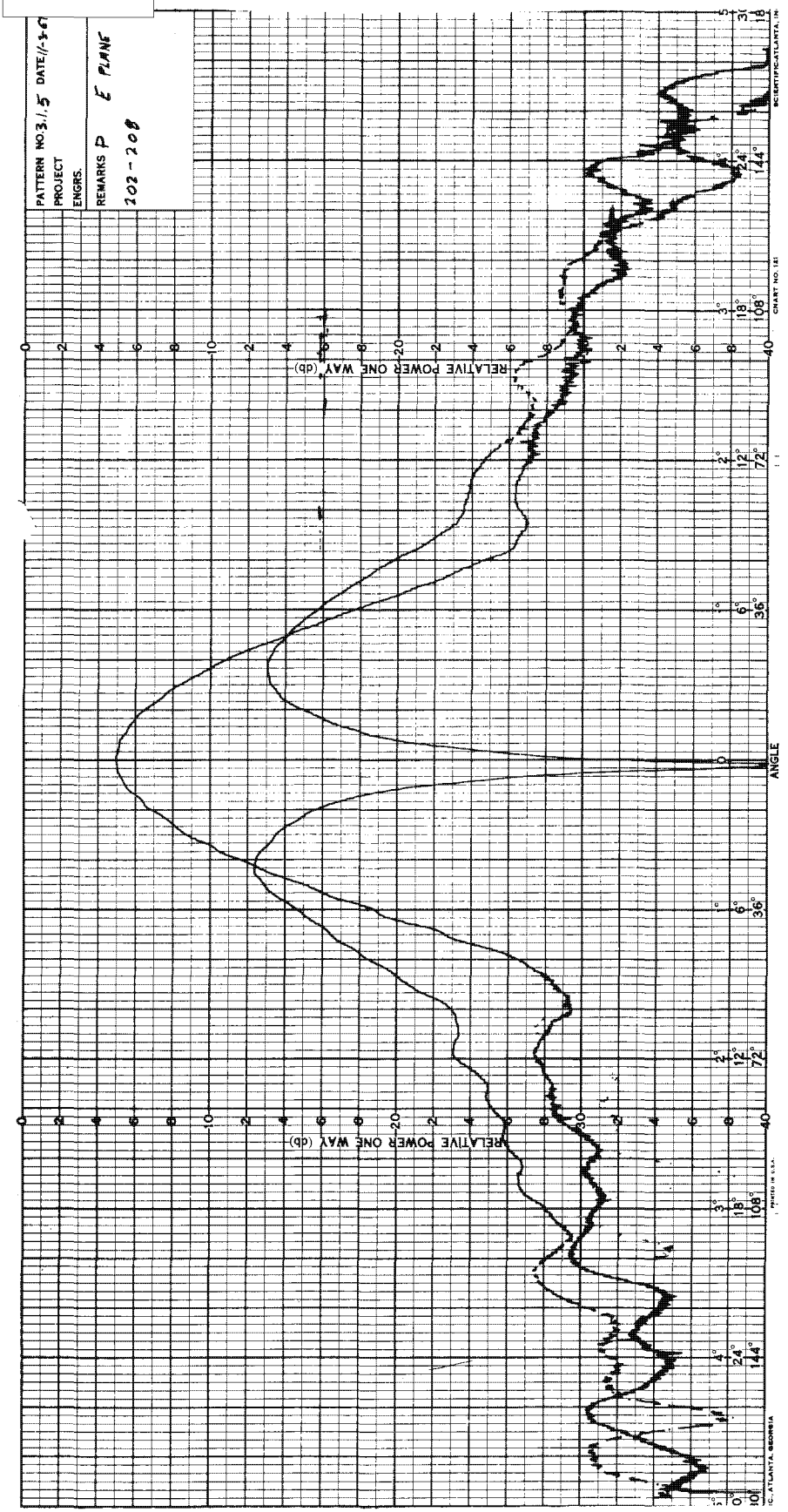


Figure 4.1-3. Spiral Difference Mode Compared to Phase Antennas (Sheet 6 of 6)

4.2 RF Assembly

4.2.1 Introduction

Functional groups of the RF assembly are: RF bandpass filter, RF checkout board (RFCO), and the main stripline (mixers). Interconnection of the groups is illustrated in Figure 4.2-1. The local oscillator (LO) is described in Section 4.3.

The function of the RF assembly is to detect signals from any RF source in the frequency range of 1800 MHz to 3300 MHz and convert to a lower intermediate frequency (IF). The desired information on signal parameters is developed from the IF.

Detection of the RF signal is accomplished without distorting the phase of the arriving signal. Additionally, the introduced noise level must be as low as possible.

The RF assembly operates in two bands. The low band covers the frequency range from 1800 MHz to 2440 MHz and the high band covers the frequency range from 2440 MHz to 3300 MHz.

System operation is checked by feeding a signal into the RFCO board from a test signal generator on board or from an external signal generator. The RFCO divides the test signal equally in phase and amplitude, and distributes test signals to each RF channel. Equal phase distribution places the test signal at boresight for all frequencies.

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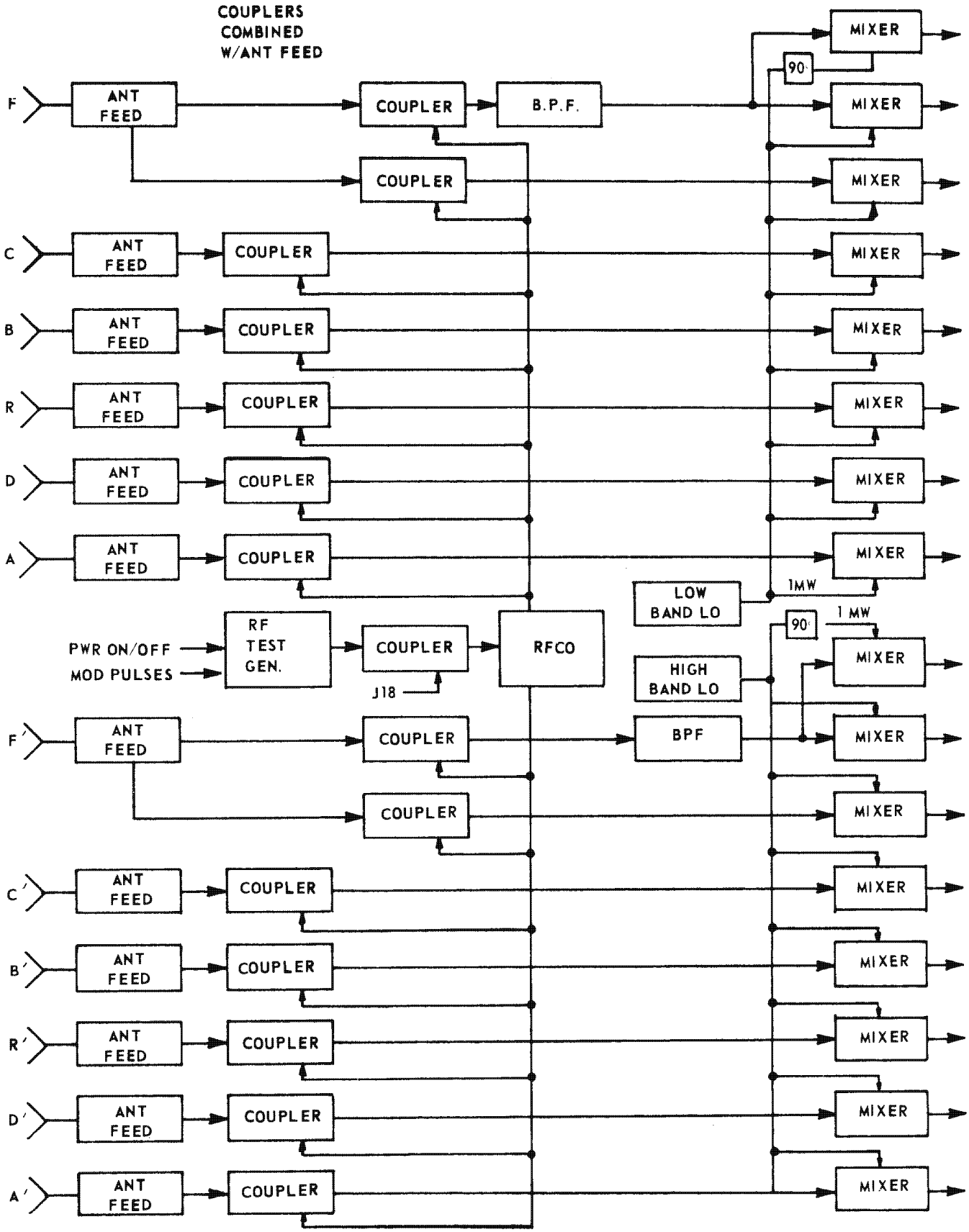

Figure 4.2-1. RF Assembly Block Diagram

4.2.2 RF Bandpass Filters

4.2.2.1 General - Two RF bandpass filters attenuate out-of-band signals by 50 db, minimum. The low-band filter has a bandpass from 1.8 to 2.45 GHz and the high-band filter has a bandpass from 2.4 to 3.3 GHz. The filters are physically located in the real/image channel, between the stripline and the Mode 1 spiral antennas of each band.

4.2.2.2 Design Analysis - The filters are designed to attenuate signals outside the passband from 500 to 10,000 MHz by 50 db, minimum. This attenuation is accomplished by using a bandpass filter and a low-pass filter in tandem. See Figures 4.2-1 and 4.2-2.

The bandpass filter is an 8-element, inter-digital array with a Chebycheff response. The design procedure[1] was based on the use of low-pass prototype filter elements valued to give the desired bandpass characteristics.

The inter-digital array has an inherent second passband centered at three times the center frequency of the pass band. It was therefore necessary to series a low-pass filter to extend the stopband to 10 GHz.

The low-pass filter design consists of open circuit stubs and quarterwave lengths of high impedance lines as shown in Figure 4.2-3. The cutoff was designed to ensure that the stopband would include the second bandpass of the bandpass filters.

1. G.L. Matthaei, "Interdigital Bandpass Filters", IRE Transaction on Microwave Theory and Techniques, Vol. MTT-10, 479-491, November 1962

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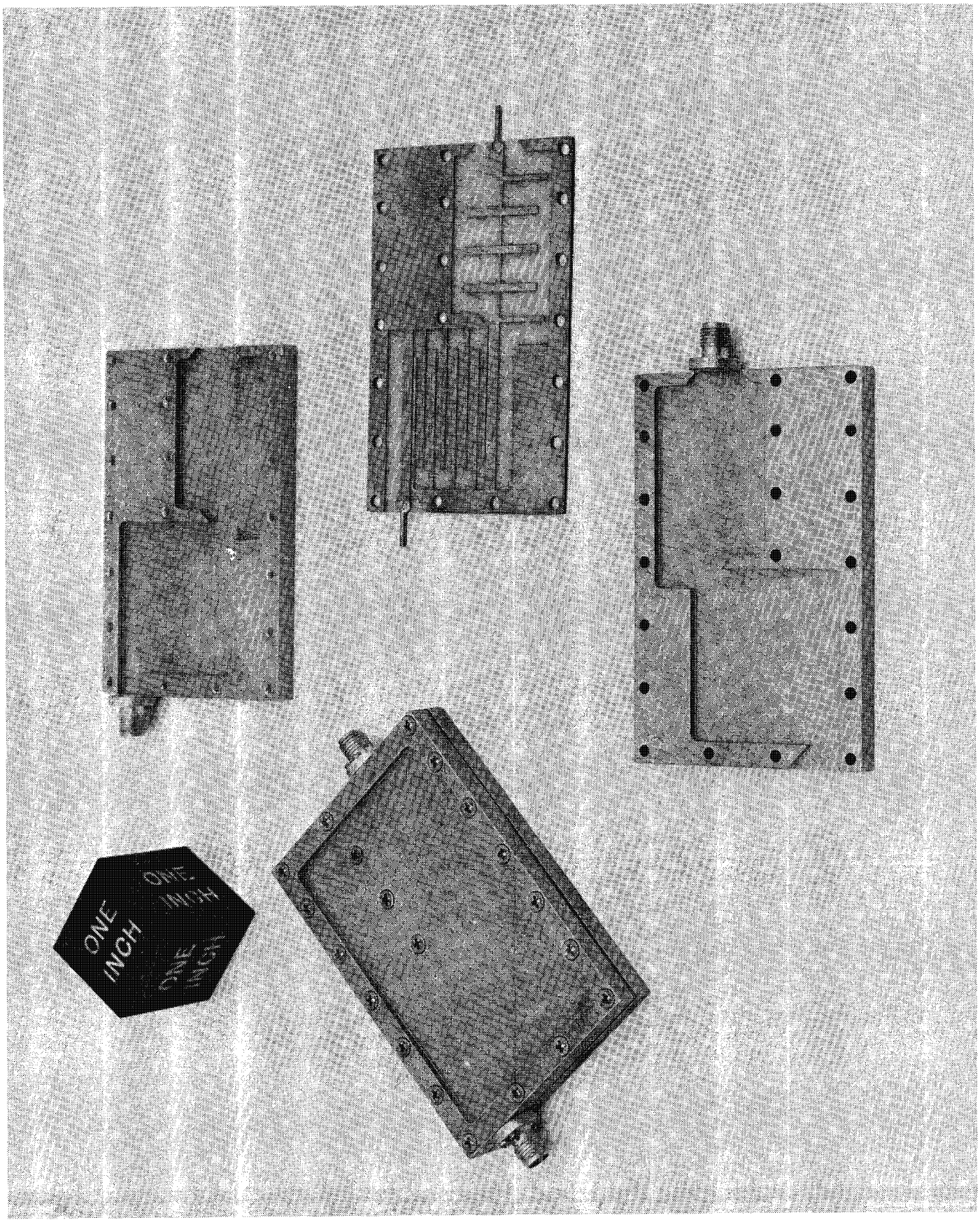

Figure 4.2-2. RF Filter

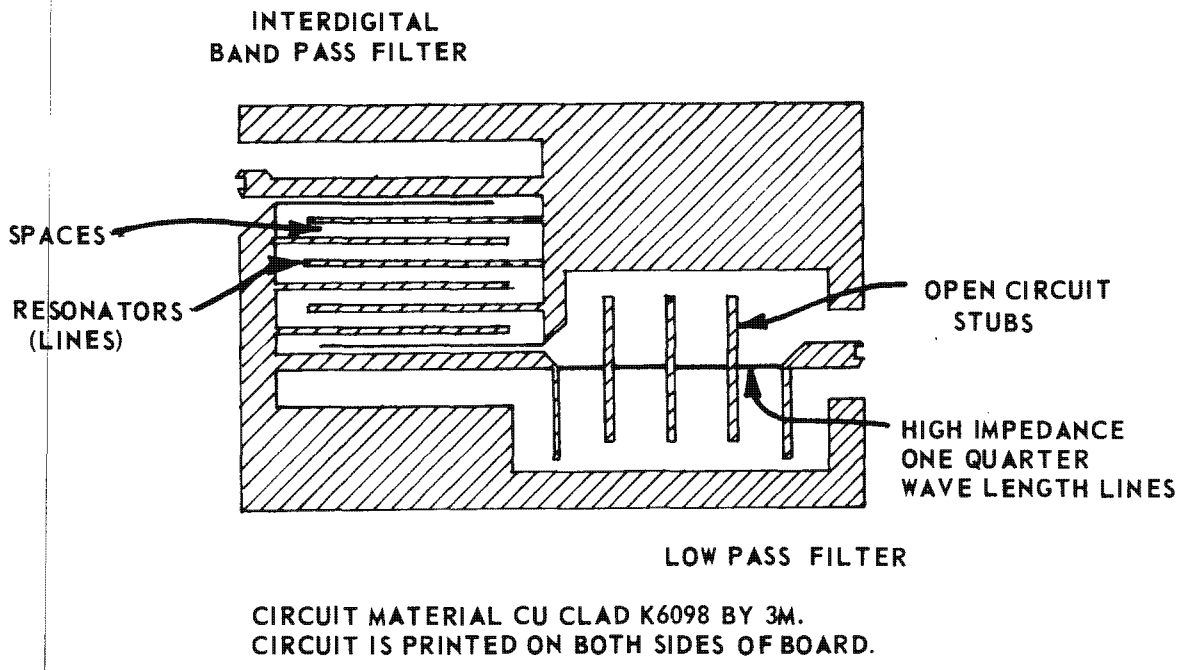

Figure 4.2-3. Stripline Low Band Filter

Construction methods for both high and low band filters are shown in Figure 4.2-4. The use of air dielectric allows areasonable line widths and spaces on the inter-digital array. The lines are assumed to be solid which is a valid assumption since both sides of the lines are at the same potential. Allowance for the dielectric between the ground planes and the resonator ends is made by trimming the resonator ends. Once the correct length has been determined, printed circuit techniques allow exact reproductions of subsequent filters.

To prevent bowing or warping of the printed circuit board, small dielectric supports were placed on the ground plane.

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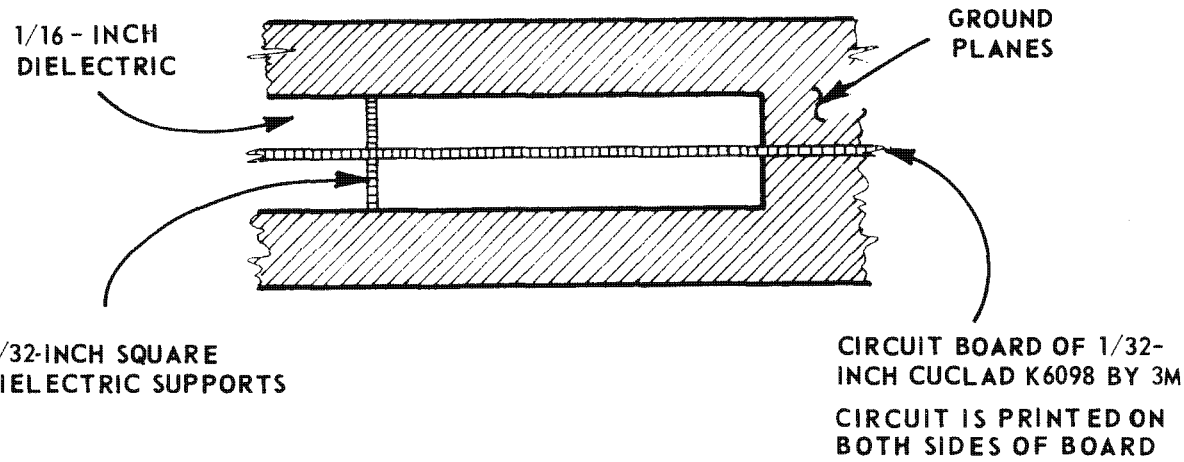

Figure 4.2-4. Filter Construction

4.2.2.3 Electrical Performance - Typical results of band-pass insertion loss, skirt selectivity, and VSWR for high and low band filters are shown in Figures 4.2-5 through 4.2-8. Electrical characteristics of the filters are tabulated in Table 4.2-1.

4.2.3 RF Checkout Board (RFCO)

4.2.3.1 Introduction- The RFCO stripline enables checkout of system operation with a single RF source. The input signal is divided into 16 equal-phase, equal-amplitude outputs.

The unit operates over the system RF spectrum; thus a single board feeds test signals from either an external test generator or the system RF calibrator to both the high and low band sections of the system. Signal output from the RFCO is injected into the system through a 20-db directional coupler

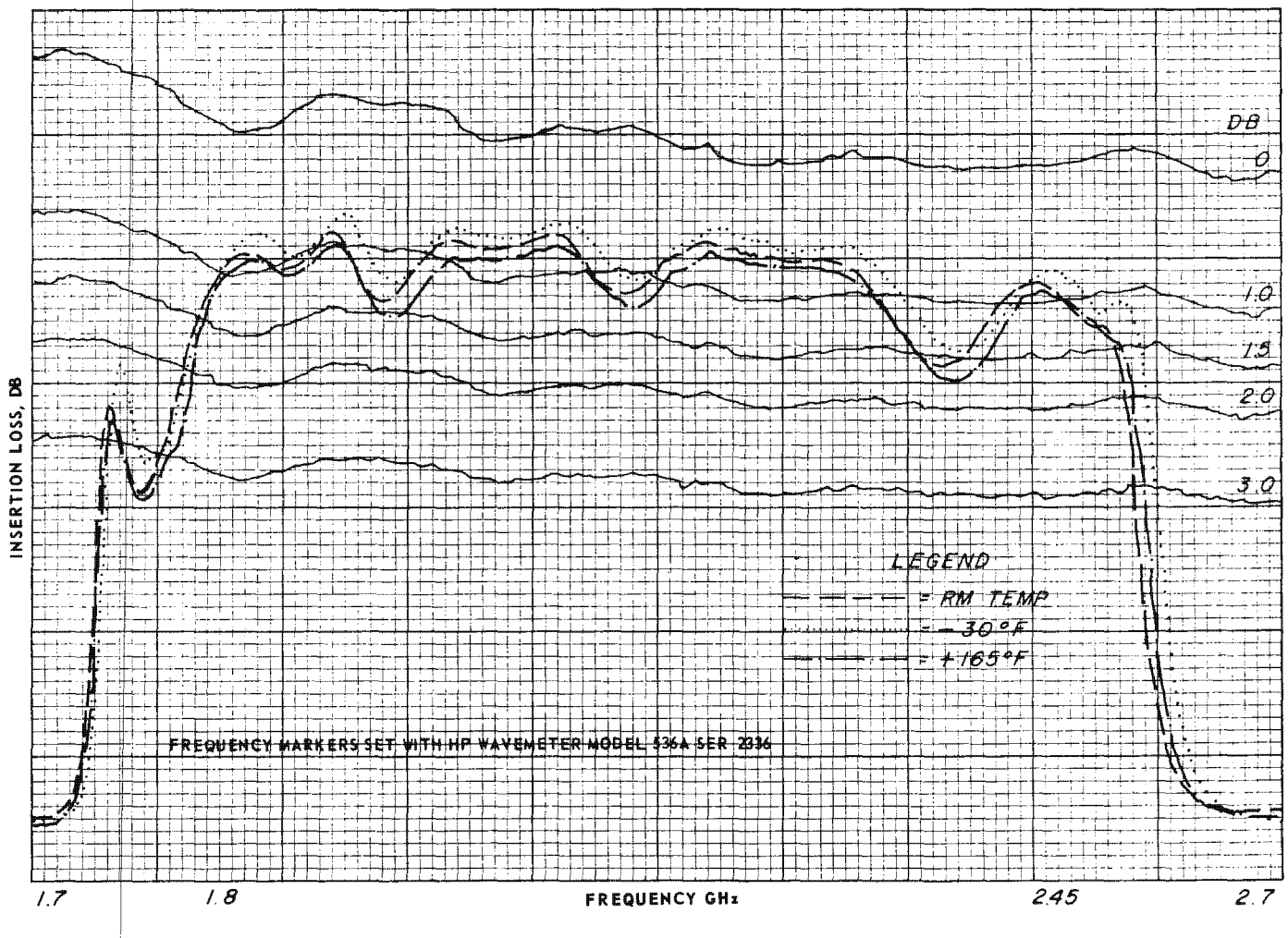

FIGURE 4.2-5. Low Band Filter Functional Test

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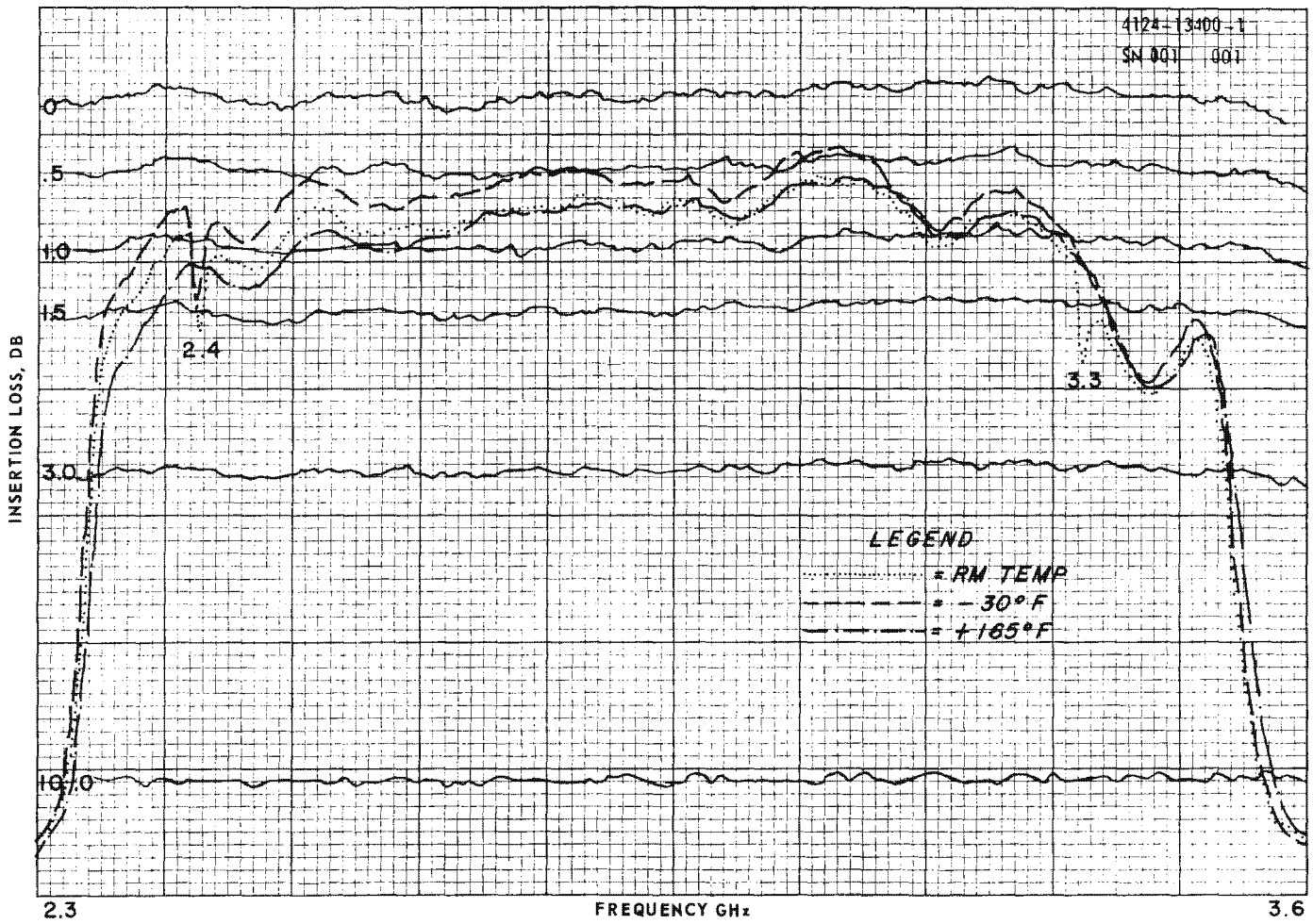

Figure 4.2-6. High Band Filter Functional Test

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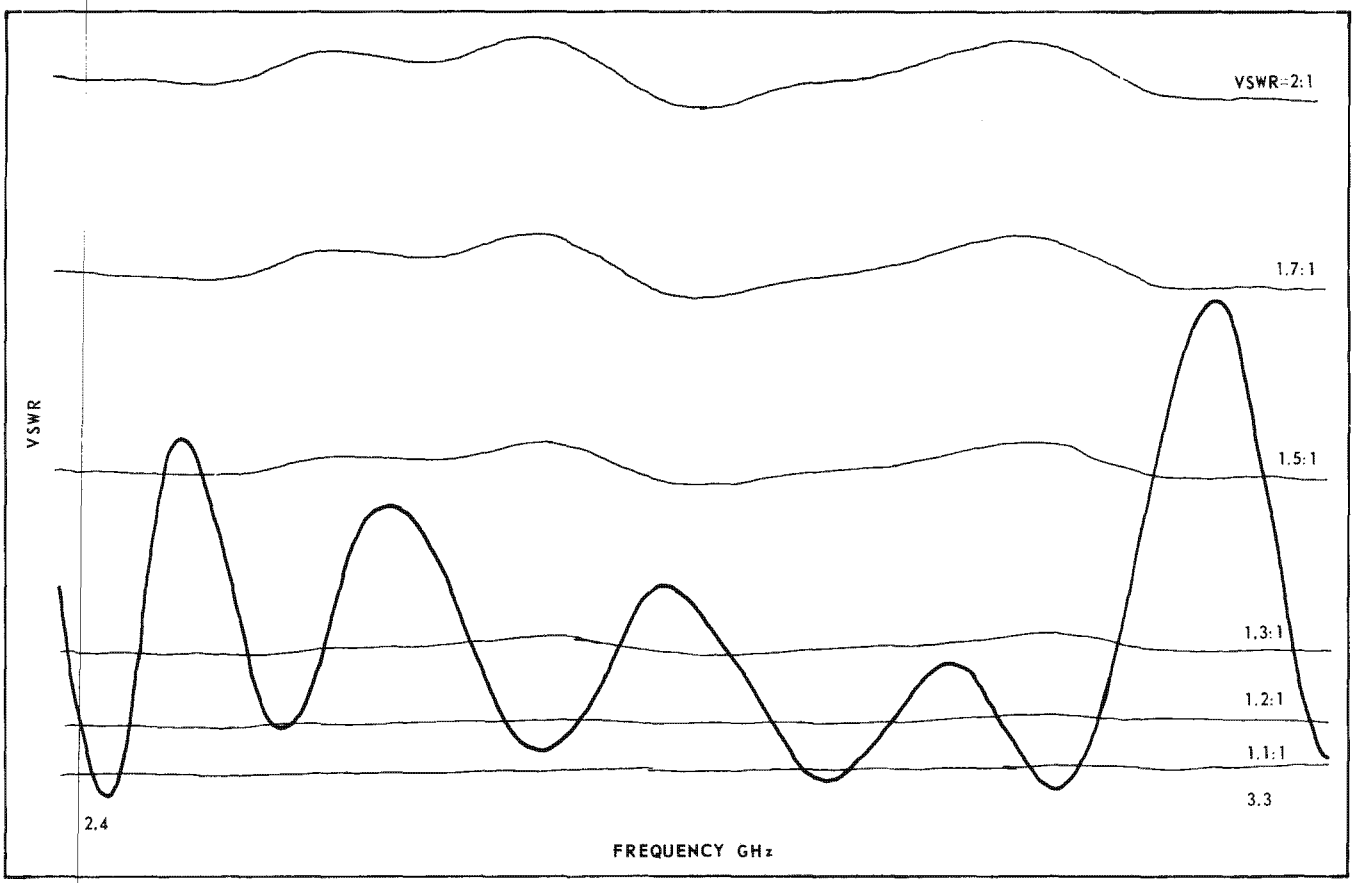

Figure 4.2-7. High Band Filter VSWR

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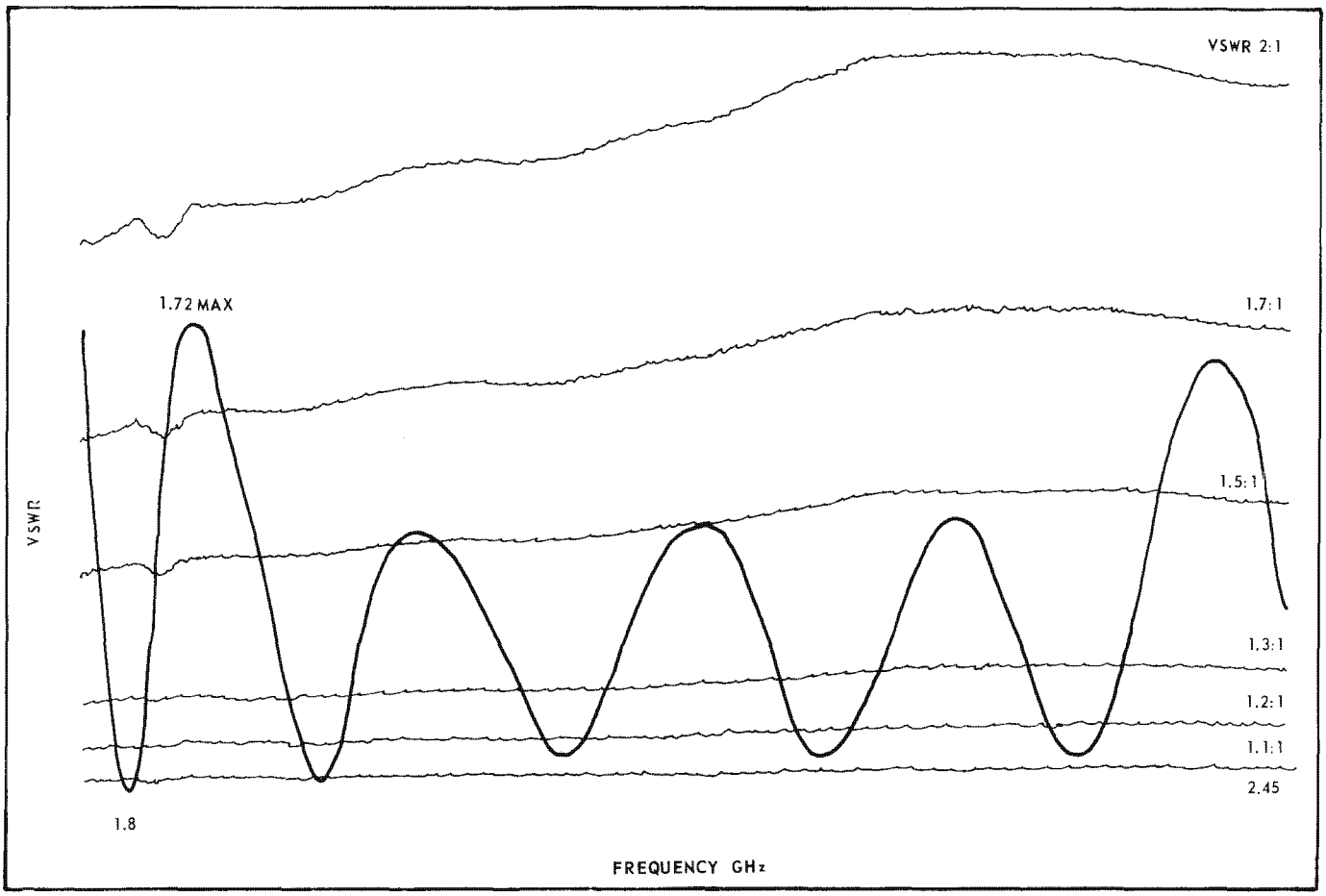

Figure 4.2-8. Low Band Filter VSWR

TABLE 4.2-1 RF BANDPASS FILTER ELECTRICAL CHARACTERISTICS

	TEST DATA		SPECIFICATIONS	
FUNCTION	Lo Band	High Band	Lo Band	High Band
Passband	1800-2450 MHz	2400-3300 MHz	1800-2450 MHz	2400-3300 MHz
Insertion Loss	1.3 db, Normal 1.7 db, Maximum	1.0 db Normal 1.3 db Maximum	1.5 db	1.5 db
Insertion Loss in Stop Band	50 db	50 db	50 db	50 db
VSWR	1.5 1.72, Maximum	1.5 1.60, Maximum	1.7	1.7

50X1

50X1

in each antenna stripline network. Figure 4.2-9 illustrates the RFCO stripline with 50-ohm terminations installed on the two unused ports.

4.2.3.2 Design Analysis - The RFCO stripline consists of 15 resistively loaded, 3-db power dividers connected to provide the 16 RF outputs. Phase properties of the signals are attained by maintaining the equality of the signal path length between each power divider. The power divider itself has no phase difference between its two output arms. Figure 4.2-10 shows a swept presentation of phase versus frequency of four typical channels of the RFCO board. Phase variation for one channel is $\pm 3.0°$, and phase tracking error between the four channels is $\pm 1.3°$.

The amplitude of any output port is approximately 13 db below the input RF signal. Loss of 12 db is attributed to the power division in the circuit path, and 1-db loss accruing due to the dissipation over the RF signal path. Insertion loss (referred to the input signal) versus frequency for a typical RFCO output is shown in Figure 4.2-11. Amplitude tracking between any two channels is ± 0.25 db.

The VSWR of any output port with all other ports terminated in their characteristic impedance, does not exceed a ratio of 1.8 to 1. Figure 4.2-12 shows a swept presentation of the VSWR versus frequency for a typical RFCO output port, with a maximum indicated VSWR of 1.5 to 1.

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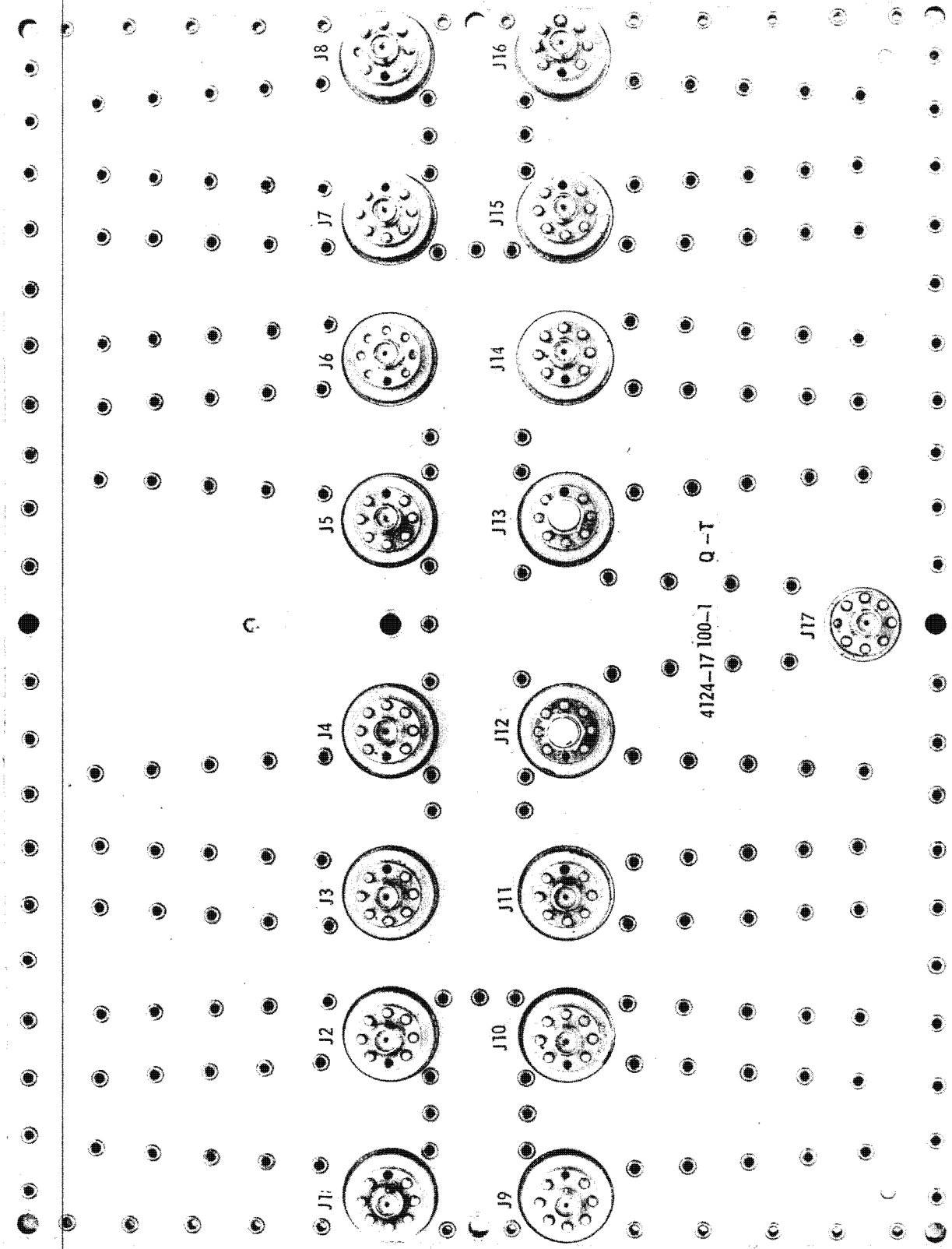

Figure 4.2-9. RF Checkout Board

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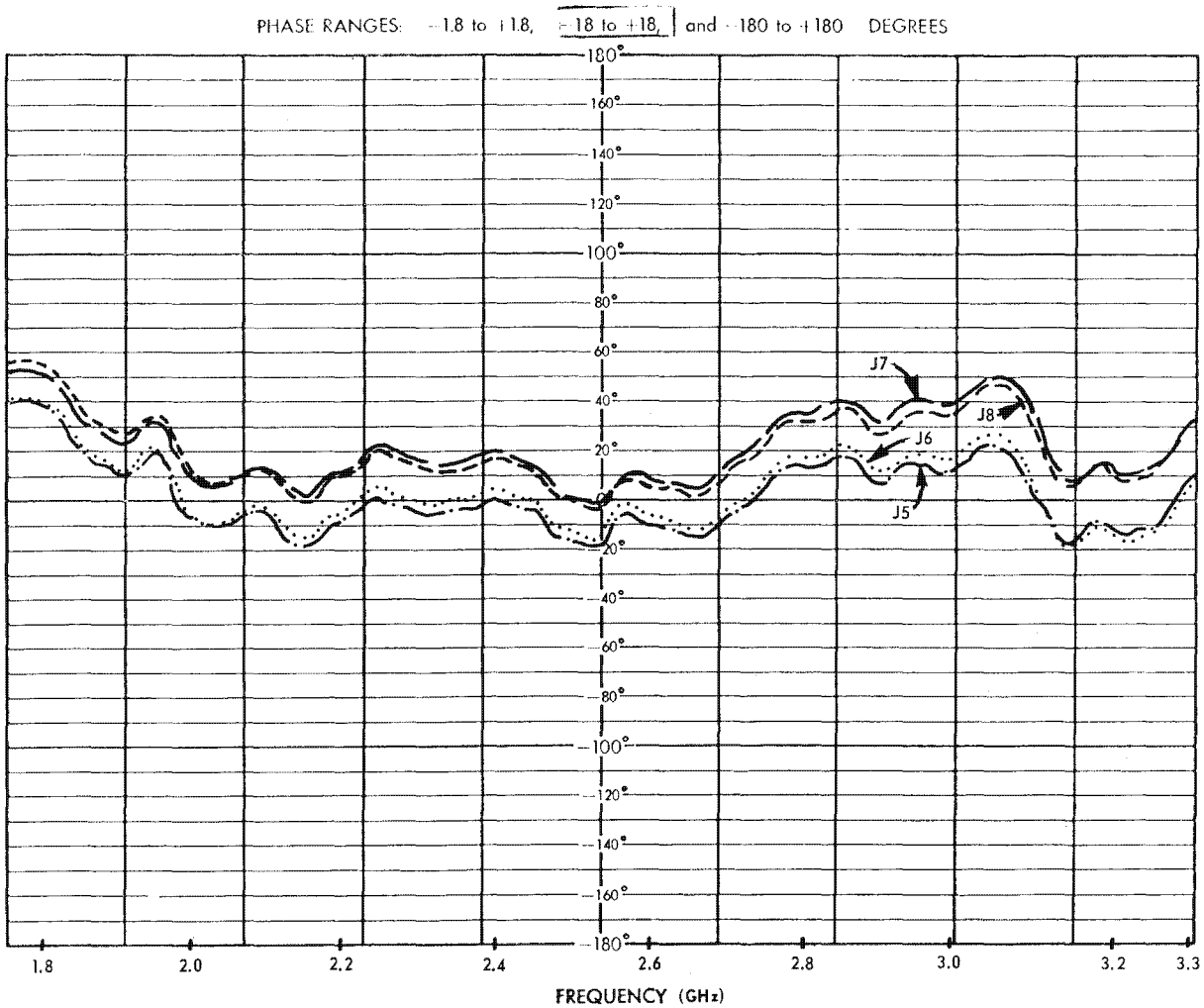

Figure 4.2-10. RFCO Phase vs Frequency

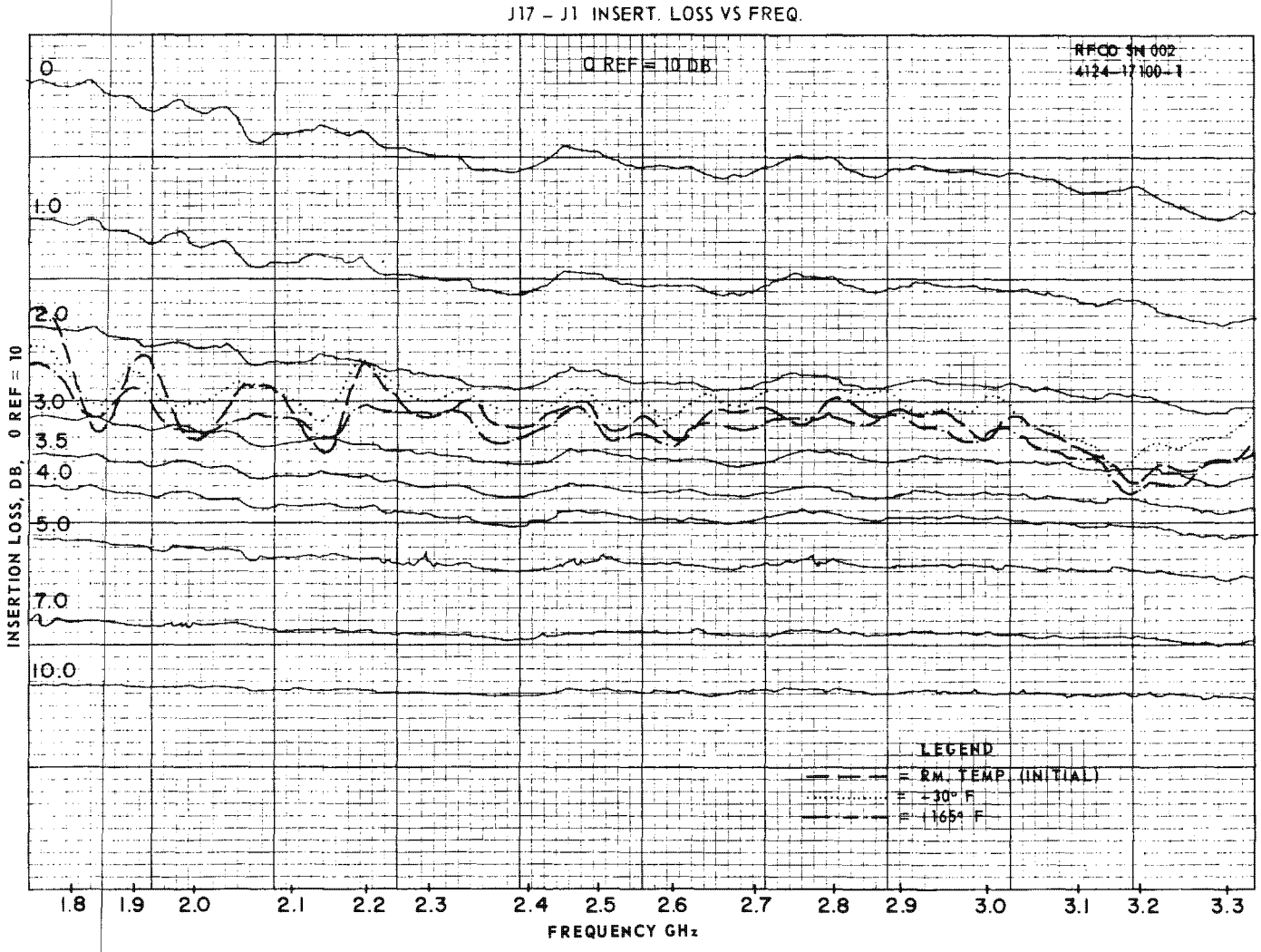

Figure 4.2-11. J17 - J1 Insertion Loss vs Frequency

Figure 4.2-12. Output VSWR vs Frequency

Isolation between any two channels of the RFCO board is 13 db, minimum, and is based on the inherent isolation between the two output arms of a single 3-db power divider.

4.2.3.3 Summary of Electrical Design Specification - Table 4.2-2 presents the summarized electrical performance specifications for the RFCO. Production assemblies meet the requirements established by the design specification.

4.2.4 Main Stripline (Mixers)

4.2.4.1 Introduction - The main stripline accepts the seven RF signal inputs from the system antennas plus the input from the local oscillator, for mixing in the main stripline to provide eight intermediate frequency (IF) outputs.

Five of the IF outputs are amplitude and phase matched to provide signals for direction finding. Two outputs are amplitude matched with a 90° phase offset to provide a means for real-image detection. The eighth output is amplitude matched with the phase outputs and is used for amplitude-ratio inhibit detection. A detection circuit is also provided to monitor the level of the LO signal. Figure 4.2-13 shows the assembled main stripline.

4.2.4.2 Design Analysis - The main stripline consists of eight balanced mixers and an LO distribution system. The assembly is designed to operate over the entire frequency spectrum of the system; however, due to the frequency

TABLE 4.2-2 ELECTRICAL PERFORMANCE SPECIFICATIONS

RFCO 4124-17100

	TYPICAL DATA	SPECIFICATION
Signal Frequency	1800-3300 MHz	1800-3300 MHz
Impedance	50 ohms	50 ohms
VSWR:		
Output Ports	1.5 to 1 Maximum	1.8 to 1 Maximum
Input Port	2.3 to 1 Maximum	2.8 to 1 Maximum
Insertion Loss	13.3 db Maximum	13.6 db Maximum
Amplitude Tracking	$\pm$0.25 db	$\pm$0.5 db
Phase Variation	$\pm$3.0°	$\pm$5.0°
Phase Tracking	$\pm$1.4°	$\pm$3.0°
Isolation	13.5 db Minimum	13.0 db Minimum

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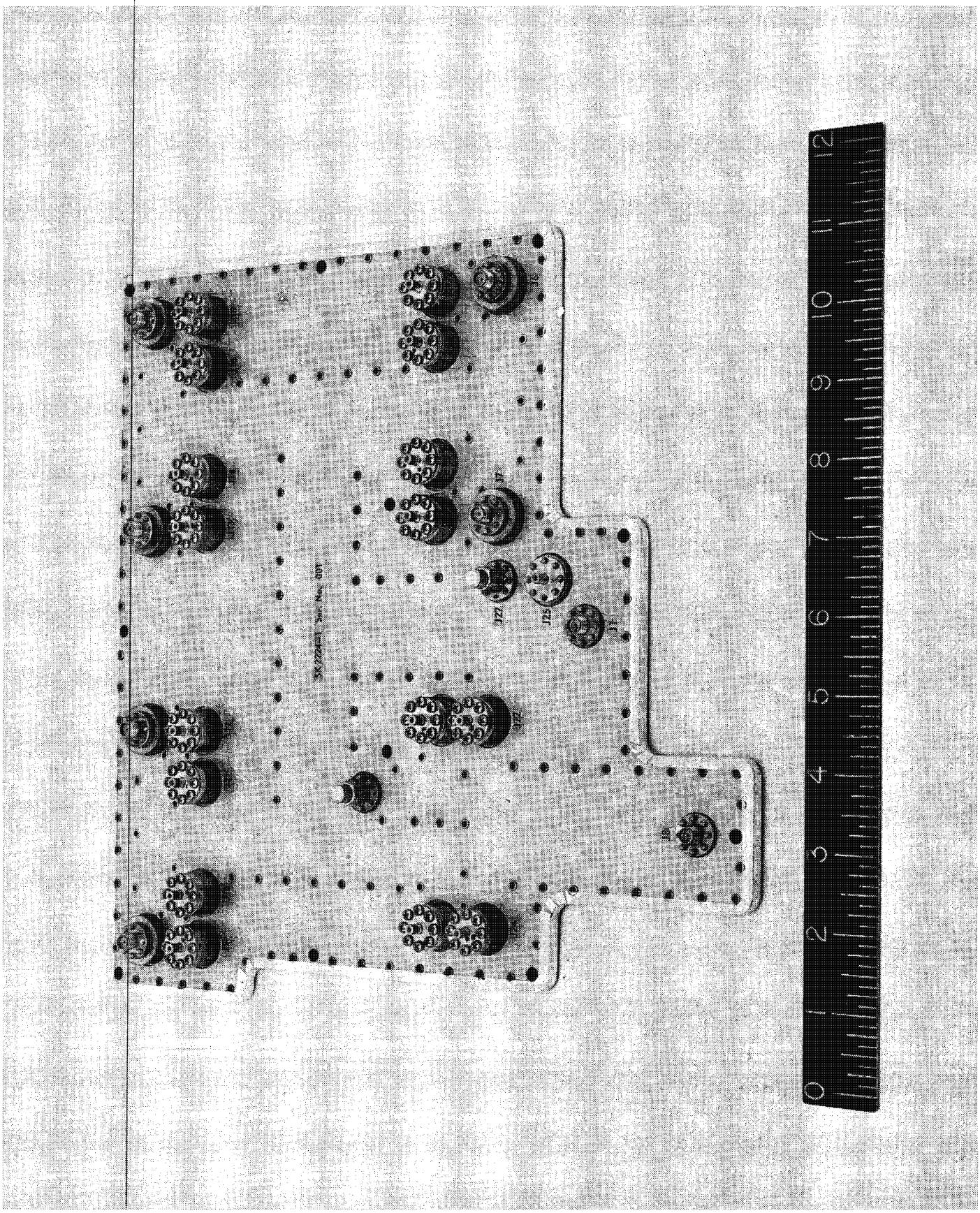

Figure 4.2-13. Main Stripline

limitations of the LO and the antennas, two boards are used. One board is used with the high-band antennas and LO, and the other board with the low-band antennas and LO.

The mixers are all of the same balanced design, using a 3-db broadside coupled, 90° hybrid to accept the RF and LO inputs. Matched, Schottky-barrier diodes are used as mixer elements.

The IF signal from the diodes is recombined at the input to the IF preamplifier with resultant cancellation of the LO noise. Figure 4.2-14 is a schematic diagram of the balanced mixer. The coupled hybrid provides a good match to the input signal. Normal VSWR is 1.3 to 1. Makimum VSWR was set at 1.8 to 1. Figure 4.2-15 shows the VSWR of four typical RF input ports across the frequency band.

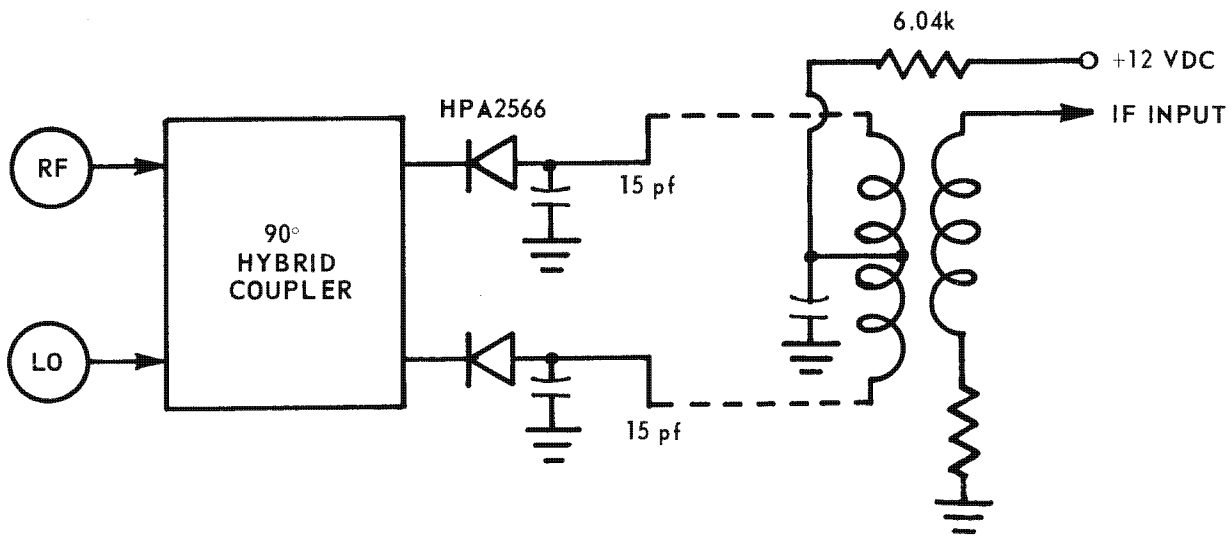

Figure 4.2-14. Balanced Mixer

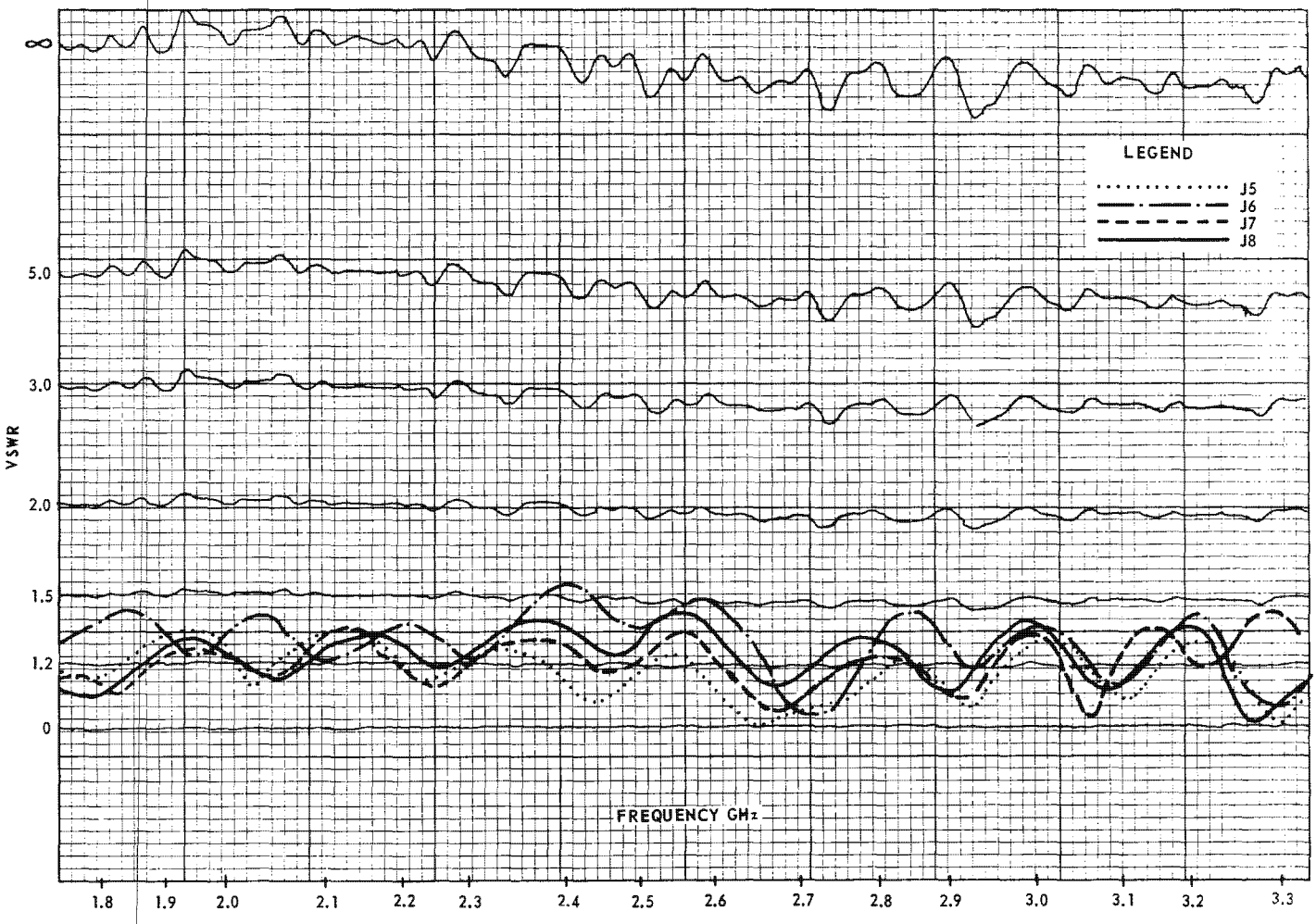

Figure 4.2-15. VSWR vs Frequency

Due to the broadband characteristic of the hybrid the mixer output amplitude is level within ±2.0 db (See Figure 4.2-16) and variation of the IF phase angle does not exceed ±5.0°. Figure 4.2-17 shows the phase performance of both the real and image IF signal of a typical mixer across the full RF frequency band.

50X1

Schottky diodes were selected for their low-noise characteristics. The diodes are operated with a fixed-current bias due to the minimum LO power limit (-6 dbm per diode element). The mixers have a maximum single side band noise figure of 8 db when operated with a 1.5 db NF IF amplifier,

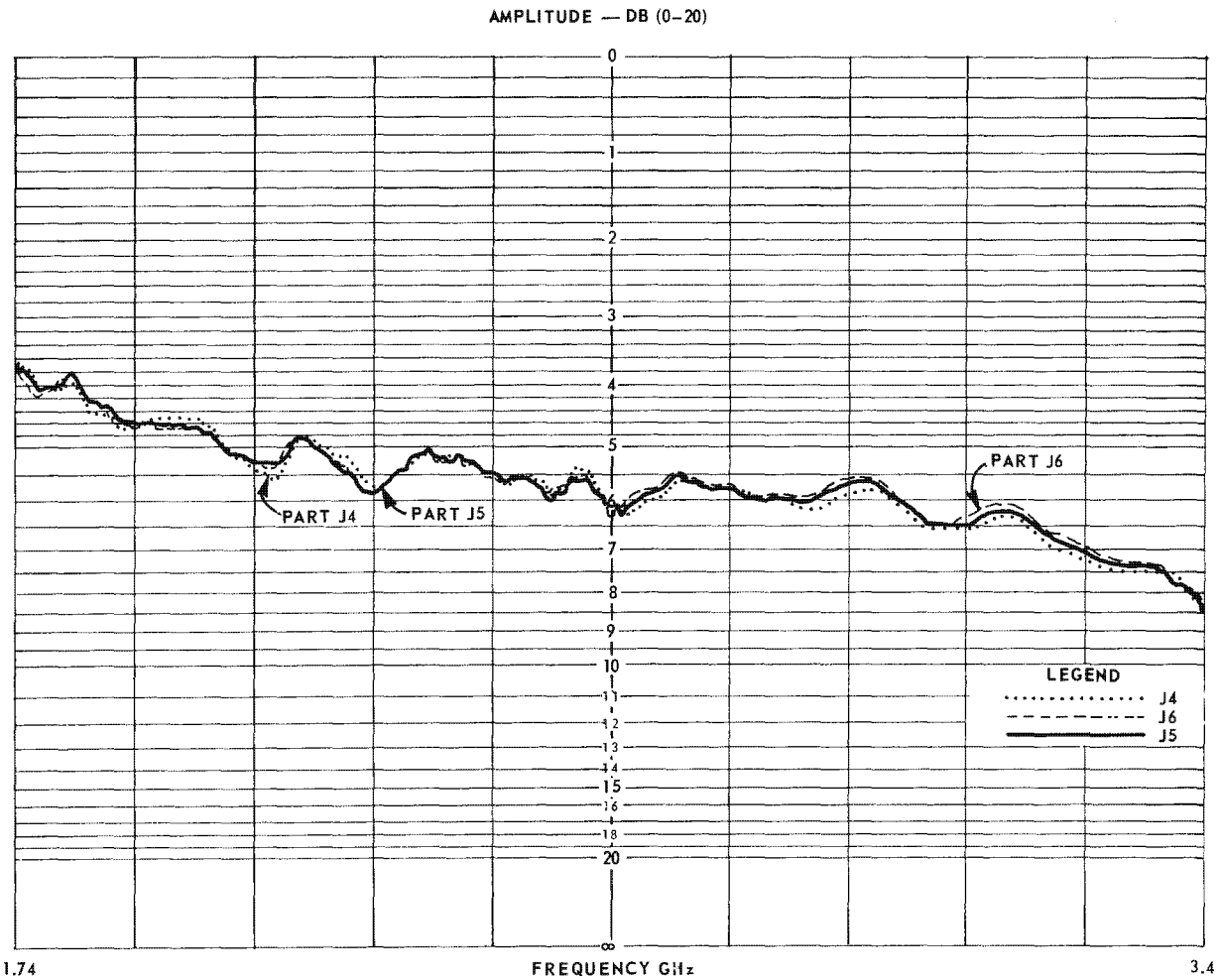

Figure 4.2-16. Amplitude Variation With LO Frequency

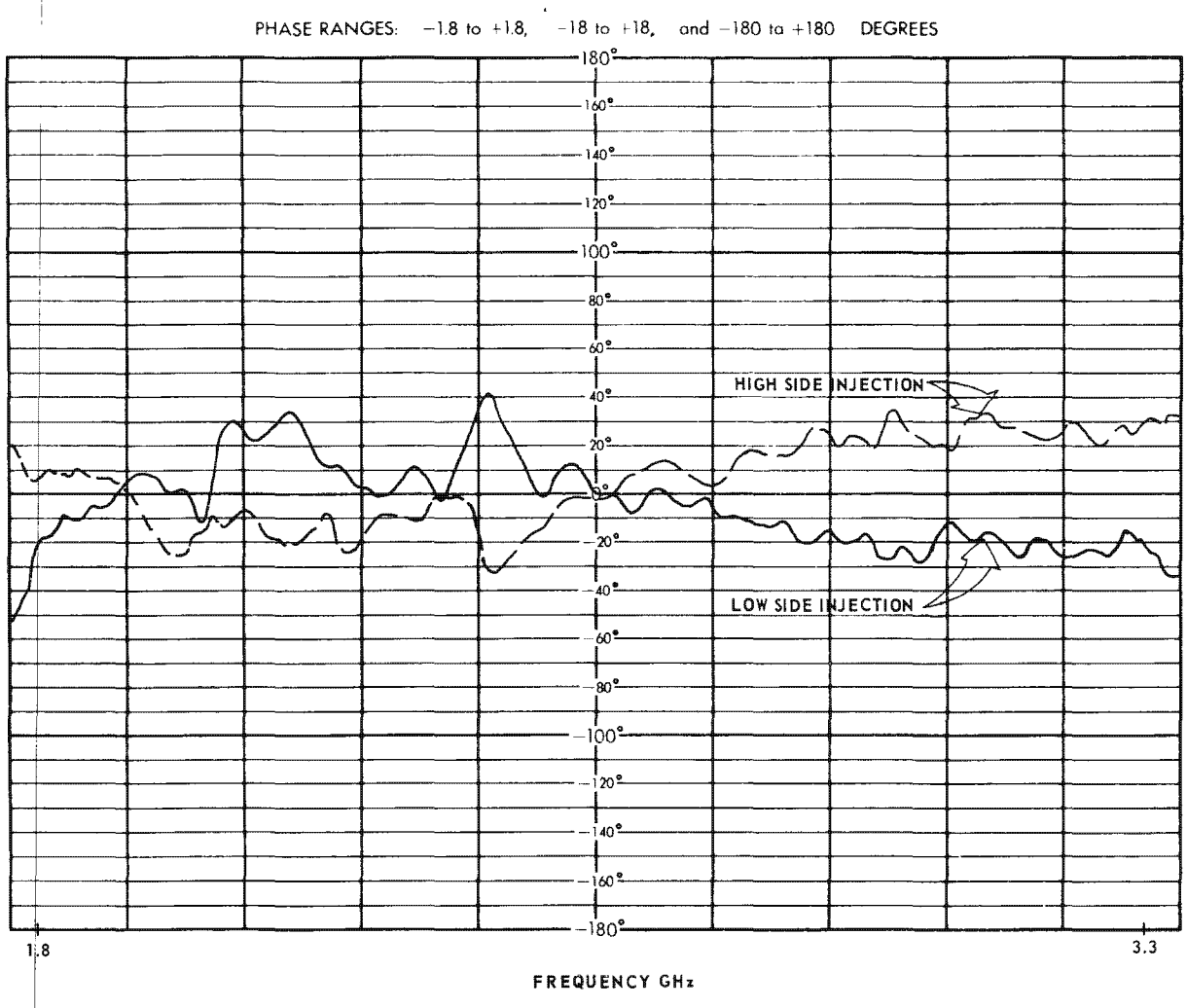

Figure 4.2-17. Boresight Phase

with a +7 dbm LO input to the stripline. A plot of a typical mixer NF across the operating frequency appears in Figure 4.2-18.

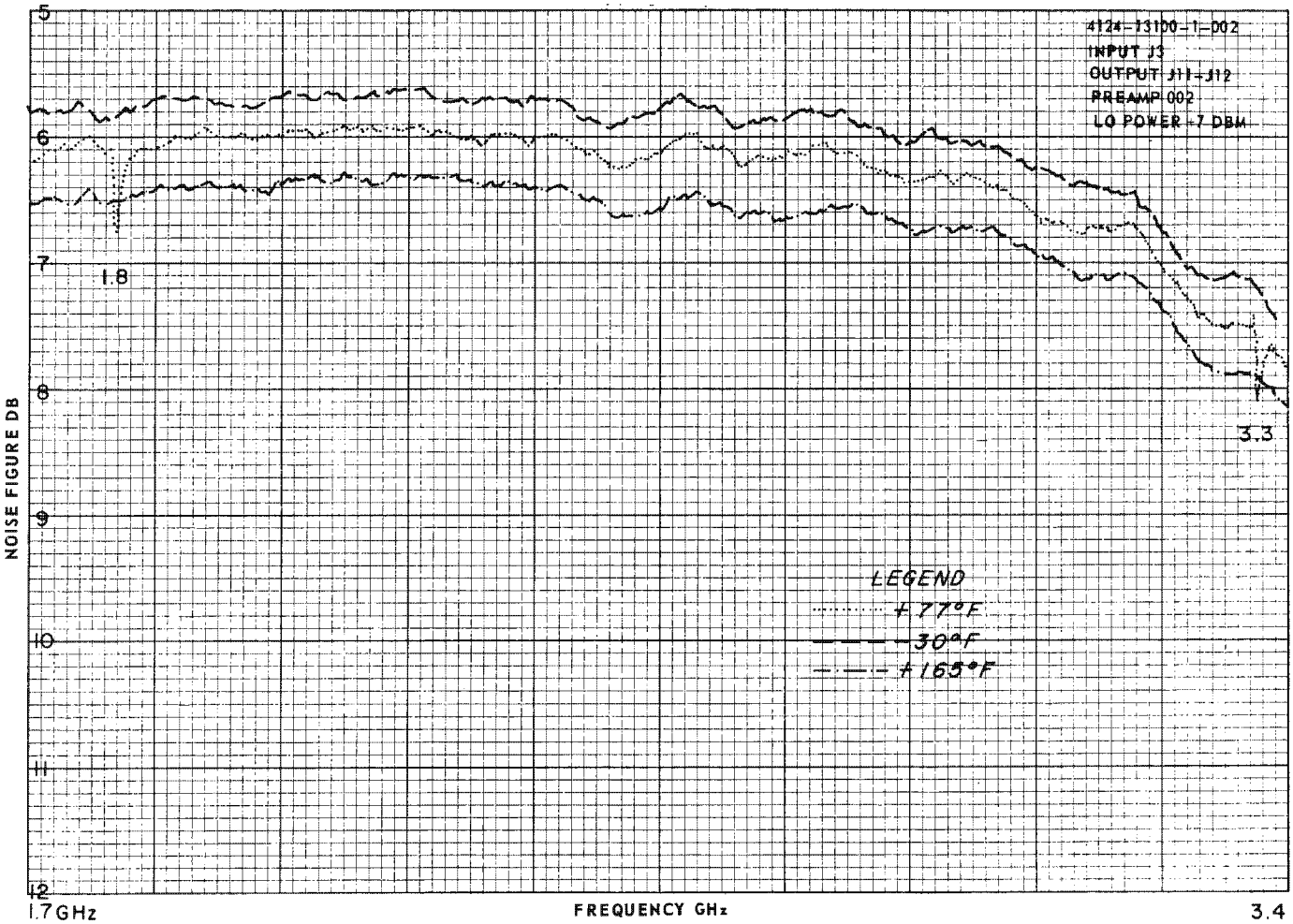

Figure 4.2-18. Noise Figure vs Frequency

In-band spurious signals are at least 55 db below the level of a T-min signal. With the addition of the system band pass filter, spurious signals outside the operating frequency band, up to 10 GHz are suppressed at least 70 db below the T-min level. Figures 4.2-19 and 4.2-20 show the spurious levels for a typical mixer with the RF bandpass filter installed.

The LO distribution network of the main stripline consists of six resistively-loaded, 3-db power dividers which have equal phase outputs and a 3 db coupled hybrid divider which has a 90° phase offset between its outputs. Interconnection of the power dividers and the mixers is illustrated in Figure 4.2-21.

By precise control of the interconnecting path length, the output of the six mixers from the equal-phase dividers have the same phase angle. Figure 4.2-22 shows the phase tracking performance three typical mixer outputs which supply the system phase information showing these tracking within $\pm 3.25°$.

Amplitude tracking between the channels is inherent in the stripline design. Figure 4.2-16 also shows amplitude tracking of the IF outputs of three channels of a typical stripline assembly. Tracking error is ± 0.4 db.

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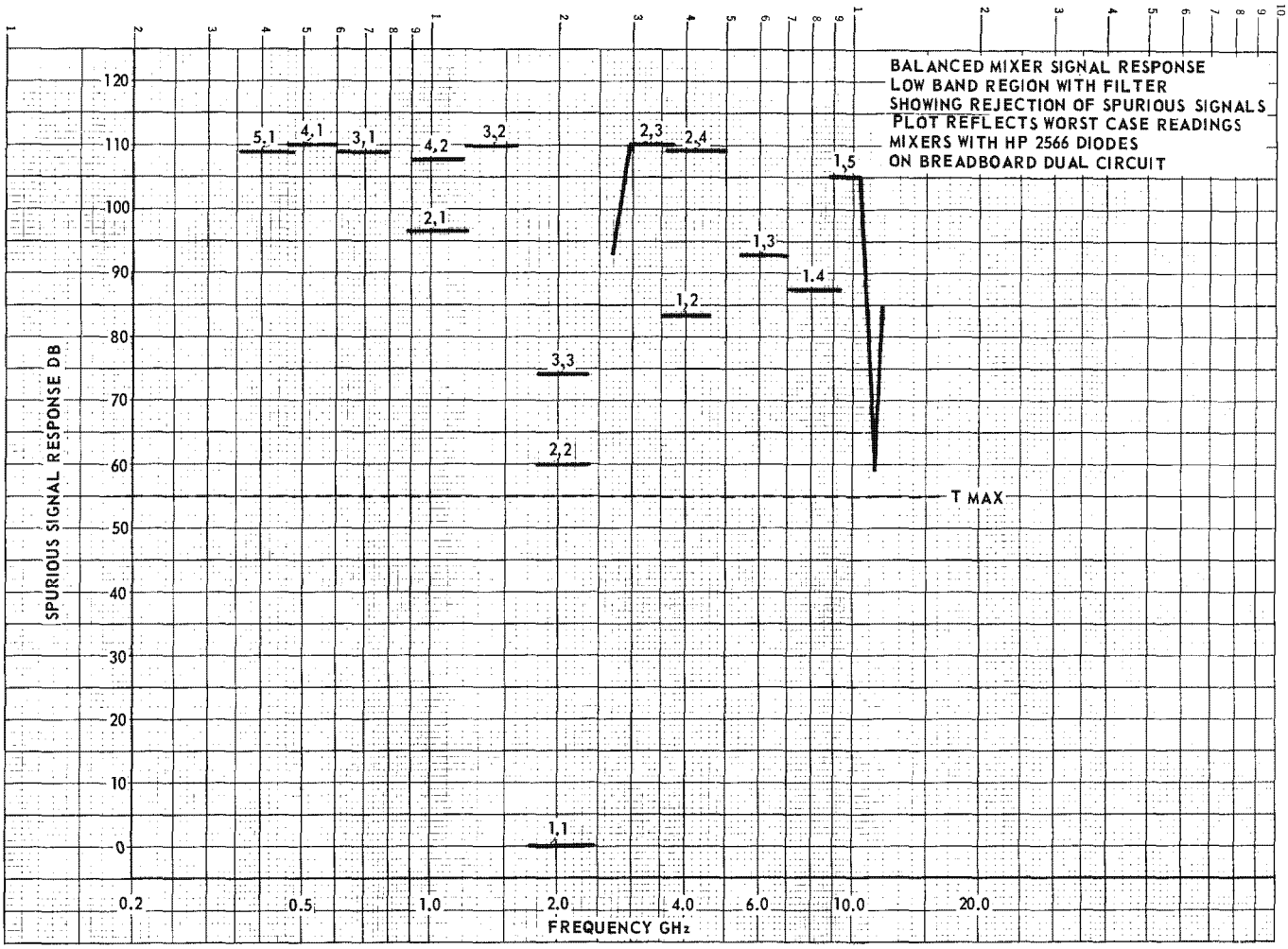

Figure 4.2-19. Low Band Mixer Signal Response

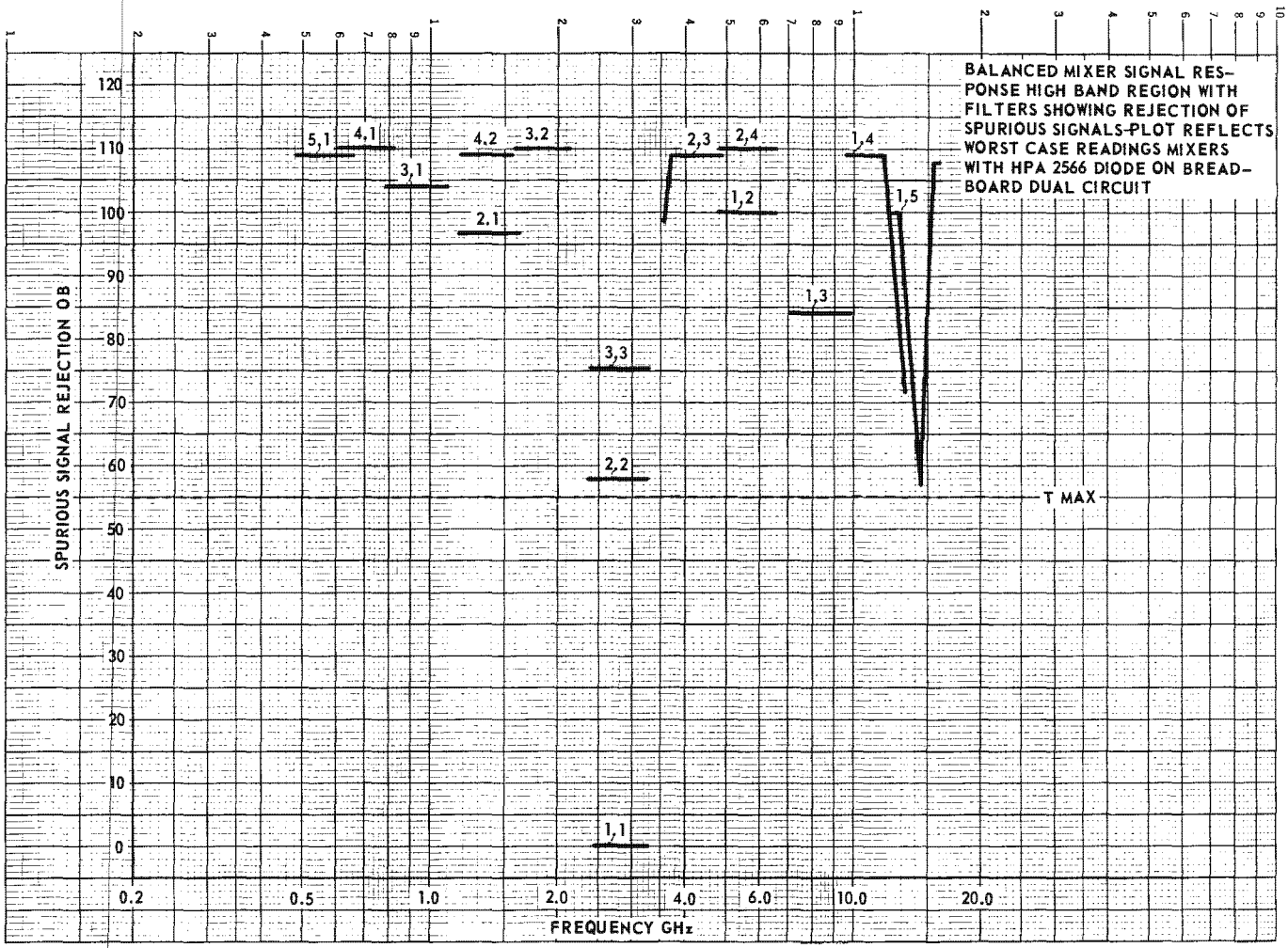

Figure 4.2-20. High Band Mixer Signal Response

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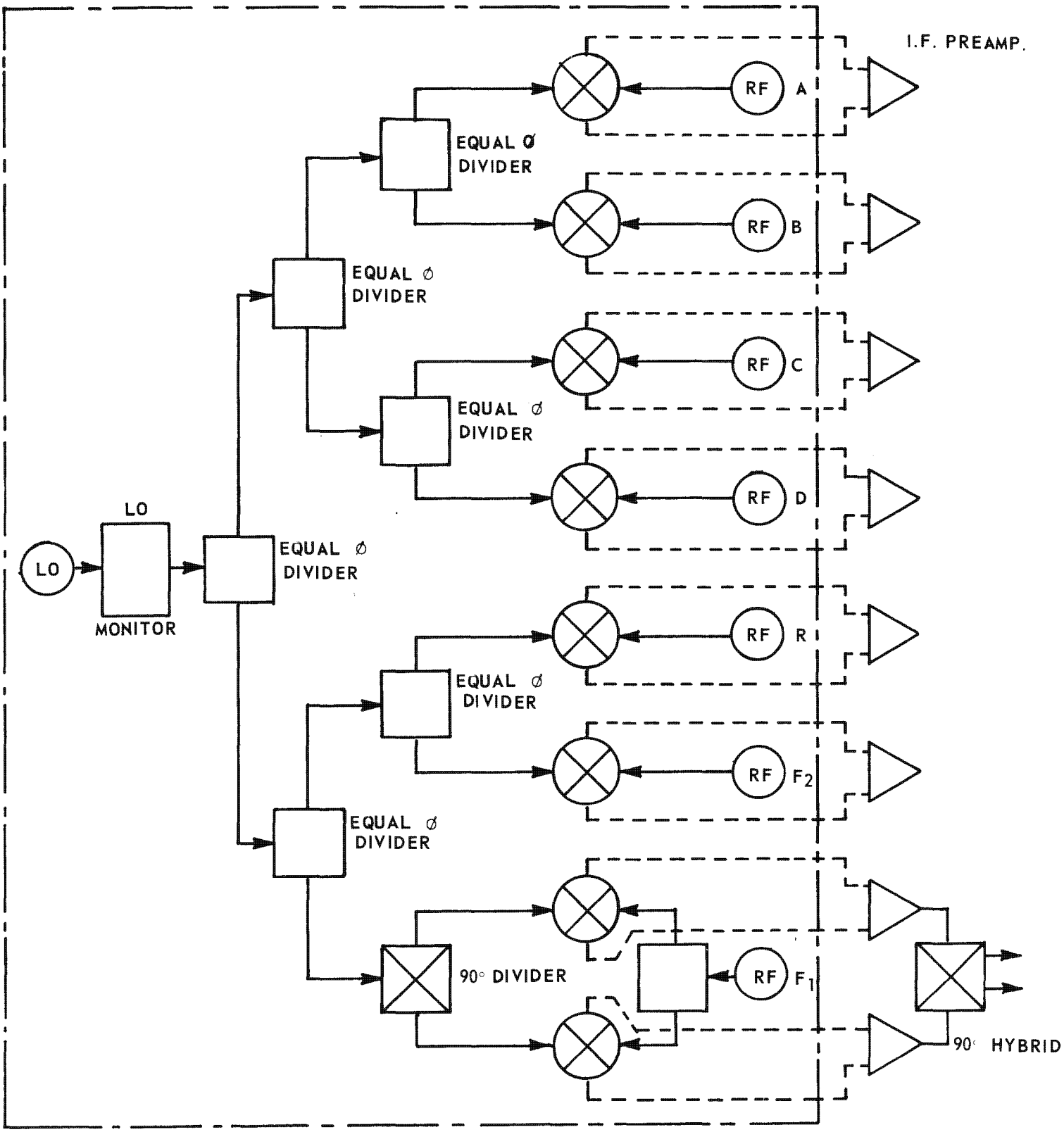

Figure 4.2-21. Main Stripline Block Diagram

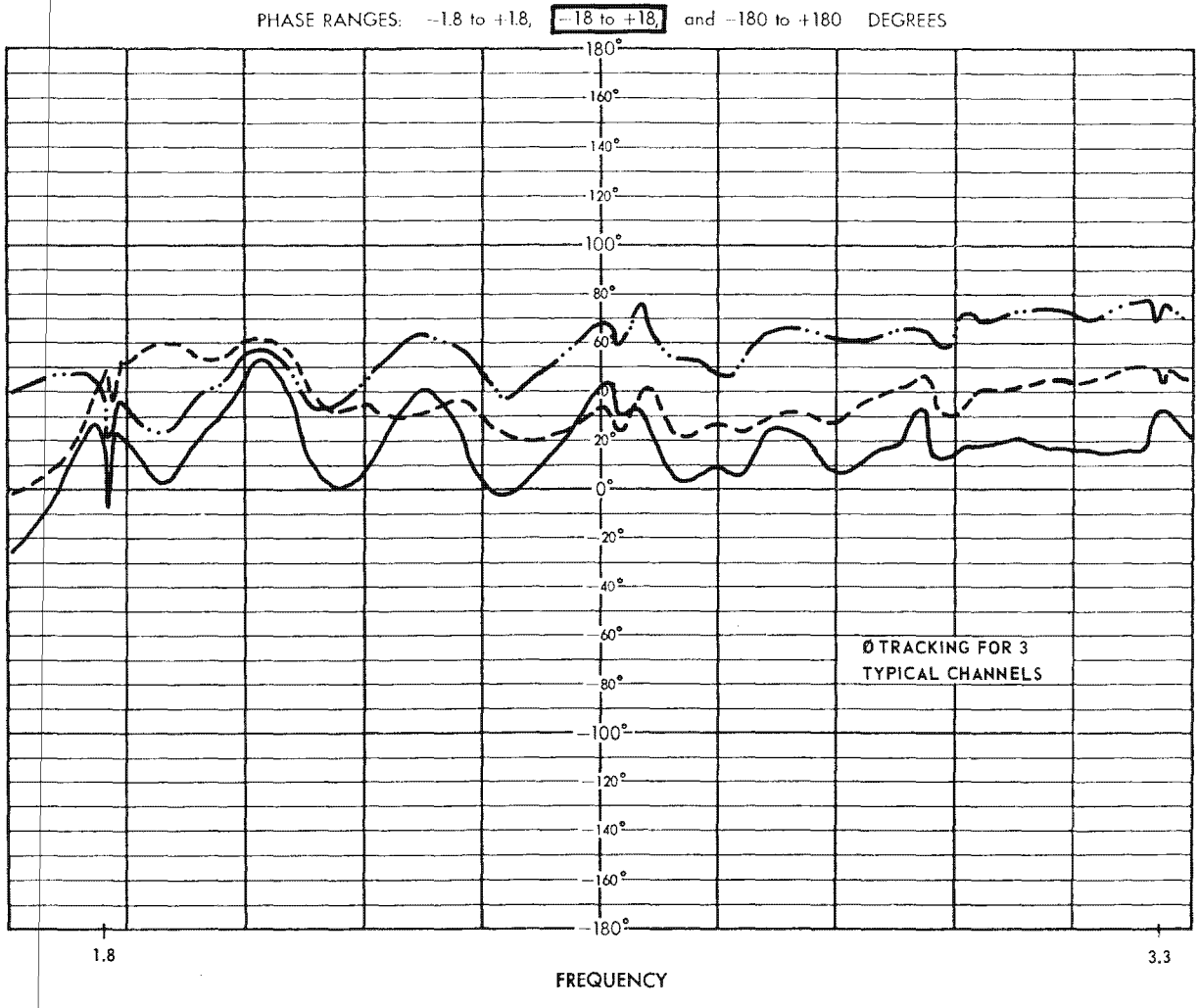

Figure 4.2-22. Main Stripline Phase vs Frequency

50X1

The 3-db hybrid divider feeds the LO signal to two mixers which have a common RF input. The RF is divided in equal amplitude and equal phase to these mixers, and the LO is injected, with a 90° phase offset. This provides two matched IF outputs, 90° offset in phase, which are used in the real-image detection function of the system.

The LO monitor is located adjacent to the LO input port. A 20-db directional coupler samples the LO energy and couples the sample to a back diode detector. The detected energy provides a voltage output, proportional to the LO power level, which is available as a telemetry point.

4.2.4.3 Summary of Main Stripline Specifications

Table 4.2-3 presents a summary of the electrical performance of a typical main stripline assembly and a comparison with the design specificagions.

4.3 Local Oscillator Assembly

4.3.1 Introduction

The local oscillator frequency range of 1780 MHz to 3320 MHz is divided into two frequency bands. The low band frequency covers from 1780 MHz to 2417.5 MHz and the high band from 2420 MHz to 3320 MHz. Each band is scanned in 2.5 MHz steps generating 256 frequencies in the low band and 361 frequencies in the high band.

TABLE 4.2-3. SUMMARY OF MAIN STRIPLINE PERFORMANCE

FUNCTION	TYPICAL	SPECIFICATION
VSWR LO Input	1.8:1	1.8:1
Signal Input	1.5:1	1.6:1
Noise Figure		
Inputs J2-J7	8.0 db	8.5 db
Input J8	11.0 db	11.5 db
LO-RF Isolation	13.5 db Minimum	13.0 db Minimum
IF-IF Isolation	30. db Minimum	30.0 db Minimum
Phase Variation	±3.0°	±5.0°
Phase Tracking	±2.75°	±5.0°
Amplitude Variation	±2.0 db	±2.0 db
Amplitude Tracking	±0.8 db	±1.0 db

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The system contains two yttrium-iron-garnet (YIG) tuned, transistor local oscillators, one for each band, operating in the fundamental frequency mode. Linear frequency tuning is accomplished by changing the current in the tuning coil of the magnetic circuit of the YIG oscillator.

Control circuits for the YIG oscillators consists of a ripple counter, digital-to-analog converter for each oscillator, a tuning-current driver for each oscillator and a reference-voltage regulator.

The two YIG oscillators, current drivers, and reference voltage regulator are mounted in a temperature controlled oven. A proportional controller maintains the oven temperature at 120°F when the sink temperature is below approximately 110°F.

The output of the low band and high band YIG oscillator is connected to the low band and high band receivers, respectively.

4.3.2 Description of Operation

A block diagram of the local oscillator assembly is shown in Figure 4.3-1. The low band and high band local oscillator control circuitry are similar in design and operation. Only the low band will be described with high band differences enclosed in parenthesis.

The basic accuracy of the local oscillator frequency and 2.5 MHz step is derived in an 8-bit (9-bit) digital-to-analog converter. The D/A converter receives from the

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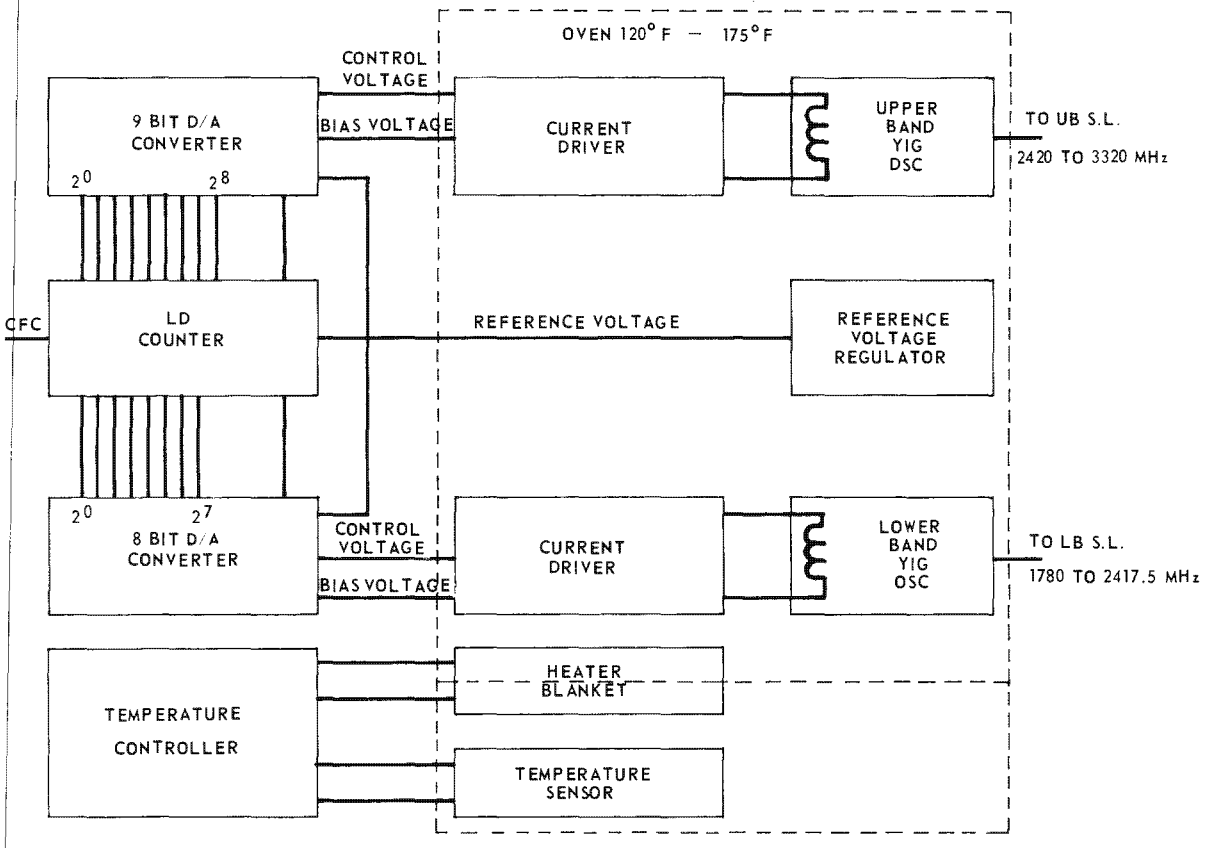

Figure 4.3-1. LO Control Block Diagram

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data handler a band enable signal and an 8-bit (9-bit) digital number from a ripple counter. The 8-bit D/A converter has two operational outputs; bias voltage and control voltage. The bias voltage is switched on by the band-enable signal. The control voltage is a precision staircase voltage that increases in 40 mv (20 mv) steps from zero to 10.2 (7.2) volts as the counter advances from a count of zero to 255 (360).

The outputs from the D/A converter are connected to current drivers. The current driver acts as a true tranconductance that develops a current through the tuning coil of the YIG oscillator proportional to the voltage inputs from the D/A converter. Bias voltage from the D/A converter establishes a tuning current of approximately 880 milliamperes that sets the low frequency of the YIG oscillator at 1780 MHz (2420 MHz). Control voltage from the D/A converter, a stair step voltage, generates the small tuning current steps necessary to increase the local oscillator frequency in 2.5 MHz steps.

Only one band is operable at any one time. The YIG oscillator will not oscillate when the band enable signal and the digital number from the ripple counter are all zeros. Under this condition, the YIG oscillator tuning current is zero. The complete frequency range is scanned by alternately scanning the low band and high band.

The frequency of the local oscillator for any count (N) contained in the ripple counter may be obtained from the following equations:

Low Band

F_{LO} (low band) = 1780 MHz + 2.5 MHz (N)

where:

N = 0, 1, 2, ..., 255.

High Band

F_{LO} (high band) = 2420 MHz + 2.5 MHz (N)

where:

N = 0, 1, 2, ..., 360.

A summary of the local oscillator assembly performance specification is shown in Table 4.3-1.

4.3.3 YIG Oscillators

The local oscillator signal source is a yttrium-iron-garnet (YIG)-tuned microwave oscillator. The heart of the device is a YIG resonator, the passive element, combined with a single microwave transistor. A matching network provides the transformation of the transistor impedance to the output load. The resonant frequency of the oscillator is directly proportional to the magnetic field. The frequency of operation is varied by changing the current through the tuning coil in the magnetic circuit of the YIG oscillator. The output of the oscillators pass through a ferrite isolator that provides load isolation minimizing frequency pulling.

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TABLE 4.3-1. LOCAL OSCILLATOR PERFORMANCE CHARACTERISTICS

PARAMETER	TYPICAL	LIMITS
Low Band		
Frequency Range	1780 to 2417.5 MHz	1780 to 2417.5 MHz
Accuracy	±0.1%	±0.3%
ΔF per step	2.5 ±0.1 MHz	2.5 ±0.5 MHz
Repeatability	±0.5 MHz	±1 MHz
Frequency Stability	±500 KHz in 10 Min	±500 KHz in 5 Min.
Settling Time		
Off to 1780 MHz	200 Milliseconds	263 ± 32 ms (Max.)
2.5 MHz step	2 Milliseconds	2 Milliseconds
Frequency steps	255	255
High Band		
Frequency Range	2420 to 3320 MHz	2420 to 3320 MHz
Accuracy	±0.15%	±0.3%
ΔF per step	2.5 ±0.1 MHz	2.5 ±0.5 MHz
Repeatability	±0.5 MHz	±1 MHz
Frequency Stability	±500 KHz in 10 Min	±500 KHz in 5 Min.
Settling Time		
Off to 2420 MHz	200 Milliseconds	263 ±32 ms (Max.)
2.5 MHz step	2 Milliseconds	2 Milliseconds
Frequency steps	360	360

Power Requirements

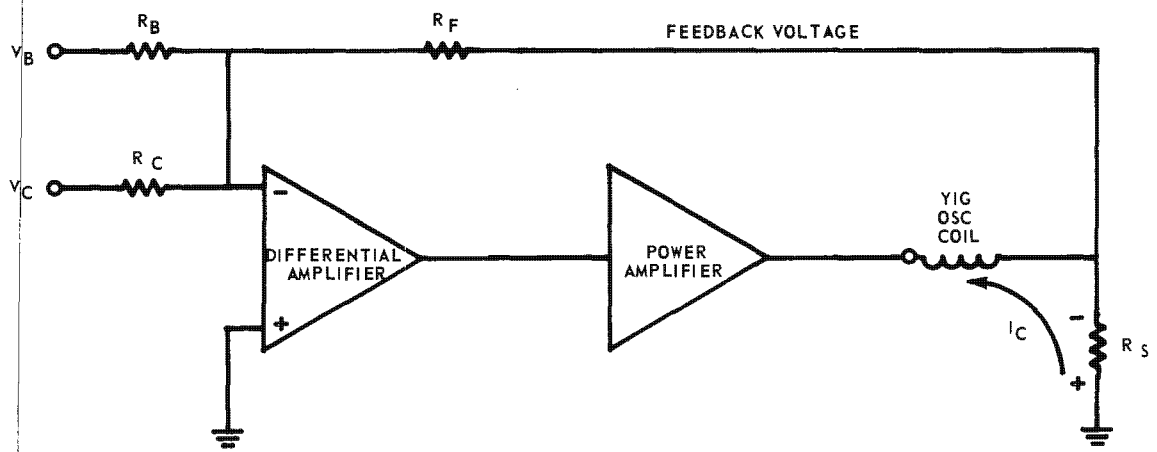
+15 volts floating at 0.8 watts
+15 volts at 0.43 watts
+12 volts at 0.48 watts
+8 volts at 0.05 watts
-6 volts at 6.00 watts (average)
22 to 29.3 volts (aux. power) at 16 watts at -30°F to 0.25 watts at 110°F or greater.

A YIG oscillator is used for both the low and high band. They are similar in design differing only in the ampere-turns of the tuning coil, matching network and YIG sphere or resonator.

A summary of the YIG oscillator performance characteristics is shown in Table 4.3-2.

4.3.4 Current Driver

A functional diagram of the current driver is shown in Figure 4.3-2. Two current drivers are used, one for each YIG oscillator. The current drivers are identical with the exception of the value of R_B and R_C shown at the input to the differential amplifier. Only one current driver will be discussed with differences shown in parenthesis.



$$I_C = -V_B \frac{R_F}{R_B R_S} - V_C \frac{R_F}{R_C R_S}$$

I_C = YIG OSCILLATOR COIL CURRENT
V_B = BIAS VOLTAGE FROM D/A CONVERTER
R_F = FEEDBACK RESISTOR
R_B = BIAS RESISTOR
R_S = YIG OSCILLATOR COIL CURRENT SENSING RESISTOR
V_C = CONTROL VOLTAGE FROM D/A CONVERTER
R_C = CONTROL VOLTAGE RESISTOR

Figure 4.3-2. Current Driver

TABLE 4.3-2. YIG OSCILLATOR PERFORMANCE CHARACTERISTICS

PARAMETER	LOW BAND UNIT	HIGH BAND UNIT
Frequency Range	1780 to 2417.5 MHz	2420 to 3320 MHz
Maximum frequency deviation from straight line between band limits (including temperature effects)	+.15% to -.05%	+.25% to -.05%
Power Output	10 mw ±3 db	10 mw ±3 db
Spurious outputs (below main signal)		
Non-harmonically related	60 db	60 db
20±5 Mc from Main Signal	80 db	80 db
Second harmonic	25 db	30 db
Third harmonic	50 db	50 db
Output Impedance (Nominal)	50 ohms	50 ohms
Residual FM	±50 KHz	±50 KHz
Frequency Response Time		
2.5 MHz step	2 ms	2 ms
0 to lower band edge	200 ms	200 ms
Tuning coil current	880 to 1200 ma	880 to 1200 ma
Tuning Sensitivity	2 MHz/ma	2.8 MHz/ma
DC Oscillator Power	15v floating at 0.4 w	15v floating at 0.4 w

The current driver is basically a high power DC differential operational amplifier connected in a self-balanced feedback-bridge configuration. It consists of a two stage differential amplifier, power amplifier, stable current sensing resistor and adder network.

The current driver receives two voltages from the 8-bit (9-bit) D/A converter, bias voltage and control voltage. Bias voltage is applied to resistor R_B that unbalances the differential amplifier causing current to flow through the YIG oscillator tuning coil and current sensing resistor, R_S, in series with the YIG oscillator tuning coil. Current through the current sensing resistor, R_S, develops a negative voltage that is fed back to the adder network through feedback resistor, R_F. Current through the YIG tuning coil increases until the feedback current through RF and input current through R_B are equal at which time the differential amplifier is again balanced at the input. Control voltage from the D/A converter is applied to resistor R_C causing additional current to flow through the YIG oscillator tuning coil until the input and feedback currents are again balanced at the differential amplifier input. The control voltage from the D/A converter is a staircase ramp that the current driver changes to a staircase current through the YIG oscillator tuning coil. The combined current through the YIG oscillator tuning coil has a waveform that rapidly rises from zero to

approximately 880 milliamperes and then increases in equal increments to approximately 1200 milliamperes returning to zero when the bias and control voltage returns to zero.

A summary of the current driver performance characteristics is shown in Table 4.3-3

TABLE 4.3-3. CURRENT DRIVER PERFORMANCE CHARACTERISTICS

PARAMETER	LOW BAND	HIGH BAND
Bias Voltage (VB)		
(OFF)	0 to 1 mv	0 to 1 mv
(ON)	10.240 v	10.240 v
Control Voltage (VC)	0 to 10.200 v	0 to 7.200 v
Current Output at 120°F		
V_B = 0, Vc = 0	0 ± 10 ma	0 ± 10 ma
V_B = 10.240 v, Vc = 0	880 ma (nominal)	880 ma (Nominal)
V_B = 10.240 v, Vc=10.2v	1200 ma (Nominal)	
V_B = 10.24 v, Vc = 7.2 v		1200 ma (Nominal)
Response Time (0 to 880 ma)	4 ms	4 ms
Linearity (Ic vs Vc)	±0.05%	±0.05%
Supply Voltage Stability	0.01 ma/mv	0.01 ma/mv
Temperature Stability (Ic)	±28 KHz/°F	±28 KHz/°F
Power Requirements	+8Vdc @ .08w -6Vdc @ 6w	+8Vdc @ .08w -6Vdc @ 6w

4.3.5 Digital-to Analog (D/A) Converters

The D/A converters decode digital inputs received from a ripple counter converting them to a precise analog voltage consistent with the count contained in the ripple counter. The system uses two D/A converters, an 8-bit D/A converter that controls the low band YIG oscillator frequency and a 9-bit D/A converter that controls the high band YIG oscillator frequency. See Figure 4.3-3.

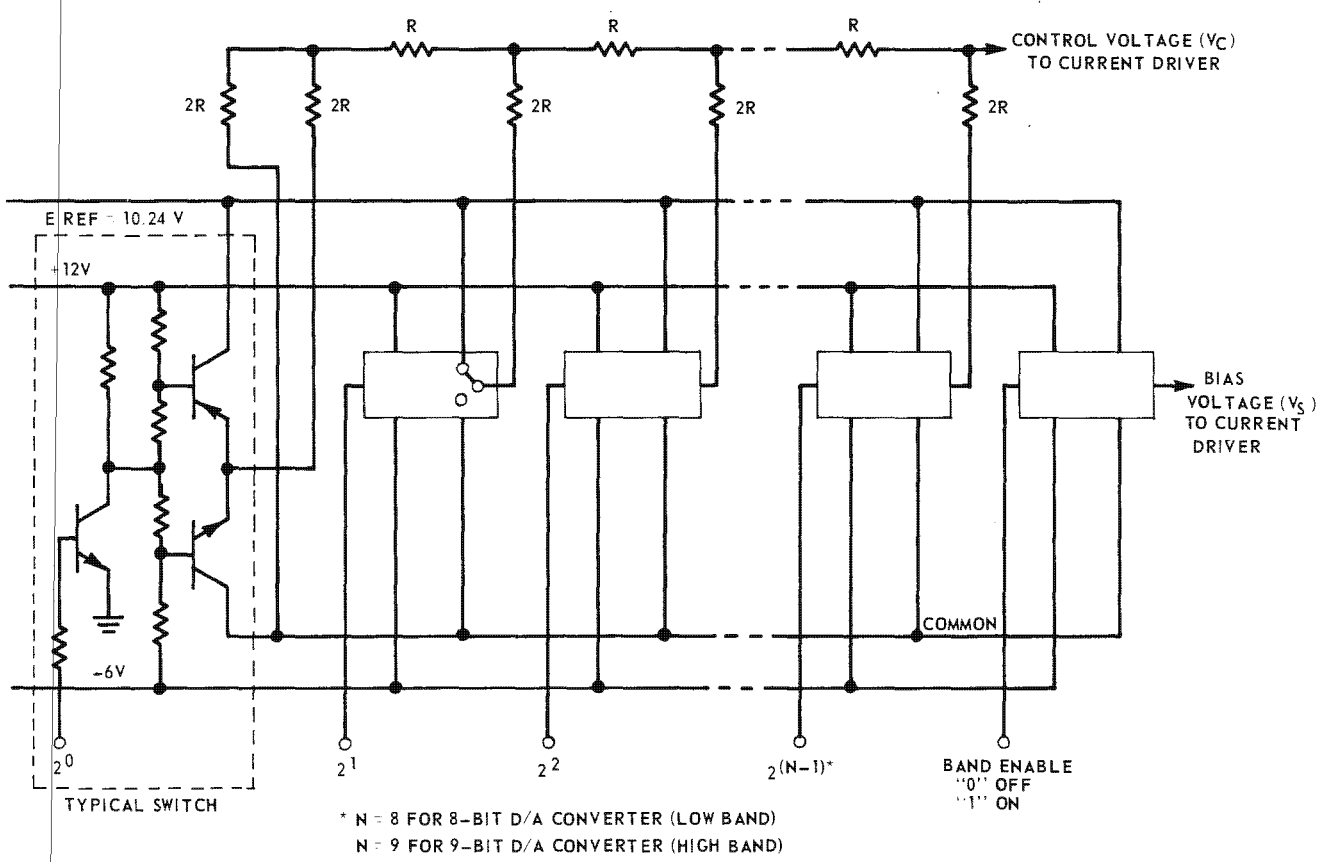


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Figure 4.3-3. Digital-To-Analog Converter

The D/A converter basically consists of a precision resistive ladder network with a solid-state switch for each bit in the ladder. The switches operate as a single-pole double-throw switch that applies a reference voltage to the ladder network in one position and grounds the input in the other position. The switches are turned on or off by parallel fed digital numbers from a ripple counter. The ladder network sums the voltages applied to the network by the switches. The output of the ladder network is a staircase voltage that is fed to the control voltage input of the current driver. Another output, bias voltage, is derived by switching the reference voltage to the current driver when a band enable signal is received from the data handler.

A summary of performance characteristics of the 8-bit and 9-bit D/A converters are presented in Table 4.3-4.

4.3.6 Reference Voltage Regulator

The reference voltage regulator provides a precision reference voltage to the D/A converters. A well regulated temperature-stable reference voltage is necessary for the D/A converters as the local oscillator frequency is directly proportional to the reference voltage. A common series regulator utilizing a two-stage differential DC amplifier, temperature-compensated reference diode and sensitor temperature compensation provides the required stable voltage.

TABLE 4.3-4. D/A CONVERTER PERFORMANCE CHARACTERISTICS

PARAMETER	8-Bit D/A	9-Bit D/A
Reference Voltage Input (E_{REF})	10.240 VDC $\pm$ 10 mv	10.24VDC $\pm$ 10 mv
Digital Inputs		
"Counter	8 bits	9 bits
Band Enable	1	1
Bias Voltage Output		
"ON"	$E_{REF} \pm \frac{0}{2}$ mv	$E_{REF} \pm \frac{0}{2}$ mv
"OFF"	0 to 2 mv	0 to 2 mv
Control Voltage Output		
N = 0	0 to 2 mv	0 to 2 mv
N = 255 (Maximum)	10.2 v	
N = 360 (Maximum)		7.2 v
No. of Voltage Steps	255	360
Voltage per step	40 $\pm$ 2 mv	20 $\pm$ 2 mv
Accuracy	$\pm$ 0.07%	$\pm$0.07%
Temperature Stability	$\pm$10 μv/°F	$\pm$10 μv/°F
Power Requirements		
+12v	0.5 w	0.5 w
-6 v	0.03 w	0.03 w
+10.24 v (E_{REF})	0.04 w/bit	0.04 w/bit

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The reference voltage regulator is housed in the local oscillator oven where the operating temperature range is controlled between 120°F to 185°F.

A summary of the reference voltage regulator performance characteristics is presented in Table 4.3-5.

TABLE 4.3-5 REFERENCE VOLTAGE REGULATOR PERFORMANCE CHARACTERISTICS

FUNCTION	SPECIFICATION
Output Voltage	10.240 Volts ± 10 mv
Output Current	0 to 30 ma
Line Regulation (14.5 V to 15.5 V)	±0.5 mv
Load Regulation (No load to Full Load)	±0.5 mv
Temperature Stability (80°F to 185°F)	±2 mv
Ripple & Noise Output	0.5 mv P-P (Maximum)
Power Requirements:	
Voltage	15 ± 0.5 VDC
Current	50 ma (Maximum)

50X1

4.3.7 Temperature Controller

The local oscillator oven temperature is regulated by a proportional control temperature controller. The LO oven temperature is controlled to 120°F when the sink temperature is below approximately 110°F. At temperatures above 110°F the LO oven temperature is not electronically controlled and rises above the sink temperature proportional to the power dissipation by the local oscillators and LO control circuitry mounted inside the oven.

A functional block diagram of the temperature controller is shown in Figure 4.3-4. Four heater blankets are

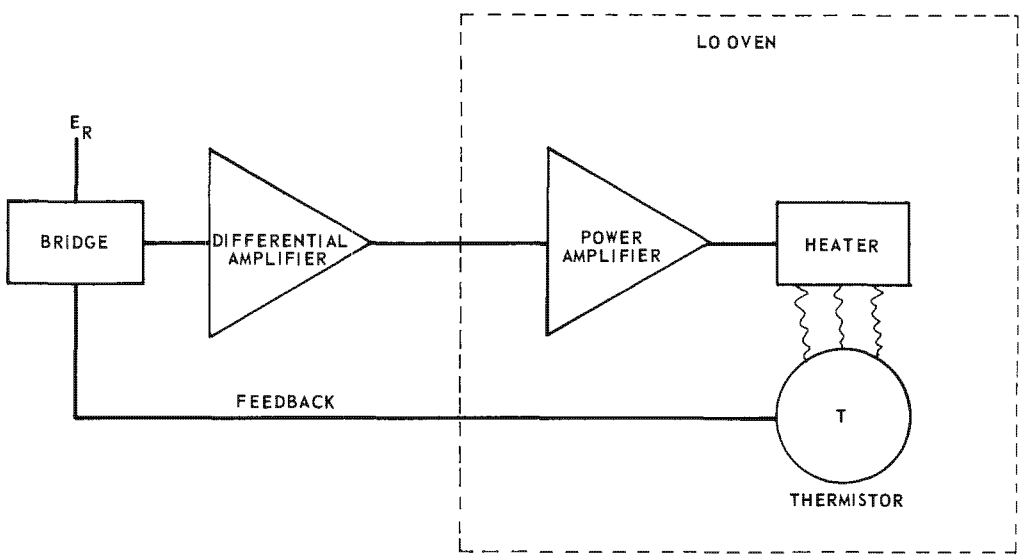

Figure 4.3-4. Temperature Controller

series-parallel connected and mounted in four cavities of a copper plate. The heater blankets are the collector load of a common emitter connected power transistor that is also mounted on the copper plate. The power dissipated by the heater blankets

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and power transistor is regulated by control of the power transistor base current. A thermistor temperature sensor located on the copper plate senses the oven temperature. The proportional temperature controller is located in the D/A converter assembly. A resistive bridge circuit of which the temperature sensor is one leg develops an error voltage proportional to the voltage difference between the reference leg and temperature sensor leg. The error voltage is amplified in a differential amplifier and emitter follower that provides base current to the heater power transistor.

The temperature controller and heaters operate from unregulated auxiliary vehicle power.

Power required for the LO oven heater and temperature controller is a function of sink temperature varying from 16 watts at -30°F to a few milliwatts above 110°F. The LO oven is further discussed in the thermal section, paragraph 9.9.7.

A summary of the performance characteristics of the temperature controller is given in Table 4.9-6.

TABLE 4.3-6 TEMPERATURE CONTROLLER PERFORMANCE CHARACTERISTICS

FUNCTION	SPECIFICATION
Input Voltage	22 to 29.3 volts
Input Current	10 ma to 900 ma
Average Power Input @ 23 V @ -30°F Sink Temperature	16 watts
Oven Temperature:	
(a)-30°F to +110°F Sink Temp.	120°F ± 5°F
(b)+110°F to +160°F Sink Temp.	120°F to 175°F ±10°F
Controller Cutoff Temperature	120°F ± 5°F Oven Temp.

4.4 RF Calibrator

4.4.1 Introduction

The calibrator is an RF generator which produces simultaneous signals at the following frequencies: 1800 MHz, 2100 MHz, 2400 MHz, 2700 MHz, 3000 MHz and 3300 MHz ± 1 MHz. The power on-off and modulation functions are controlled by the data handler.

When the Black Hawk system is energized the data handler issues command to apply voltage to the calibrator every four minutes and the voltage is applied for eight seconds. During this eight-second period, each time a change frequency command (CFC) is issued to the LO, calibrator power is commanded for 4 msec. During this 4 msec period modulation

pulses are supplied by the data handler to the calibrator every 500 usec at a 1-usec pulse width.

Figure 4.4-1 shows the complete RF calibrator. Figure 4.4-2 is a block diagram of the RF calibrator.

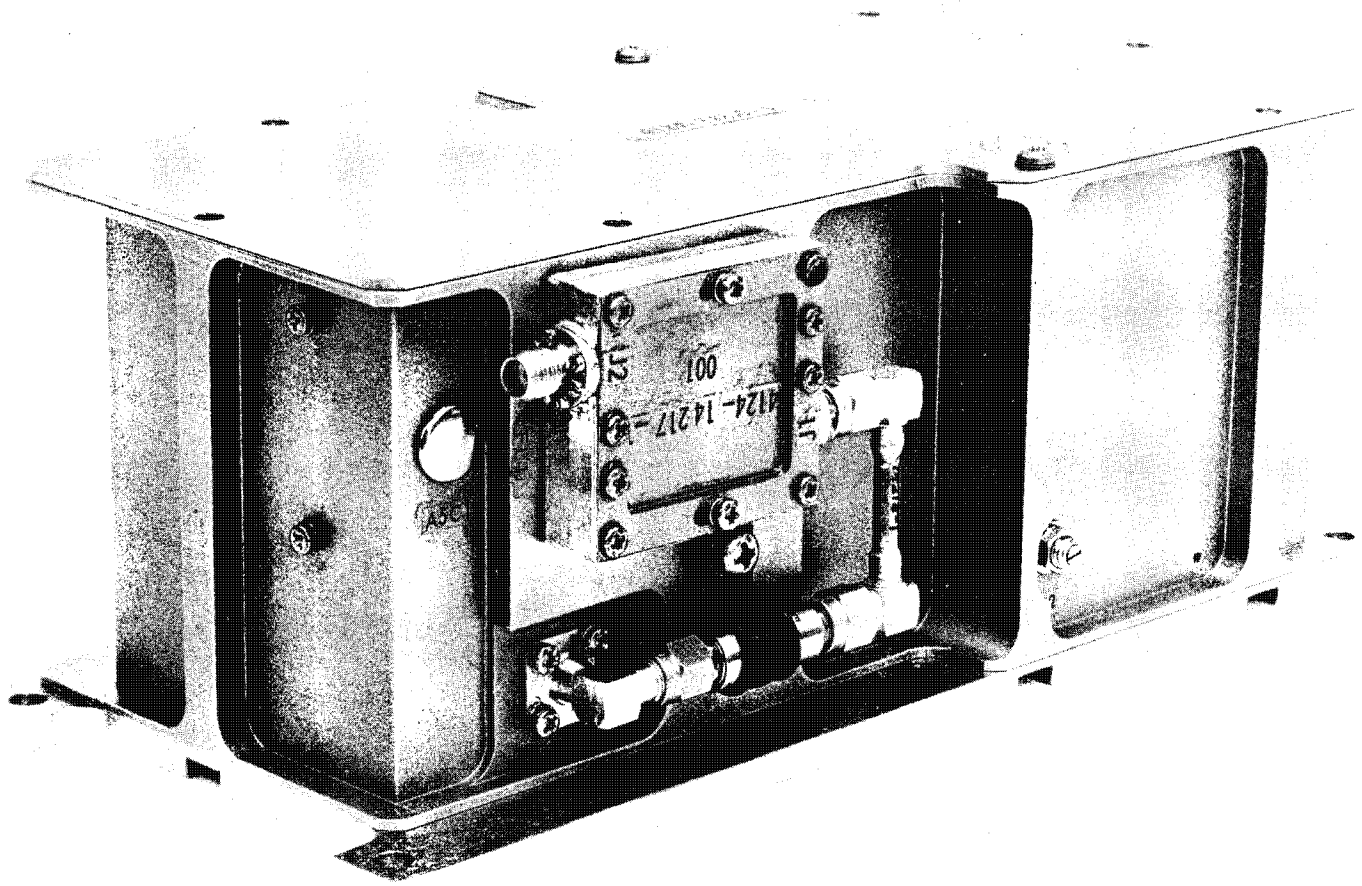

Figure 4.4-1. RF Calibrator

4.4.2 Design

The calibrator signal source is a crystal controlled oscillator operating at 75 MHz. Temperature stable components are used to meet the frequency stability desired so that an oven is not required.

The 75-MHz signal is then multiplied by four in a single transistor stage to obtain 300 MHz. The cw signal from the multiplier is modulated to produce 1-usec pulse every 500 usec.

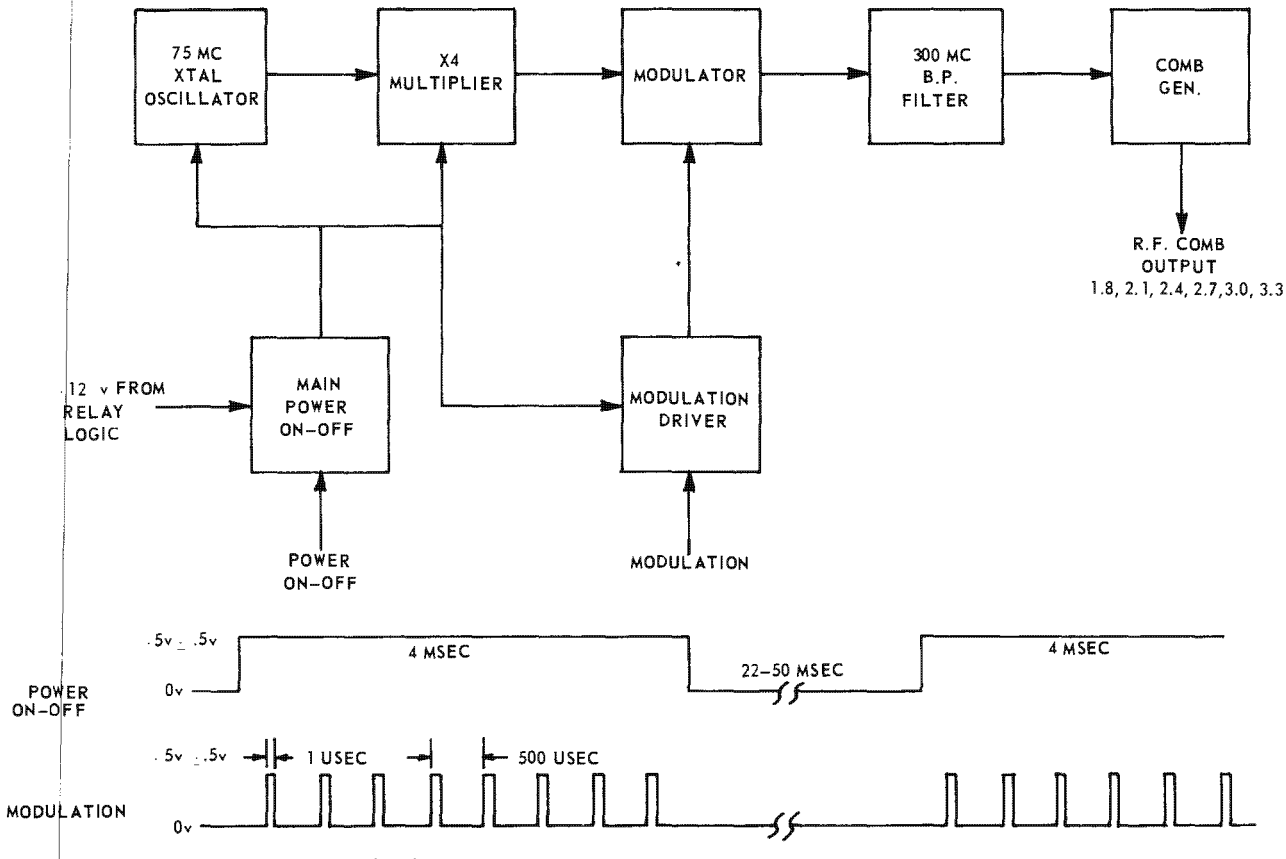

Figure 4.4-2. RF Calibrator Block Diagram

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The modulator consists of a pair of diodes which short out the RF path when no DC voltage is applied. The ON-OFF ratio of the modulator is greater than 50 db. A single stage modulator driver controls the diodes from the data handler command. A "1" on the command line (5.0 volt) turns the RF on, while an "0" on the command line turns the RF off and no signals are emitted.

The X4 multiplier generates other frequencies a-long with the desired 300 Mc. These undesired signals are eliminated by using a 300 Mc bandpass filter. In this manner only the 300 Mc will drive the comb generator.

The comb generators consist of a single step re-covery diode (HPA 0182). The output of the diode is terminated in a 3 db attenuator. The attenuator provides matching be-tween the diode and output filter and its DC path furnishes the DC return for the step recovery diode. The comb generator produces RF signals every 300 Mc across a very wide spectrum. Therefore it is necessary to restrict the output frequencies by using a RF bandpass filter.

The RF bandpass filter is an eight element inter-digital with air dielectric. The RF structure is stripline etched on telfon-fiberglass. The construction is similar to the filter described in Section 4.2-1.

The RF spectrum output is shown in Figure 4.4-3.

The electrical performance data is given in Tables 4.4-1 and 4.4-2.

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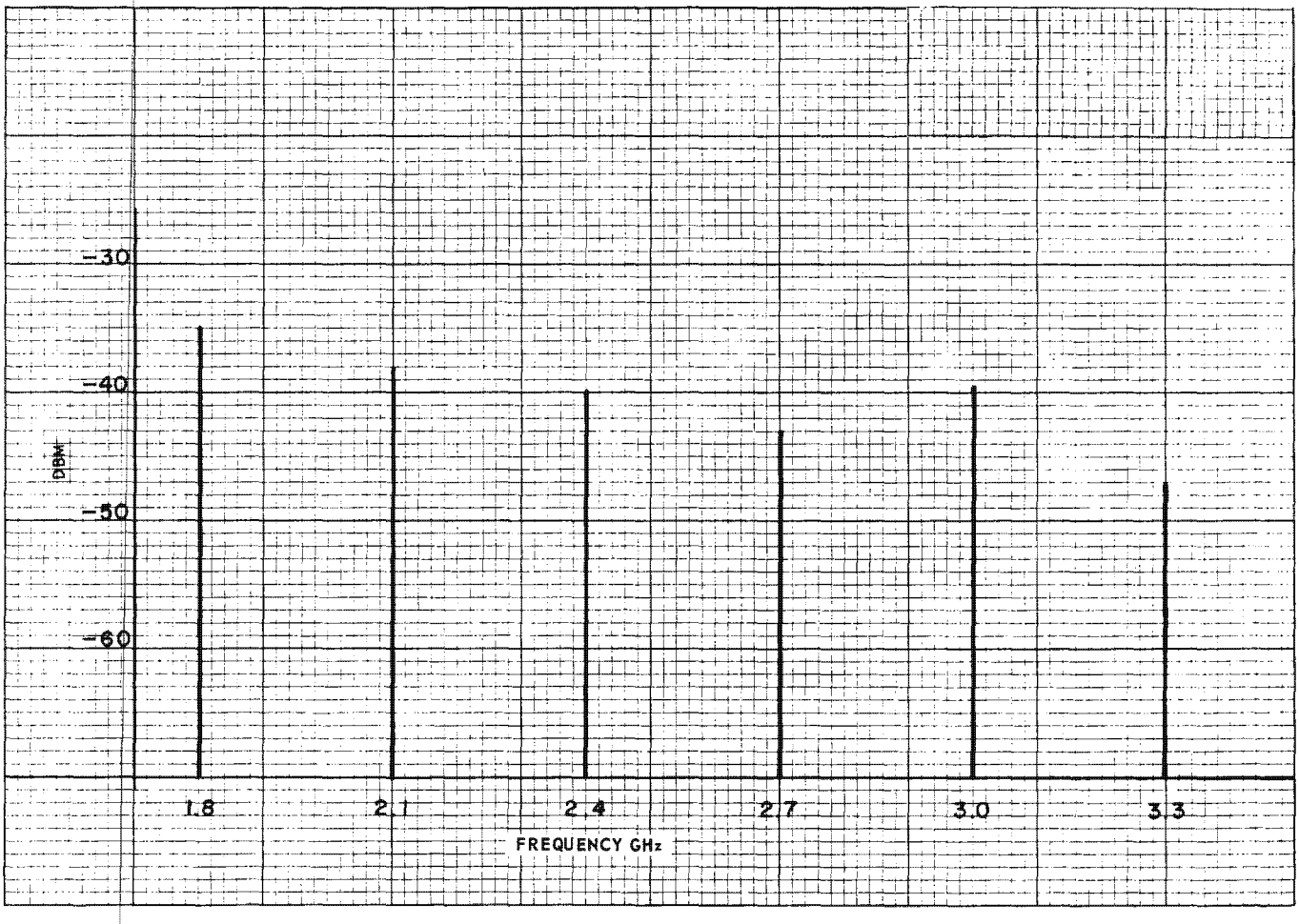

Figure 4.4-3. Calibrator Frequency Spectrum

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TABLE 4.4-1. FREQUENCY DEVIATION VERSUS TEMPERATURE

Temp °F	Freq. (GHz.)	ΔF	$\frac{\Delta F}{F}$	Spurious Level -dbm
RM	3.299834	0	0	-64
-30°	3.299863	+ 29KHz	8.8 PPM	-62
+165°	3.299810	- 24KHz	7.3 PPM	-68

TABLE 4.4-2. SPECTRUM POWER VERSUS TEMPERATURE

TEMP.	OUTPUT FREQUENCY (GHz).					
	1.8 (dbm)	2.1 (dbm)	2.4 (dbm)	2.7 (dbm)	3.0 (dbm)	3.3 (dbm)
RM	-26	-25	-30	-34	-36	-44
-30°	-28	-26	-32	-38	-40	-48
+165°	-30	-30	-40	-46	-48	-50

4.5 Intermediate Frequency (IF) Assembly

4.5.1 Introduction

The IF assembly consists of circuitry required to accept signals from the balanced mixers in the RF assembly and provide the basic input functions to the data handler. The following outputs are provided.

(1) Phase relationships between channels A, B, C, D. and R in binary coded form.

(2) Absolute amplitude information in binary coded form.

(3) A means of confirming the incoming frequency if it is within the 20 MHz $\pm$ 1.75 MHz limits.

(4) Fine-frequency information in binary coded form.

(5) A T_{min} confirm signal which is generated if the amplitude of the incoming signal is greater than the minimum signal that the system is designed to process.

(6) A signal-indicate (SI) confirm signal which is generated when the incoming signal is greater than 3 db below T_{min}. This signal initiates system data processing.

(7) A signal-indicate confirm signal in the presence of CW. SI in the presence of CW replaces the normal SI and occurs when the

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incoming signal is 15 db greater than the CW.

(8) A T_{max} inhibit signal which indicates that the incoming signal is greater than the maximum allowable amplitude that the system is required to process.

(9) An amplitude-ration inhibit if the amplitude of the F_2 channel exceeds that of the C channel by a predetermined amount.

(10) A pulse-width confirm if the intercepted pulse width is greater than 400 nano-seconds.

(11) A signal-indicate confirm signal which initiates recognizer processing.

(12) A "real" confirm signal when the incoming signal is 20 MHz above the local oscillator frequency.

(13) A real-or-image confirm signal when the incoming signal is 20 MHz above or below the local oscillator frequency.

(14) A predetected signal whose amplitude, frequency, and pulse width are proportional to the incoming signal. Two reference tones (6 MHz and 46.875 kHz) and a 250-kHz tag pulse which indicates that the emitter is inside the A/R circle are contained in the predetected output.

(15) Three amplitude-confirm pulses when the incoming signal is greater than 10, 20, or 30 db above T_{min}. These signals set predetector gain during the record interval.

(16) A recognizer amplitude-confirm signal whose threshold is controlable to 0, 5, 10, or 15 db above T_{min}.

The IF assembly consists of the following subassemblies: Sixteen IF preamplifiers, two pre-amp switches, four IF phase channels, one frequency confirm channel, two log IF amplifiers, one amplitude-ration (A/R) and pulse-width confirm unit, one signal-indicate (SI) generator, one real and image channel, an analog-to-digital (A/D) converter, one signal combiner, one quadrature hybrid, one signal recognizer unit, and one predetector unit. See Figure 4.5-1.

The preamplifiers, preamp switches, signal combiner and quadrature hybrid are located on the antenna side of the unit. The remaining subassemblies are located in four adjacent chassis mounted on the reverse side of the unit. Signal coupling between subassemblies is accomplished with co-axial cables.

Four techniques are used to insure temperature stability in the IF assembly. First, each circuit has been developed using temperature-stable configurations, where possible, without compromising performance. Second, temperature

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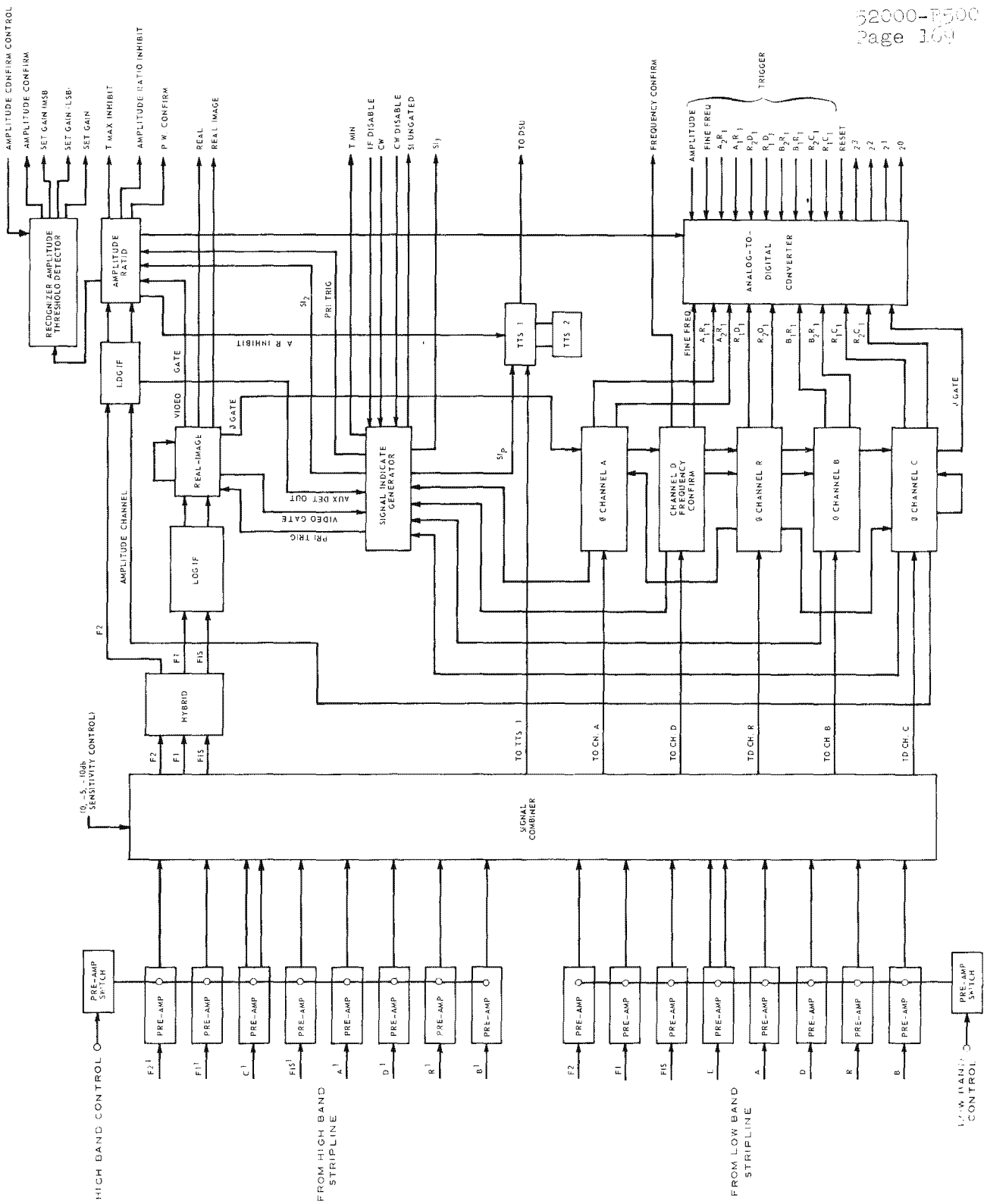

Figure 4.5-1. IF Assembly Block Diagram

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sensitive resistors (sensistors) have been used in circuits which require a positive temperature-coefficient. Third, diodes are used for compensation where negative temperature-coefficients are needed; and fourth, thermistor-sensitive-hybrid combinations are used where non-linear compensation is required.

Decoupling networks have been used throughout the IF assembly to provide isolation between states and to serve as a path to ground for any signal that might be on the power lines coming to the IF assembly

4.5.2 Preamplifier Subassembly

4.5.2.1 Introduction

The system contains sixteen preamplifiers of which eight are used for each RF band. The preamplifiers are packaged in three separate housings mounted around each stripline assembly. The circuitry is a three-stage modular design.

In the first module, a tuned input transformer takes the output from the balanced mixer and couples it into a high-gain, low-noise stage. A neutralization loop is incorporated to increase the amplifier stability. Negative feedback from the output network is used to provide a low input impedance, to increase the dynamic range, and to stabilize the circuit for temperature and bandwidth variations. A resistor coupled to the center tap of the input transformer provides a path for mixer diode bias.

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The second module has a tuned transformer for additional selectivity. This transformer has two outputs. The first is a narrow band output which is applied to the succeeding amplifier and the second is a wide band auxiliary output which is used to drive the predetector. This second output is internally terminated in all preamps except the two (one in each band) used for derivation of the predetected signal. The amplifier in this module is used mainly as a buffer stage. Negative feedback from the collector circuit, and emitter degeneration, are used to decrease gain and provide greater isolation, to increase the dynamic range, and to stabilize the grounded emitter type circuit for temperature variations.

The third module has a tuned circuit which further reduces the noise bandwidth and couples to the output emitter follower stage. The emitter follower stage has provision for gain adjustment of the preamplifier and provides current drive for the switching diode in the following combiner and attenuator subassembly.

4.5.2.2 Summary of Technical Specifications

Pertinent electrical specifications are presented in Table 4.5-1.

4.5.3 Signal Combiner Subassembly

4.5.3.1 Introduction

The signal combiner subassembly contains nine identical modules. Each module consists of an input diode

TABLE 4.5-1 PREAMPLIFIER SPECIFICATIONS

FUNCTION	CHARACTERISTIC
Dynamic Range	-95 to -45 dbm
Band Center	20 MHz ± 0.2 MHz
Bandwidth (3 db)	Normal 6 to 6.5 MHz Pre-D App. 10 MHz
Gain	34 db ± 1 (nominal) into a 50 ohm load
Linearity	±0.25 db over the dynamic range
Noise Figure	2 ± 0.3 db
Input Impedance	Approximately 70 ohms balanced to the crystal mixer
Output Impedance	50 ohm resistive

switch, an amplifier and a remote control attenuator. The preamplifiers from each band feed their outputs to this sub-assembly. The signal utilized by the predetector uses the ninth module. Band switching is performed at the inputs to each module by switching diodes in series with each input terminal. The remote attenuator function operates simultaneously in each module when commanded by the data handler. Two 5-db levels of attenuation are provided when a logic 1 is fed to either terminal E4 or E3.

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The internal functions of each module are divided into three sections. The input and switching section, the amplifier and attenuator section, and the output section.

The first section contains the input diodes and their common d-c load resistor. The signal is capacitively coupled into the amplifier section through the series RC network which is designed to transform the input impedance of the amplifier to 50 ohms resistive. Band switching in each channel is performed by the input diode whenever current drive is provided by the preceeding preamplifier. The preamplifier in the other band is simultaneously turned off removing the current drive to the alternate input diode causing this input to be shut off by back bias from the "on" preamp current drive.

Transistor Q1, the second section amplifier, provides signal gain to overcome circuit losses and boost the overall channel gain. It is a grounded base amplifier which is capacitively coupled to the attenuator series-resistance arm. The attenuator shunt resistances are switched in by switching diodes whenever current drive is fed into either control terminal E4 or E3.

The third section is the direct coupled output emitter follower amplifier, Q2, which provides power gain and buffering between the attenuator network and the 50-ohm output circuit.

4.5.3.2 Summary of Technical Specifications

Pertinent electrical specifications for a typical channel are presented in Table 4.5-2.

TABLE 4.5-2 SIGNAL COMBINER SPECIFICATION

FUNCTION	CHARACTERISTIC
Dynamic Range	-60 to -20 dbm -55 to -15 dbm -50 to -10 dbm
Attenuation Control	0, -5, -10 db
Bandwidth	(-3 db points) 8 to 32 MHz
Gain	10 db Max (nominal) into 50 ohm load
Input Impedance	Approximately 50 ohms resistive
Output Impedance	(Same as above)

4.5.4 Hybrid Subassembly

4.5.4.1 Introduction

The hybrid subassembly contains four modules. See Figure 4.5-2. Module A-2 contains a four-port quadature hybrid specifically designed for the 20 MHz IF band center and a 50-ohm coaxial line impedance. Modules A1, A3, and A4 are identical IF amplifiers as used for the first IF amplifier in the phase channel subassembly. This subassembly provides the basis for real or image signal identification by sensing the phase of the incoming signal from the signal combiner sub-

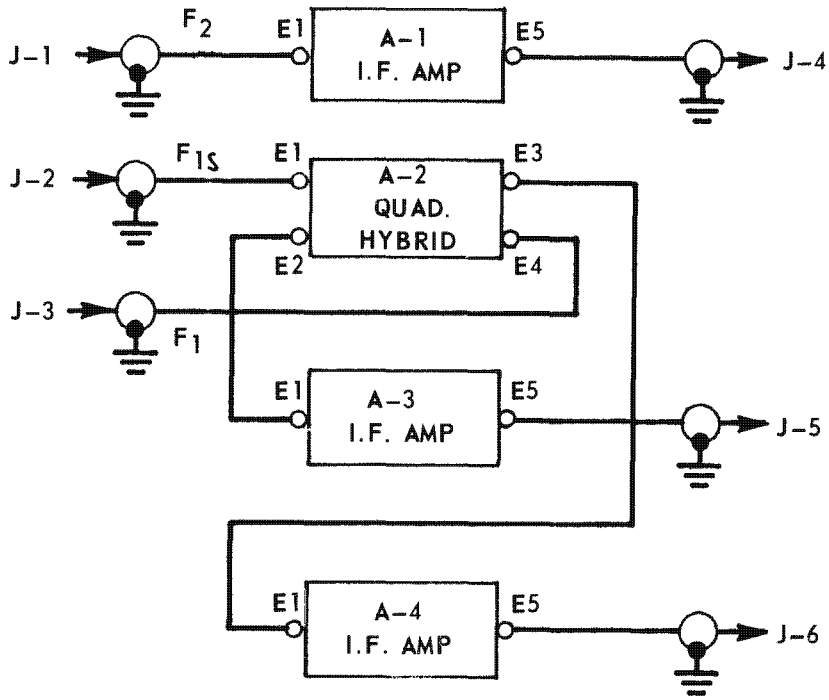

FIGURE 4.5-2 HYBRID

assembly. For a "real" signal a quadature phase shift is developed in the stripline between channels F_1 and F_{1S}. The output from the mixers is fed to the preamps and combiner sub-assembly for these two channels. Delayed channel F_{1S} is fed into J-2 while the in-phase signal of channel F_1 is fed into J3. This signal condition is phase shifted through the Module A-2 quadature hybrid and amplified. The phase-boosted signal is amplified through A-3 and fed to J-5 while the phase-nulled signal is amplified through A-4 and fed to J6.

The "real" signal creates an output at J-5 which is greater than 26 db above the low output at J-6. When an image signal enters the stripline subassembly, reversed phase

characteristics are developed through the F channels which cause the output amplitudes to be reversed. The output at J-6 is then 26 db over the output at J-5.

These signals are fed to the following log IF sub-assemblies for each channel.

The amplifier in module A-1 equalizes the gain to the log IF in channel C.

4.5.4.2 Summary of Technical Specifications

Pertinent electrical specifications is presented in Table 4.5-3.

TABLE 4.5-3 HYBRID SUBASSEMBLY SPECIFICATIONS

FUNCTION	CHARACTERISTICS
Input Level	(all jacks) -10 dbm Max. -60 dbm Min.
Bandwidth	J-1 Input, (Approx. 10-30 MHz at -3 db points)
	J2 & J3 Inputs, 20 ± 4 MHz at -3 db
Gain	J1 Input, 17 db
	J2 & J3 Inputs, 20 db
Phase Quadature	90° ± 3°
Impedance	Input and Outputs, 50 ohms

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4.5.5 Preamplifier Switch Subassembly

4.5.5.1 Introduction

The Preamplifier Switch Subassemblies switches the +12 volt power to the eight preamplifiers in each band. Two preamplifier switch assemblies are used, one for each band. The switch is controlled by a logic input from the digital subassembly. Only one switch at a time is commanded "on."

The preamplifier switch is constructed in a one module subassembly that is mounted with the preamplifiers for each band. The circuit consists of three stages. The first stage is an emitter follower amplifier that provides isolation and power gain to prevent loading of the digital command. Its output is direct coupled through a current limiting resistor to a saturating driver amplifier, Q2. The third stage is a switching transistor which is driven into saturation for turn-on when Q2 is saturated.

4.5.5.2 Pertinent Data

TABLE 4.5-4 PREAMP SWITCH SPECIFICATION

Input:	Logic "one" 4.0 ± 0.5V
Output:	+11.7 ± 0.5V

4.5.6 Intermediate Frequency (IF) Phase Channels (51000)

4.5.6.1 Introduction

The four IF phase channels and one frequency confirm channel are located in the IF assembly and receive input signals from the signal combiner which in turn receives inputs from the preamplifiers. The IF phase channels and frequency confirm channel perform the following functions over the 40-db dynamic operating range.

(1) Provide dc levels with the amplitudes proportional to the corresponding input signal phase.

(2) Provide a video pulse, the amplitude of which is proportional to the IF frequency.

(3) Provide the frequency confirm signals.

(4) Provide the log IF subassembly with a linearly amplified signal from channel C for amplitude measurements.

(5) Provide the signal-indicate generator with a signal from channels A, B, C, and D.

Each phase channel contains certain basic modules that are used in each of the four phase channels. However, one channel is different in the way that it is internally connected. In this portion of the report, a modular breakdown description of phase channel A which is considered to be a

typical channel, is discussed. Also, discussion follows describing how each individual phase channel differs in performing its function in the System. See Figures 4.5-3 and 4.5-4.

4.5.6.2 Channel A

Channel A receives the 20 MHz signal from the channel A preamplifier through the signal combiner. These signals are amplified in the first and second IF amplifiers and limited in the first and second limiters. A boresight module between the first and second IF amplifier serves to adjust the phase of the signal. The signals at the output of the second limiter are then restored to sine wave form by the phase channel filters. The signals at this point have a maximum peak-to-peak amplitude of 2.2 volts and will vary only 5 db over the 40 db dynamic input range. The channel A filter output is coupled to four different points, two internal and two external to the channel.

One of the external outputs is not used. The other is coupled by a coaxial cable to the SI generator. One of the internal outputs goes through the 90° phase shifter to a third limiter, third limiter amplifier, high level amplifier, squaring circuit and to one input of a phase detector. This signal is called A_2. The signal that is coupled directly to a third limiter, third limiter amplifier, high level amplifier, squaring circuit and to one input of the second phase detector is called A_1.

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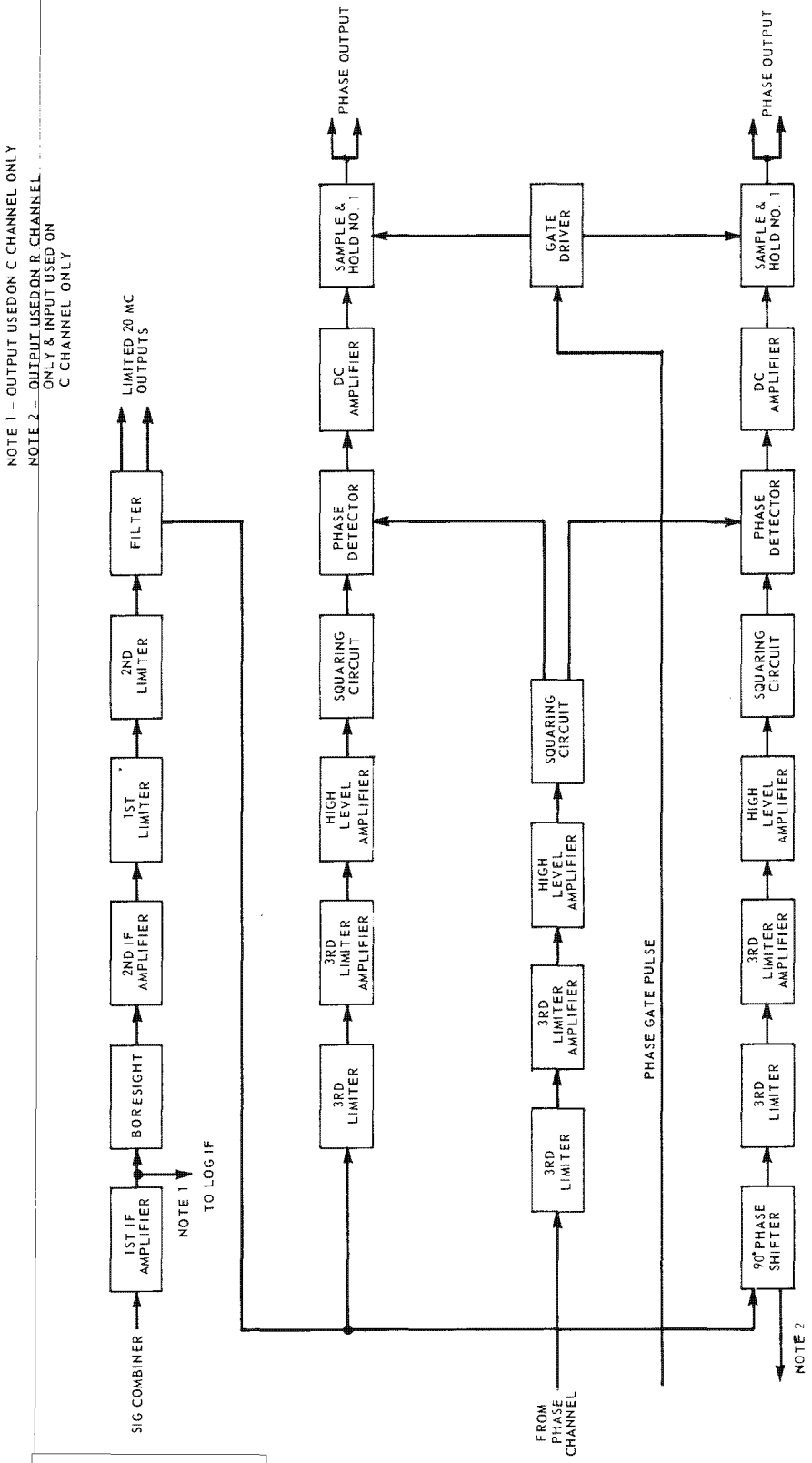

Figure 4.5-3. Typical IF Phase Channel

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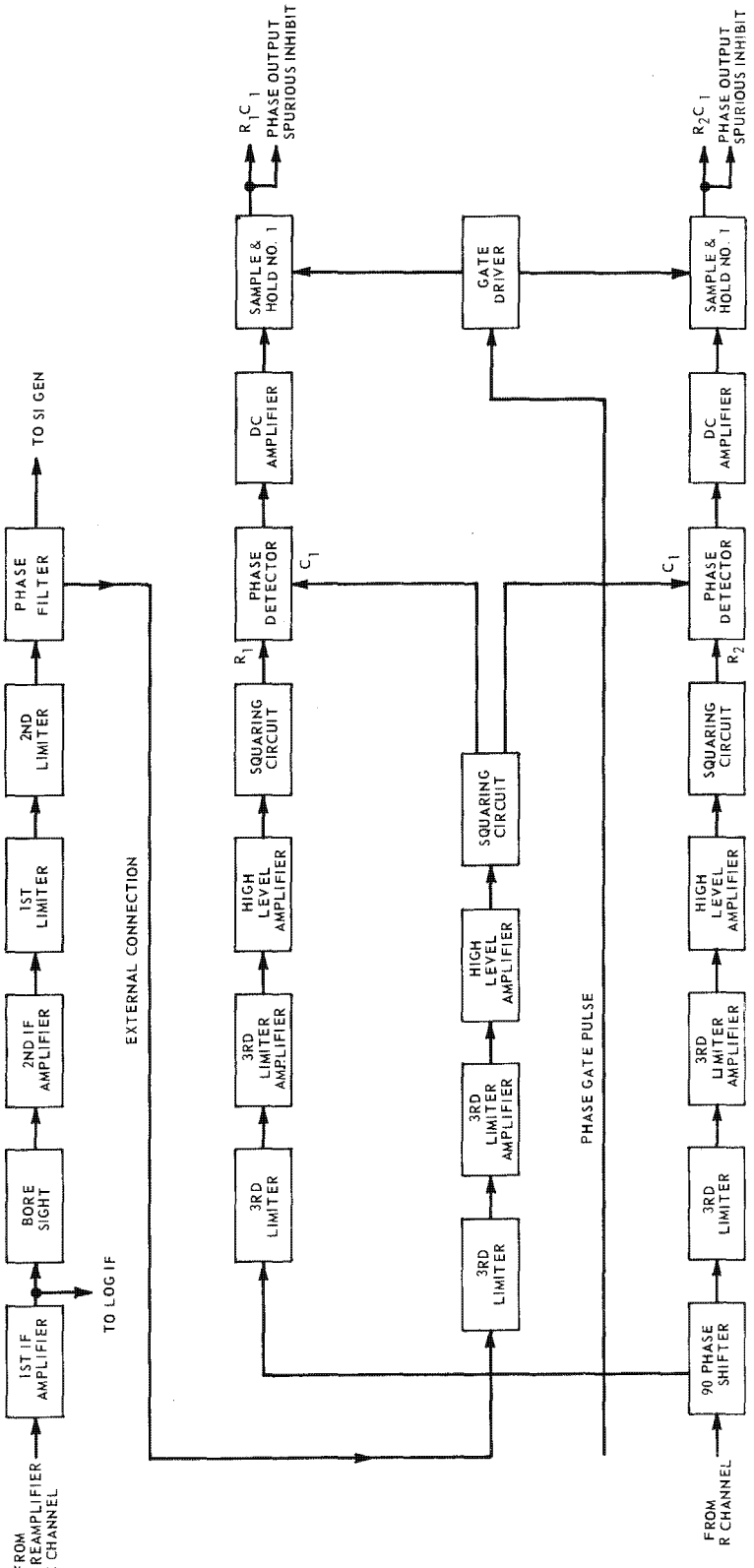

Figure 4.5-4. IF Phase Channel C

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A signal from the filter of channel R is coupled into channel A and continues to a third limiter, third limiter amplifier, high level amplifier, squaring circuit and then to one input of each of the two phase detectors. This signal is called R_1. The output of the first phase detector is called A_1R_1 and the output of the second phase detector is called A_2R_1. The A_1R_1 signal is coupled to a DC amplifier and then to the sample and hold. Here it is gated and held then coupled by coaxial cable to the A/D converter. A_2R_1 also goes to a DC amplifier and sample and hold A_2R_2 is also coupled by coaxial cable to the A/D converter.

4.5.6.2.1 First IF Amplifier Module

The first IF amplifier is a linear, untuned, grounded base amplifier. The input impedance is set to give a 50-ohm resistive load to the coaxial line from its respective signal combiner output. Wide bandwidth, minimum phase distortion, and good temperature stability are obtained with this RC coupled amplifier. A power gain of 17 db with an upper (3 db down) roll-off frequency of 28 MHz is obtained with this circuit. An amplitude change of less than ± 0.5 db is maintained over the temperature extremes. The output consists of two emitter followers which provide isolation for coupling to the boresight module and to the log IF subassembly. The signal output to the boresight is taken from the output of the first emitter follower, while the output to the log IF is taken from the output of the second emitter follower.

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4.5.6.2.2 Boresight Module

From the first IF amplifier, the signal goes on to the boresight module. Any phase difference between channels occurring through the IF phase channel or differences in phase arrival from the RF Assembly Unit are corrected by this circuit. The boresight amplifier is a split load inverter circuit in which the normal and phase inverted signals are combined through an RC phase shifter into one phase controlled output. The phase inversion is made greater on the collector output so that no signal loss occurs through the circuit. The boresight adjustment is made by trimming capacitor, C_1. The normal range of adjustment is $\pm 10°$ at the 20 MHz band center frequency. Bandwidth is kept to a 28 MHz roll-off (-3 db) frequency by use of low collector load resistance which is direct coupled into the input emitter follower of the second IF amplifier.

4.5.6.2.3 Second IF Amplifier Module

The second IF amplifier is also an untuned, RC coupled grounded base amplifier. It consists of three stages; the first stage is an emitter follower which receives its operating bias from the boresight module and provides the impedance transfer and power gain required to drive the low input impedance of the second stage. The second stage is the grounded base amplifier which is direct coupled to the emitter follower output stage.

Wide bandwidth and low phase distortion with good temperature stability are obtained with this design. A power gain of 17 db is obtained with an upper (-3 db) roll-off frequency of 28 MHz. An amplitude change of less than $\pm$0.5 db is maintained over the required temperature range. The output emitter follower stage drives the first limiter in the phase channel.

4.5.6.2.4 First Limiter Amplifier Module

The first limiter amplifier (Figure 4.5-5) is basically a standard amplifier consisting of a common collector amplifier driving a DC coupled common base amplifier. The input of the first limiter varies over a 40-db dynamic range.

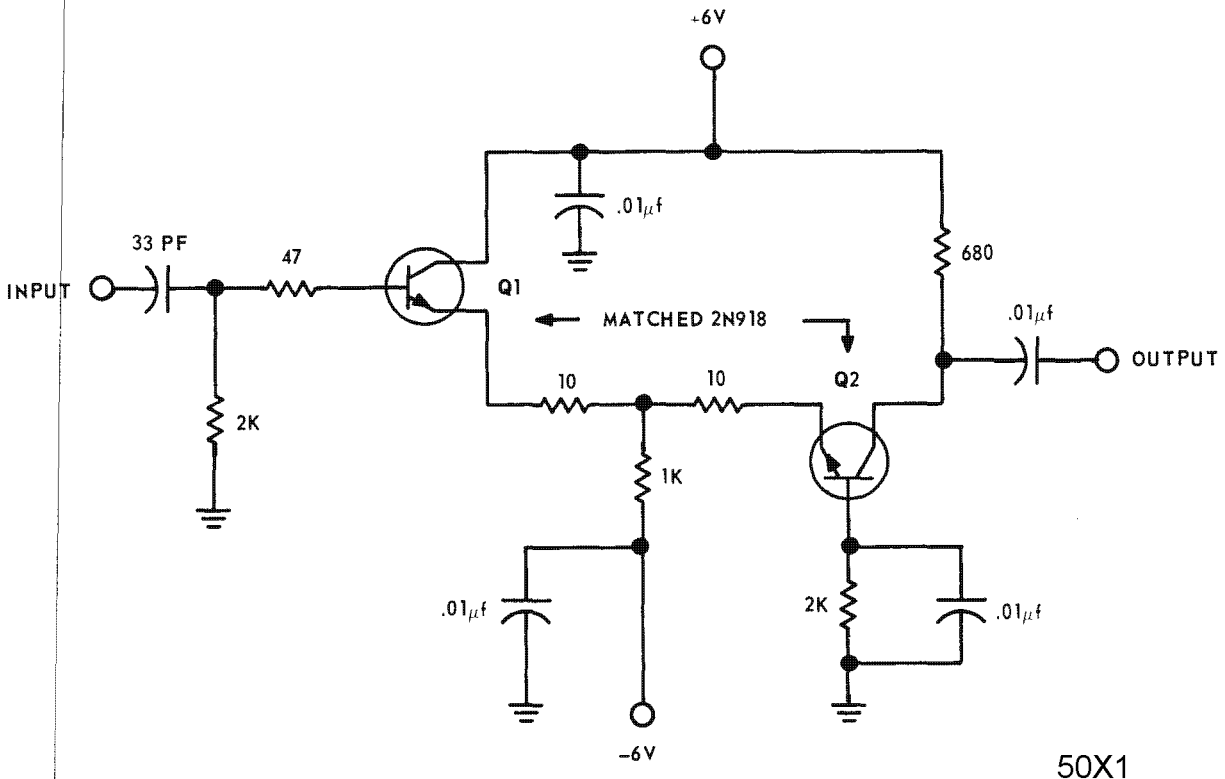

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Figure 4.5-5. First Limiter

The output is limited over the top 17.5 db of dynamic range and decreases in a linear manner for signals below this level. The limiting on the positive half cycle of the incoming signal is obtained when the common collector amplifier emitter goes positive, with respect to the emitter of the common base amplifier, and causes the common base amplifier to be cut off. The limiting on the negative half cycle is obtained by the input signal driving the common collector amplifier to cut off. The current in the common base amplifier is then limited by 1 K resistor in the emitter circuit, which prevents the amplifier from saturating. The resistor in the base of the common base amplifier is AC by-passed; and selected so as to provide a constant zero cross over point of the AC signal over the dynamic range. The module has a 17-db gain when it is not in the limiting conditions.

4.5.6.2.5 Second Limiter Amplifier Module

Since the first limiter has 17.5-db limiting its output will vary by 22.5 db for a 40-db change in the input. The second limiter also has 17.5-db limiting. Therefore, the 22.5-db change at the input results in a 5-db change at the output. This means that for a change on the input of the first limiter amplifier of 40-db, the output of the second limiter amplifier will change by 5-db. The output of the second limiter amplifier will vary in a linear manner below the limiting level.

4.5.6.2.6 Filter Module

The purpose of the filter in the IF phase channel is to restore the signal that has been limited in the first and second limiter amplifiers to a sine wave. The filter is a low pass filter designed to be 3-db down at 20 MHz; attenuating at a rate of 12-db per octave. The signal at this point should be a sine wave for two reasons. (1) The 90° phase shifter needs a sine wave input in order to operate properly, and (2) since the signal is transferred from one subassembly to another, it must be a sine wave in order to prevent phase distortion. A darlington circuit is used in the output for a low impedance driving source.

4.5.6.2.7 90° Phase Shifter

The 90° shifter is placed in one of two identical circuit branches driven by the filter. The phase shifter is used to obtain a second phase difference curve for referencing purposes. A phase splitting circuit is used in which the collector signal and emitter signal are summed through a resistor-capacitor combination to obtain the desired 90° shift. The transistor itself will also have a shift or delay, and this delay will be frequency sensitive. To compensate for the effect that the transistor will have, another transistor amplifier is used. The input to the transistor containing the phase shifting network is also coupled to the other amplifier in such a way that the only thing affecting the phase

shift is the RC network.

4.5.6.2.8 Third Limiter Module

The third limiter provides approximately 10 db limiting. The limiting is accomplished by biasing a PNP emitter follower, 0.2 volt above cut-off, followed by a NPN emitter follower biased 0.2 volt above cut-off. The result of this limiting is to produce a square wave that is 0.4 volt peak-to-peak. The input of the third limiter comes from either the 90° phase shifter or the filter. It has a maximum input of approximately 2.2 volts and decreases to 1.0 volt at the lower end of the 40-db dynamic range, which is sufficient drive for the following third limiter amplifier.

4.5.6.2.9 Third Limiter Amplifier Module

The third limiter amplifier is a standard amplifier with a gain of approximately 14 db. Its output is constant at approximately 1.9 volts.

4.5.6.2.10 High Level Amplifier Module

The high level amplifier is a standard amplifier that is driven into saturation to produce an output voltage of 6 volts peak-to-peak. Its gain is approximately 10 db. It is used to drive the squaring circuit.

4.5.6.2.11 Squaring Circuit Module

The squaring circuit has an input signal of 6 volts peak-to-peak and produces a square wave of 2 volts peak-to-peak from its output. The first transistor is an NPN emitter follow-

er that is biased to 1.0 volt on its emitter. When the input goes negative by more than one volt, the transistor is cut off. The emitter of the NPN transistor provides the bias for the second transistor, which is a PNP. The emitter of the PNP is connected to a positive voltage source through the emitter resistor. The voltage source is adjusted so that the voltage drop across the resistor is 1.0 volt. As the signal on the PNP base goes more than 1.0 volt positive, the transistor is cut off, producing a 2-volt peak-to-peak output signal that is a square wave with rise and fall times in the order of 3 to 5 nsec. This output is one of the signal inputs used by the phase detector for phase difference measurements.

4.5.6.2.12 Phase Detector Module

Phase measurement is accomplished by measuring the difference in signal arrival in one channel with respect to another. Phase measurements are made by utilizing the inputs and outputs of four IF channels and one frequency confirm channel. Outputs are available to indicate the phase difference between channels A-R, B-R, R-C, R-D. As can be noted in the Figure 4.5-2, there are three sets of identical circuitry consisting of a third limiter, third limiter amplifier, high level amplifier, and a squaring circuit. Two of these branches derive their inputs from within that channel, while the remaining center branch obtains its input from a filter located in another channel which is to be phase compared. The externally

fed branch is an input source to both phase detectors. It should be noted that one of the branches in the reference channel described above is shifted by 90 electrical degrees, for reasons to be discussed later, with respect to the branch which obtains its input from the same place.

To designate that a signal has been delayed 90 electrical degrees, the subscript 2 is added to the designation of the channel. If the signal has not been shifted by 90°, the subscript 1 is added. For example, A_2 means that this signal has been delayed 90° with respect to A_1. Signals arriving at the phase detector are 20 MHz square waves, which are symmetrical about zero.

To measure the phase difference between A and R, the following process occurs: Signal, A_1, (Figure 4.5-6) is fed into input #1 of the phase detector, while another signal, R_1, is fed into input #2. The two input signals are applied to the bases of two transistors which are connected in an emitter follower configuration and share a common emitter resistor. The operation of the circuit depends on the emitter following the base voltage of the transistor that is the most positive. As long as one transistor is conducting there will be an output. If both inputs are in phase, the output will be a square wave symmetrical about the zero axis. This signal is integrated by a 200-ohm resistor and a 120-pf capacitor. Because this is a waveform symmetrical about zero, the in-phase pulse will

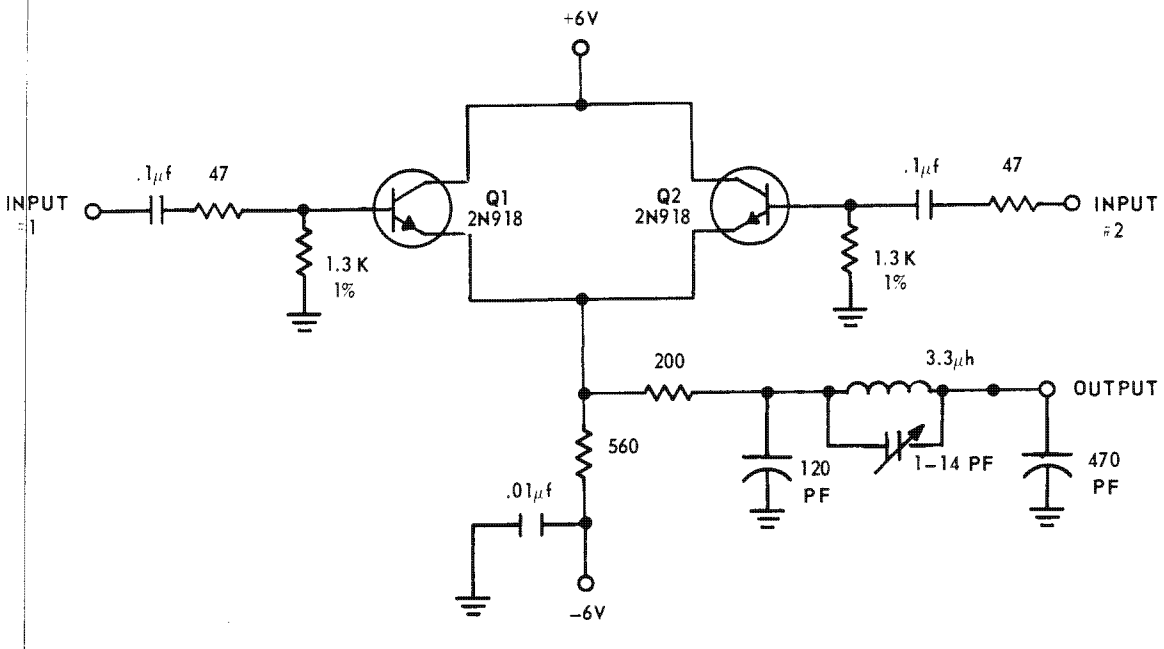

Figure 4.5-6. Phase Detector

integrate to zero. As the phase difference between the two input signals increases, the integrated phase detector output of the two signals increases up to a difference of 180°. At this time, the integrated output starts decreasing and reaches 0 at 360°. This output is called A_1R_1. The process by which the phase difference measurements are achieved in the phase detector is illustrated in Figure 4.5-7. A plot of phase difference A_1R_1 versus output voltage is illustrated in Figure 4.5-8.

Since the output increases with phase difference between 0° and 180° and decreases between 180° and 360°, the response of the phase detector is ambiguous when the phase

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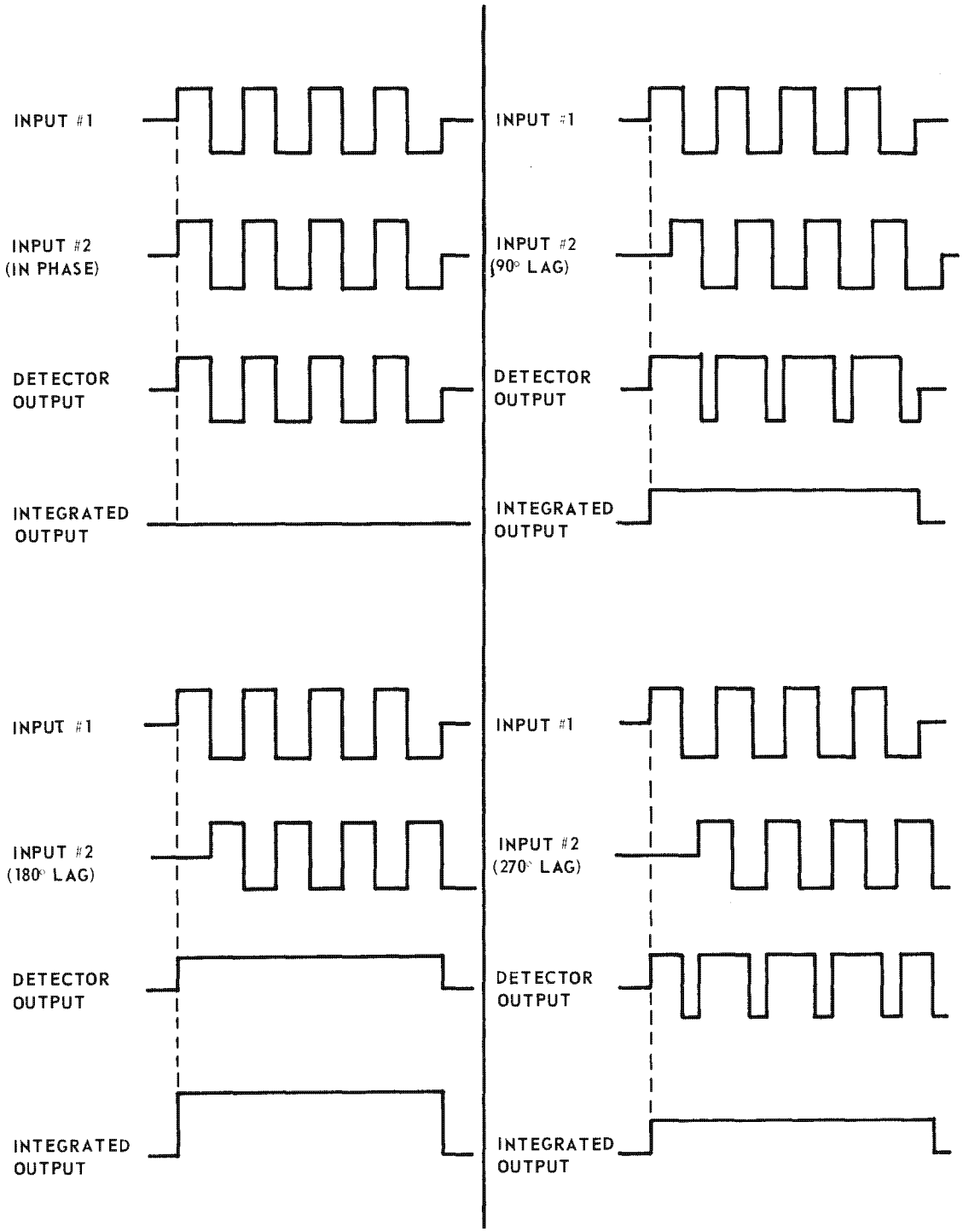

Figure 4.5-7. Phase Detector Timing

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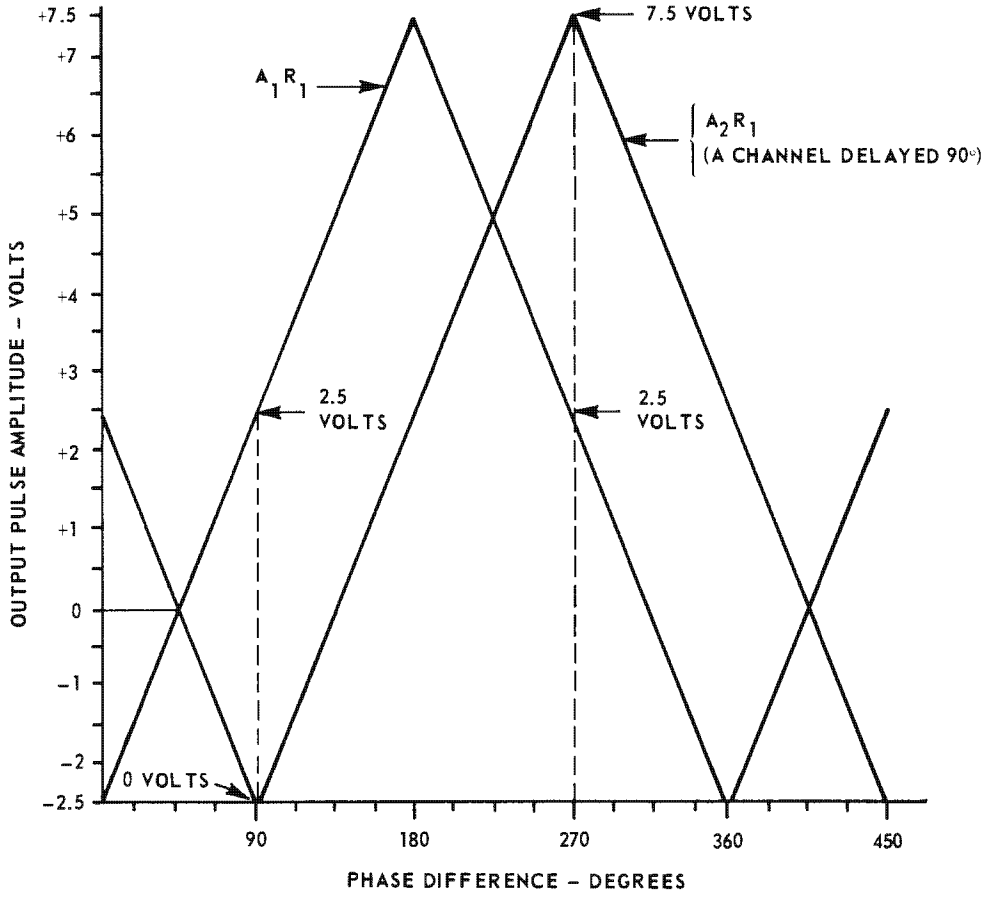

Figure 4.5-8. Phase Detector Response Curve

difference is greater than 180°. To correct this ambiguity and provide phase difference measurements over 360°, one of the reference channel branches is delayed by 90° to produce an input to the second phase detector of A_2. The inputs to this phase detector are R_1 and A_2. Its output follows the phase curve shown in Figure 4.5-8.

An example will be cited here to illustrate how the ambiguity is removed from the phase difference curves. If the signal into channel A is not displaced by 90° from the input to channel R, it is impossible to determine from the

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A_1R_1 output phase curves (Figure 4.5-8) whether this signal phase difference is 90° or 270°. By looking at both curves, A_1R_1 and A_2R_1, it can be seen that at 90° A_1R_1 reads 2.5 volts while A_2R_1 reads -2.5 volts, which distinguishes it from 270°. The latter reads +2.5 volts on A_1R_1 and +7.5 volts on A_2R_1. The data handler phase combiner section uses this principal in decoding 360° of unambiguous phase information.

The following relative phase difference signals are processed and sent to the A/D converter: A_1R_1, A_2R_1, B_1R_1, B_2R_1, R_1D_1, R_2D_1, R_1C_1, and R_2C_1.

4.5.6.2.13 DC Amplifier Module

The DC amplifier is a grounded base linear amplifier that amplifies the integrated output of the phase detector in such a manner that a 0° phase difference represents a predetermined level at its output. At a 180° difference, the output is greater than 8.5 volts for the fine channel (6.25 volts for the coarse channel). The emitter resistor is selected to set the low level point, while the collector resistor is selected to provide the proper volts-per-degree phase slope. Fine phase slope is 18°/volt; coarse phase slope is 28.8°/volt.

4.5.6.2.14 Gate Driver Module

This module is a switching circuit where the load, a phase output gate, is transformer coupled in series with the switching transistor. This circuit provides power to open the two phase output gates in a phase channel. The gate-width

generator in the R/I subassembly furnishes the timing pulse for driving the circuit.

4.5.6.2.15 Sample and Hold No. 1

The input signal to the sample and hold is direct coupled to the DC Amp No. 1 or No. 2. The gate driver triggered by the phase gate pulse serves to open the sample gate for 200 nanoseconds which allows the "hold" capacitors to charge to the gated level.

The first transistor stage in the sample and hold module is a constant current generator which serves to subtract the "pedestal" voltage from the incoming signal.

The sample and hold output circuits serve to present a high impedance to the "hold" capacitor and a low impedance to the commutator gate.

4.5.6.3 Channel B

This channel (Figure 4.5-3) is similar to channel A. The filter of channel B has four outputs, two internal, and two to external connections. One external connection is not used and the other output goes to the signal indicate generator. The two internal outputs are coupled to the 90° phase shifter and a third limiter, the same as in channel A. Therefore, one phase detector has B_1 for an input and the other phase detector has B_2 as an input. Channel R couples a signal into channel B. This signal, after passing through a third limiter, third limiter amplifier, high level amplifier and squaring

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circuit, is coupled to the remaining inputs of the phase detectors. Channel B produces signals known as B_1R_1 and B_2R_1. These signals are amplified, gated and held, and coupled to the A/D converter.

4.5.6.4 Channel R

Channel R (Figure 4.5-3) is the same as channel A, except that the phase filter has three external outputs. The phase filter also has two internal outputs. One of the external outputs is coupled to channel A, another to channel B and the third to channel C. The other two internal signals are coupled to the 90° phase shifter and the third limiter, as in channel A. Therefore, the signal on one input of one phase detector is R_2 and the signal on the input of the second phase detector is R_1. Channel D couples a signal into channel R and travels the same path as the R_1 signal that was coupled into channel A. This signal is coupled to the other input of the phase detectors and is known as D_1. The outputs, R_1D_1 are amplified, gated and coupled to the A/D converter.

4.5.6.5 Summary of Technical Specifications

Pertinent specifications for the IF phase channels (A, B and R) are presented below in Table 4.5-5.

TABLE 4.5-5 IF PHASE CHANNEL SPECIFICATIONS

INPUT POWER			
+6 volt	-6 volt	+8.0 volt	-8.0 volt
+12 volt	+15 volt		

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TABLE 4.5-5 (Cont'd)

INPUT SIGNAL	
Dynamic Range	40 db
Input Level	1.10 mv to 110 mv peak-to-peak
Pulse Width Range	0.4 usec to CW
Recovery Time	less than 5.0 usec
Frequency Confirm Bandpass	20 MHz + 2.0 MHz
Ø Gate Pulse	+6.5V video pulse, 200 ns
OUTPUT SIGNALS	
Phase Output (Channels A, B, R	Amplitude -2.5 to +7.5 volts (Related to Phase Difference)
Output to Log IF	20 MHz Linear 0.008 to 0.8 volt peak-to-peak
Output to SI	20 MC 1.3V peak-to-peak @ Tmin

4.5.7 Intermediate Frequency (IF) Phase Channel (51100)

4.5.7.1 Introduction

This channel is similar to Channel A (51000) except in the internal connection of the phase filter and external connection of the reference 3rd Limiter. The phase filter has two outputs connected externally. One output is connected externally to the SI generator and the other is connected externally to its own reference input.

4.5.7.2 Channel C

Channel C is shown in Figure 4.5-4. The first IF Amplifier has an output coupled to the Log IF subassembly. Channel R couples a signal into channel C and this signal travels the same path as the two internal signals from the

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phase filter in channel A. The same method used in channel A to produce A_2 is used in channel C to produce R_2. Two outputs, R_1C_1 and R_2C_1, are amplified, gated and held and coupled to the A/D converter.

4.5.7.3 Summary of Technical Specifications

Pertinent specifications for the IF Phase Channel C are presented in Table 4.5-6.

TABLE 4.5-6 IF PHASE CHANNEL C SPECIFICATIONS

INPUT POWER			
+6 volt	-6 volt	+8 volt	-8 volt
+12 volt	+15 volt		

INPUT SIGNALS	
Dynamic Range	40 db
Input Level	1.10 mv to 110 mv p-p
Pulse Width Range	0.4 msec to CW
Recovery Time	less than 5.0 usec
Frequency Confirm Bandpass	20 MHz + 2.0 MHz
Ø Gate Pulse	+6.5V video pulse, 200 ns
OUTPUT SIGNALS	
Phase Output	Amplitude -2.5 to +7.5 volts (Related to Phase Difference)
Output to SI	20 MHz, 1.3V p-p @ Tmin
Output to Log IF	20 MHz Linear 0.008 to 0.8 v p-p

4.5.8 IF Frequency Confirm Channel

4.5.8.1 Introduction

There is one frequency confirm channel and it receives its signals from one of the phase antennas. Like the phase channels, it receives its signals thru the signal combiner. The frequency confirm channel performs the following functions over the 40 db dynamic operating range.

(1) Provides reference signals to the R phase channel for input signal phase information.

(2) Provide a video pulse, the amplitude of which is proportional to the IF frequency.

(3) Provide frequency confirm signal.

(4) Provide the signal indicate generator with a signal for SI

4.5.8.2 Channel D

This channel (Refer to Figure 4.5-9) is similar to channel A through the filter circuit. The channel D filter also has four outputs. One external output is coupled to channel R and the other is coupled to the SI generator. Another output is coupled internally to a third limiter, third limiter amplifier, high level amplifier, squaring circuit, and to a phase detector. The fourth output of the filter is coupled to a 37.5 nsec delay line, third limiter, third limiter amplifier, high level amplifier, squaring circuit, and to the

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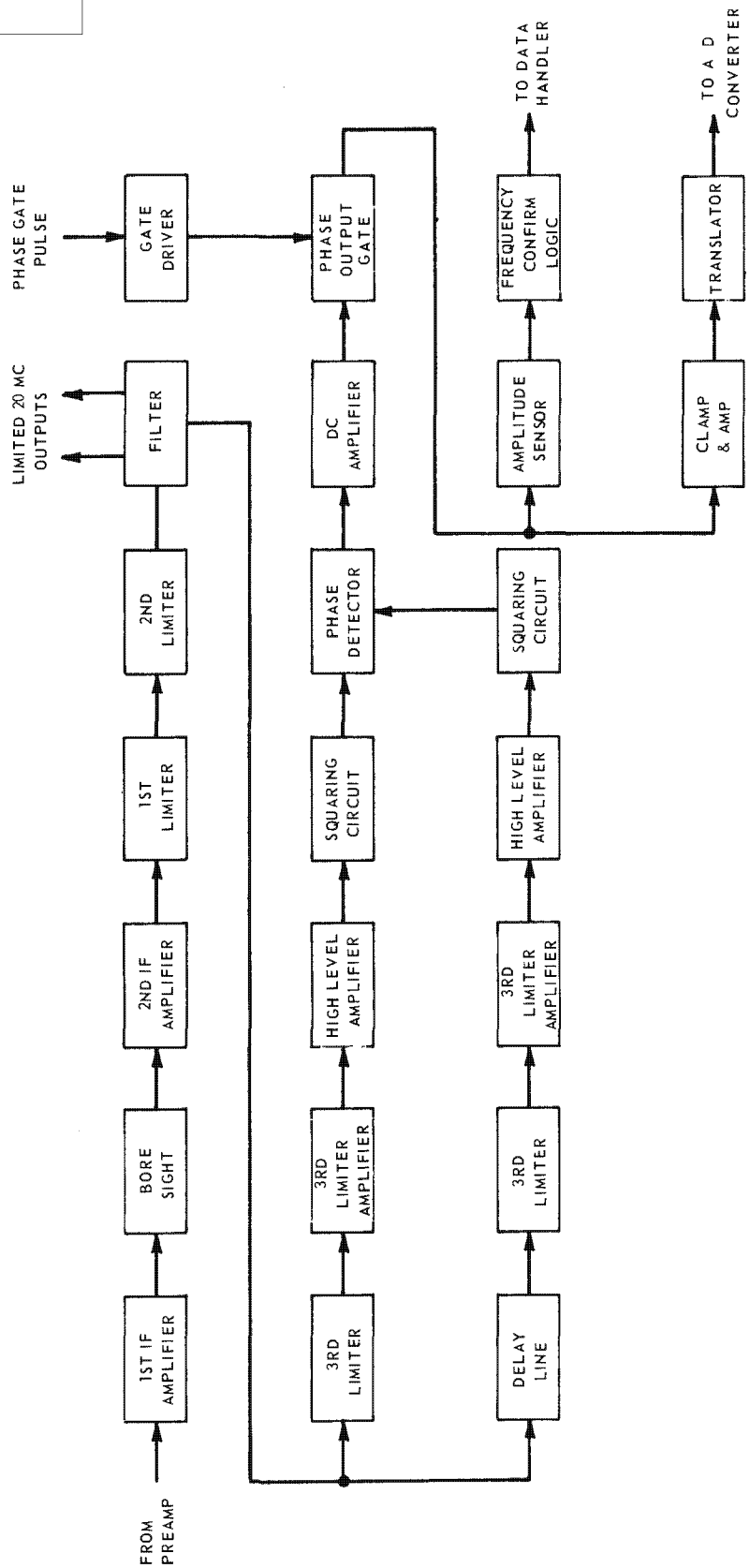

Figure 4.5-9. Frequency Confirm

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phase detector. The fixed delay (37.5 ns) produces a phase delay which is a function of frequency. The phase detector output varies in amplitude as a function of frequency. The output is coupled to a DC amplifier, gated and then coupled to an amplitude sensor module and to a clamp and amplifier module. A plot of the output voltage versus the incoming IF frequency is shown in Figure 4.5-10. The amplitude sensor and

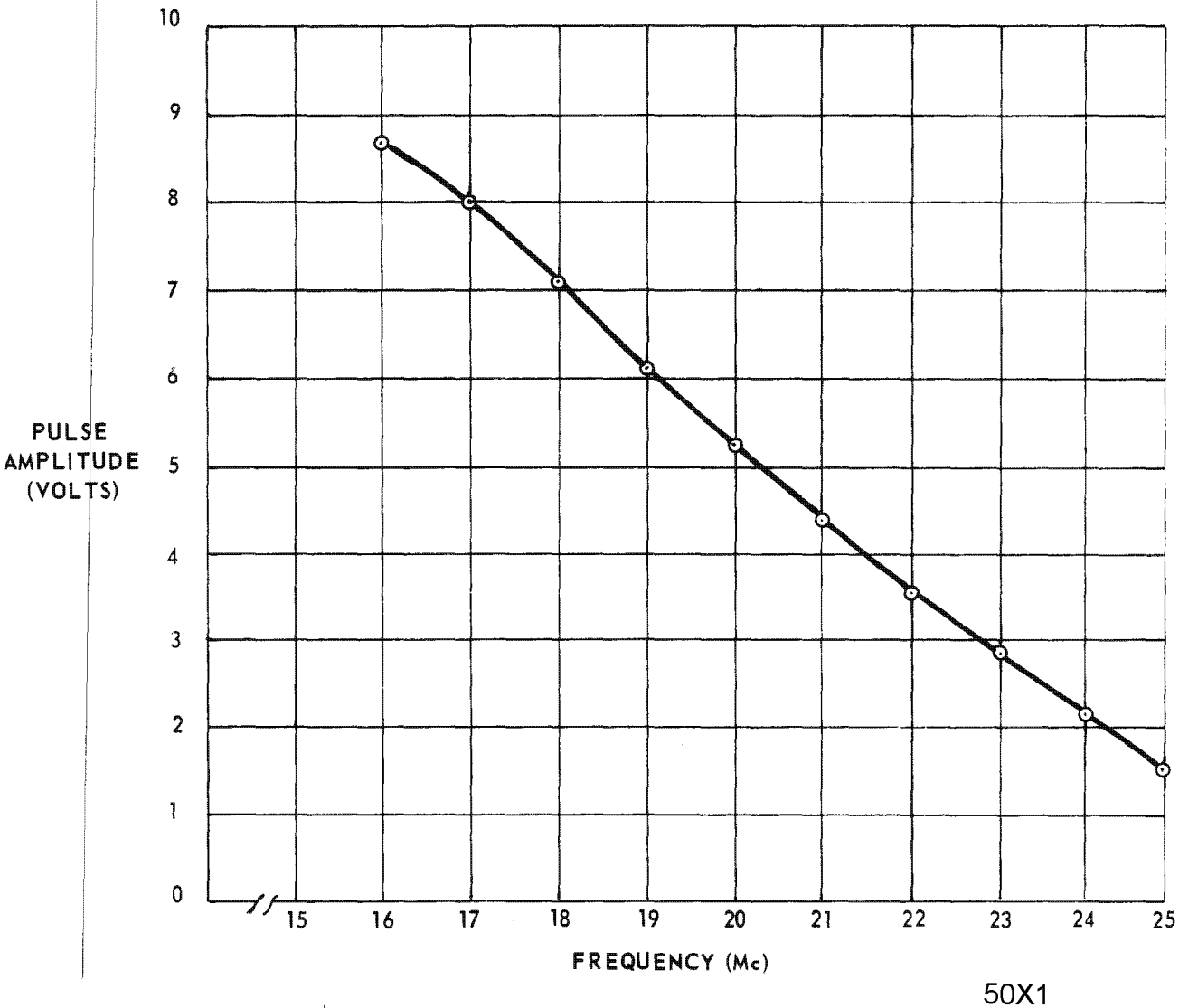

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Figure 4.5-10. Pulse Amplitude vs Frequency

frequency confirm logic modules sense the amplitude of the signal and furnish confirm pulse for those signals from 18.25 ± 25 MHz to 21.75 ± .25 MHz.

4.5.8.2.1 Amplitude Sensor

The gated output of D phase channel is fed directly into the direct coupled amplitude sensor. This circuit is designed to have an output after a certain input threshold voltage is obtained. The threshold voltage (3.6 volts) corresponds to 21.75 MHz. As the input voltage is increased, a point will be reached where the circuit will turn itself off. Turnoff voltage (6.75 volts) corresponds to 18.25 MHz. The circuit will have an output as long as the input voltage ranges between 3.6 and 6.75 volts which indicates to the system that the intermediate frequency is within the proper range.

4.5.8.2.2 Frequency Confirm Logic

This module is driven by the amplitude sensor. Two transistors are connected to generate an enable level

when the IF signal is within frequency-confirm range. The output voltage may range between 2.2 and 3.0 volts. This is sufficient voltage to indicate to the DH that the incoming signal is within tolerance.

4.5.8.2.3 Clamp and Amplifier

The gated output of D phase channel is fed to a clamping amplifier. This circuit is designed to expand the frequency analog voltage from 18 to 22 MHz to a 5.0 volt change to cover the operating range of the A/D. The amplifier is a grounded base linear amplifier.

4.5.8.2.4 Translator

The translator is driven by the clamping and amplifier and is designed to subtract the proper voltage from the amplified frequency analog pulse to present the proper pedestal to the A/D converter.

4.5.8.2.5 Phase Output Gate Module

This module is used only in the frequency-confirm channel. The output from the DC amplifier is gated by a ring diode gate. A gate driver circuit furnishes the power for turning the diodes on so that the frequency analog information can be conducted through the gate and into the darlington emitter follower driver. The gated output starts at approximately 250 nsec after the start of the pulse and lasts for a period of 200 nsec.

4.5.8.3 Summary of Technical Specifications

Pertinent specifications for the IF frequency-confirm channel are presented in Table 4.5-7.

TABLE 4.5-7 FREQUENCY CONFIRM SPECIFICATIONS

INPUT POWER			
+6 volt	-6 volt	+8.0 volt	-8.0 volt
+12 volt	+15 volt		

INPUT SIGNALS	
Dynamic Range	40 db
Input Level	1.10 mv to 110 mv p-p
Pulse Width Range	0.4 usec to CW
Recovery Time	less than 5.0 usec
Frequency Confirm Bandpass	20 MHz $\pm$ 2.0 MHz
Ø Gate Pulse	+6.5V video pulse, 200 ns

OUTPUT SIGNALS	
Frequency Encode Pulse	200 ns pulse, 9.0V Max. (Related to input frequency)
Output to SI	20 MHz, 1.3V p-p @ Tmin
Output to Log IF	20 MHz linear 0.008 to 0.8V p-p
Frequency Confirm Pulse	Amplitude 0 to 3.5 volts (Related to input frequency)

4.5.9 Log IF Amplifier

4.5.9.1 Introduction

The log IF amplifier subassembly (Figure 4.5-11) consists of two identical channels. One channel drives an auxiliary video detector contained within the subassembly.

The purpose of the log IF subassemblies is to convert the linear amplitude information in C, F_1, F_{1S} and F_2

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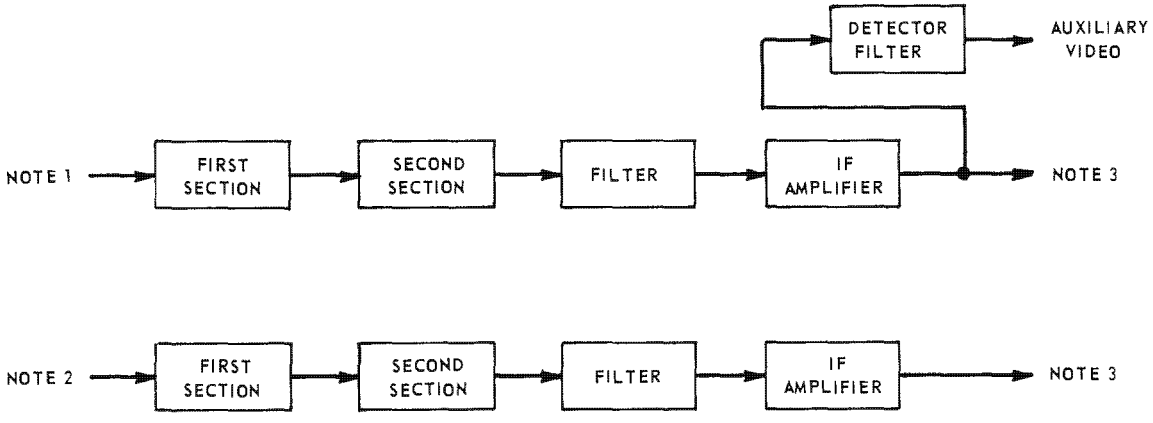
Pre-amps for both high and low band into logarithmic functions, establish the bandwidth of the amplitude channel, feed logarithmic IF signals to the amplitude ratio and pulse width confirm subassembly at the required levels of voltage and impedance, and feed logarithmic IF signals to the Real-Image Logic subassembly. In addition, a video signal proportional to the logarithm of the intercept signal received at the C antenna (high and low) is provided in analog form. The pulse width of the video signal is proportional to the width of the intercepted burst.



NOTE 1 FROM PHASE CHANNEL C FOR HIGH & LOW BAND FOR A/R INFORMATION. FROM HYBRID F_1 FOR HIGH & LOW BAND FOR R/I INFORMATION.

NOTE 2 FROM HYBRID F_2 FOR HIGH & LOW BAND FOR A/R INFORMATION. FROM HYBRID F_{1S} FOR HIGH & LOW BAND FOR R/I INFORMATION.

NOTE 3 TO A/R FOR CHANNEL C & HYBRID F_2 INPUTS. TO R/I FOR HYBRID F_1 & F_{1S} INPUTS.

Figure 4.5-11. Log IF Block Diagram

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4.5.9.2 Discussion of Log Sections

The reverse conductance characteristics of a quantum mechanics device, known as a backward diode, is utilized in the design of the log IF subassembly. The backward diode exhibits a lower voltage drop at a given reverse current than does a conventional diode biased in the forward direction. The reverse conductance characteristics of the backward diode approximate a log function. Moreover, the reverse conductance characteristics of the backward diode are virtually temperature insensitive, having a temperature coefficient of 0.10 mv/°C.

Figure 4.5-12 illustrates the design approach employed in the development of the log IF amplifier. The method is a theoretical and analytical approach, which is used in devising a way to shape the output signal response of the circuit for the purpose of linear output presentation on a monopulse basis at the intermediate frequency. Signal wave shape symmetry is maintained throughout, making the design insensitive to the duty cycle.

The curves of Figure 4.5-12 are derived from the Hoffman 1N3539A backward diode V-I characteristics. The curves shown depict only the positive swing of the CW or pulsed IF applied. Similar curves could be drawn for the negative swing. The inductor across the diodes serves to tune out the diode capacitance at the operating frequency.

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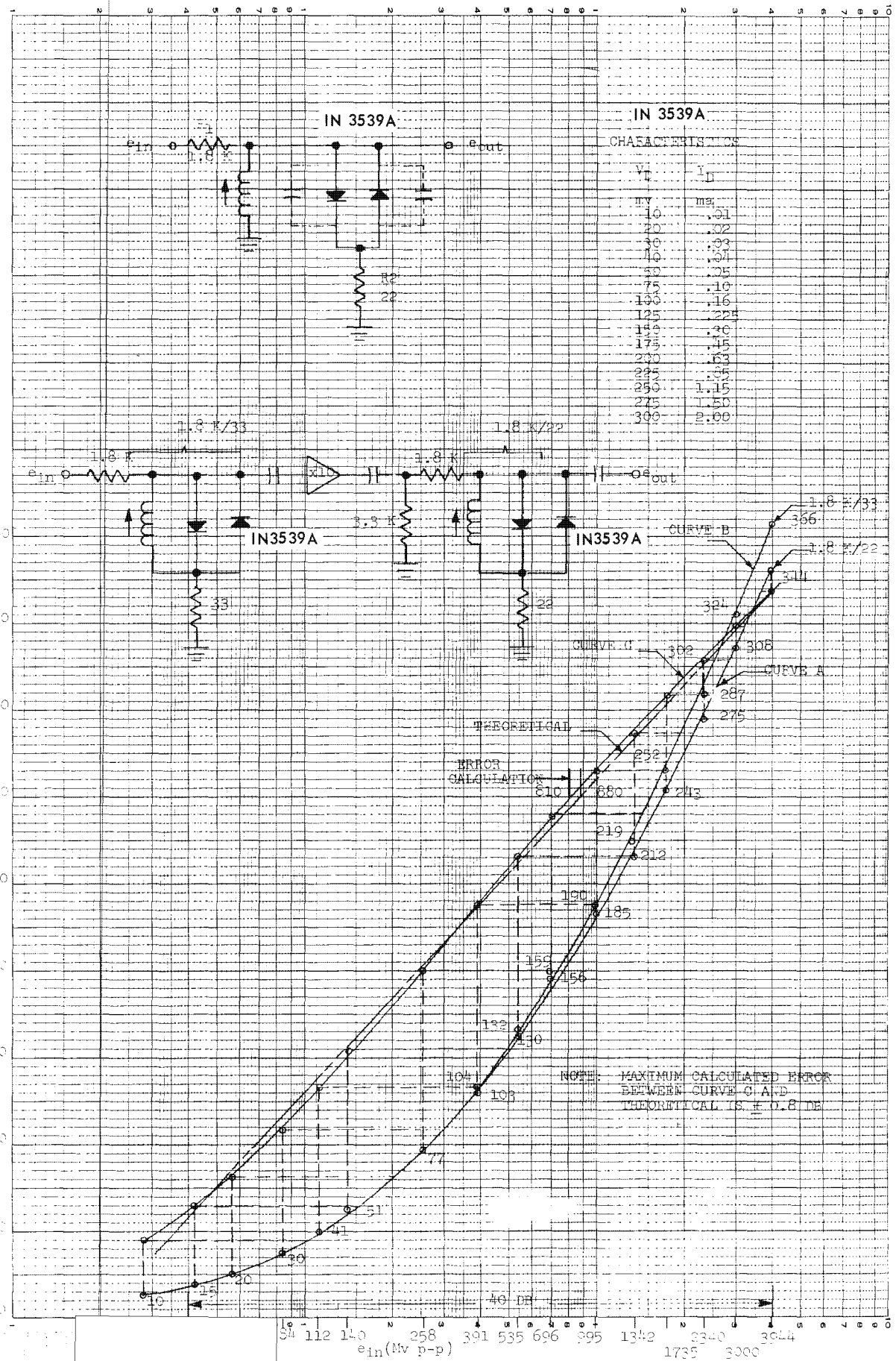

Figure 4.5-12. Log IF Amplifier Design Approach

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The curves are obtained as follows: Curve A is obtained by making e_{in} the dependent variable for different values of V_D and I_D and fixed values of R_1 and R_2. It is also assumed that the diode capacitance offers negligible loading effect when tuned out.

Curve B is obtained the same way as Curve A except that R_2 is changed.

Curve C is obtained by multiplying the ordinate of Curve B by 10 and using these values as e_{in}, then finding a new value of e_o from values of Curve A that correspond to the new values of e_{in}. Follow the following example for a clearer presentation:

EXAMPLE: To calculate one point of Curve C by using Curves A and B:

Since $e_{in} = I_D R_1 + e_o$

$e_o = V_D + I_D R_2$

and $e_{in} = I_D(R_1 + R_2) + V_D$

Take point $e_{in} = 2340$ mv

$e_o = 287$ mv

on Curve B

Multiply e_o by 10 or 287 x 10 - 2870 mv

Find an e_o on Curve A that corresponds to an e_{in} of 2870 mv.

This point corresponds to 302 mw, and in

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turn corresponds to the original e_{in} of 2340 mv.

Figure 4.5-13 is drawn from actual data obtained from one of several log IF amplifiers constructed by the above method. The actual hardware performance closely follows the theoretical predictions, proving the validity of the design approach. Little circuit alignment is necessary; and pairs of amplifiers track well over the dynamic range. In the subassembly, the log IF amplifier is divided into two separate modules, designated first and second log IF section. The output of the second log IF section feeds the log IF filter module.

4.5.9.3 Log IF Filter Module

The log IF filter receives input signals having a dynamic range of 17 db from the logging sections of the subassembly. The filter is of standard flat bandpass Butterworth design having a bandwidth of 8 Mc and a stop band attenuation of greater than 20 db.

The filter serves a two-fold purpose:

(a) It reduces the bandwidth of the signals received by the subassembly from the IF phase channels in order to improve the overall signal-to-noise ratio of the amplitude channel.

(b) Since the frequency confirm information from the frequency confirm channel D is ambiguous

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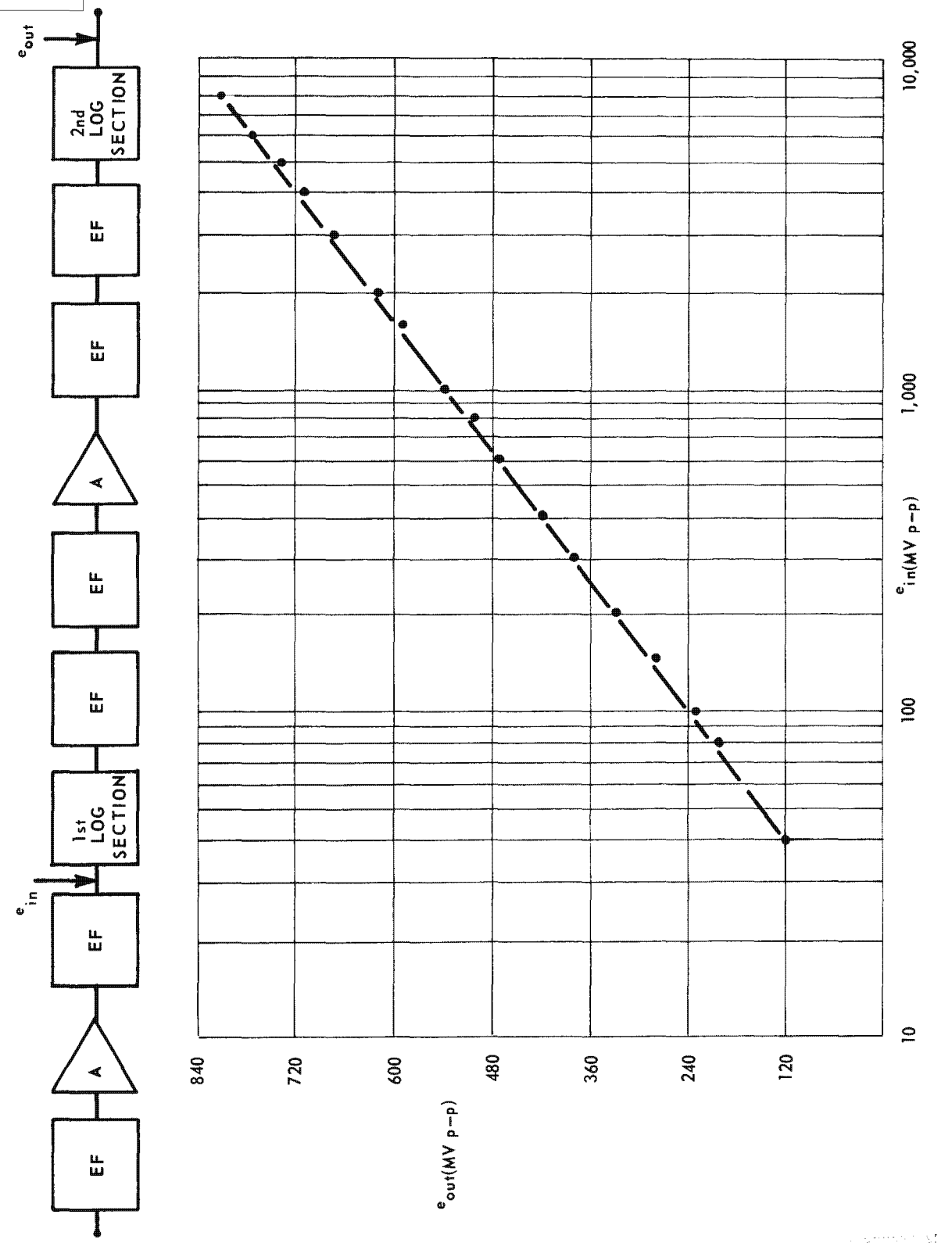

Figure 4.5-13. Log IF Amplifier Characteristics

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when the intermediate frequency is in the vicinity of 6.67, 33.3, and 46 Mc, the stop band attenuation characteristics of the filter assure attenuation of the ambiguous signal to a level such that it appears to be below the Real and Image operation when processed by the R/I subassembly.

The filter output is coupled through an emitter follower to the IF amplifier module.

4.5.9.4 The IF Amplifier Module

The IF amplifier consists of a common base stage driving a low output impedance, high frequency, darlington circuit. The output is coupled with coaxial cable to the A/R subassembly. The channel C IF amplifier module also drives the detector filter.

4.5.9.5 The Detector Filter Module

The detector filter module consists of an isolating emitter follower driving a transistor detector followed by a high cut-off frequency low pass filter. The module detects the C channel signal and provides an output pulse that closely reproduces the envelope of the intercept signal. The output pulse amplitude is proportional to the log of the amplitude of the intercept signal. The detector filter output is coupled through coax cable to the SI generator and also is furnished as an output of the system.

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4.5.9.6 Summary of Technical Specifications

Pertinent electrical specifications are presented in Table 4.5-8.

TABLE 4.5-8 LOG IF AMPLIFIER SPECIFICATIONS

POWER INPUT			
-6 volt	+8.0 volt	+12 volt	+15 volt
INPUT SIGNAL TO EACH CHANNEL:			
Frequency		20 MHz	
Level		+2 to -38 db	
Channel		Terminated in 50 ohm	
OUTPUT SIGNAL			
2 Outputs (to corresponding section of A/R and R/I		20 MHz Bandwidth - 4.5 MHz Level 3.0 volt peak-to-peak (max) Dynamic Range - 17 db	
Detector Filter (to SI Gen. from Channel corresponding to C)		Video Pulse Level 0.6 volts (O-P) (Max) Dynamic Range -17 db Calibration curve furnished with each unit.	

4.5.10 Signal-Indicate Generator

4.5.10.1 Introduction

The signal indicate generator receives four IF signals from phase channels A, B, C and D. An input is also received from channel C routed through the log IF. The data handler also provides three inputs and one input comes from the R/I, thus making a total of nine inputs. There are seven

outputs, two of which go to the amplitude ratio, one to the real and image logic, two to the data handler, one to the recognizer, and one to the TTS #1.

The operation of the SI generator can best be explained by referring to the block diagram 4.5-14. IF signals are received from channels A, B, C and D and fed into their respective limiter amplifiers, the signals are then detected and fed into an adder. The output of the adder is then fed to three amplifiers. The detected signals will add algebraically whereas the noise from the four channels will be an RMS addition. A 6 db signal-to-noise ratio improvement is realized using this technique.

Three of the four video amplifiers and adder amplifiers will be controlled by an SI control module. The other video amplifier and adder will provide a wide open SI (ungated). One of the controlled adders and video amplifiers will provide the normal SI, another provides Tmin, and the third provides the CW SI. The normal SI and CW SI adder and video amplifier coupled to their respective Schmitt triggers and these are in turn fed to the SI OR gate.

When an SI coming out of the SI gate is coupled to the data handler, and it is more than 22.9 microseconds in width, the DH disables the SI. After processing, the SI is enabled. If again a 22.9 microseconds width pulse is measured, the DH will disable the SI until processing is completed. If this process goes on for four times, the indication will be

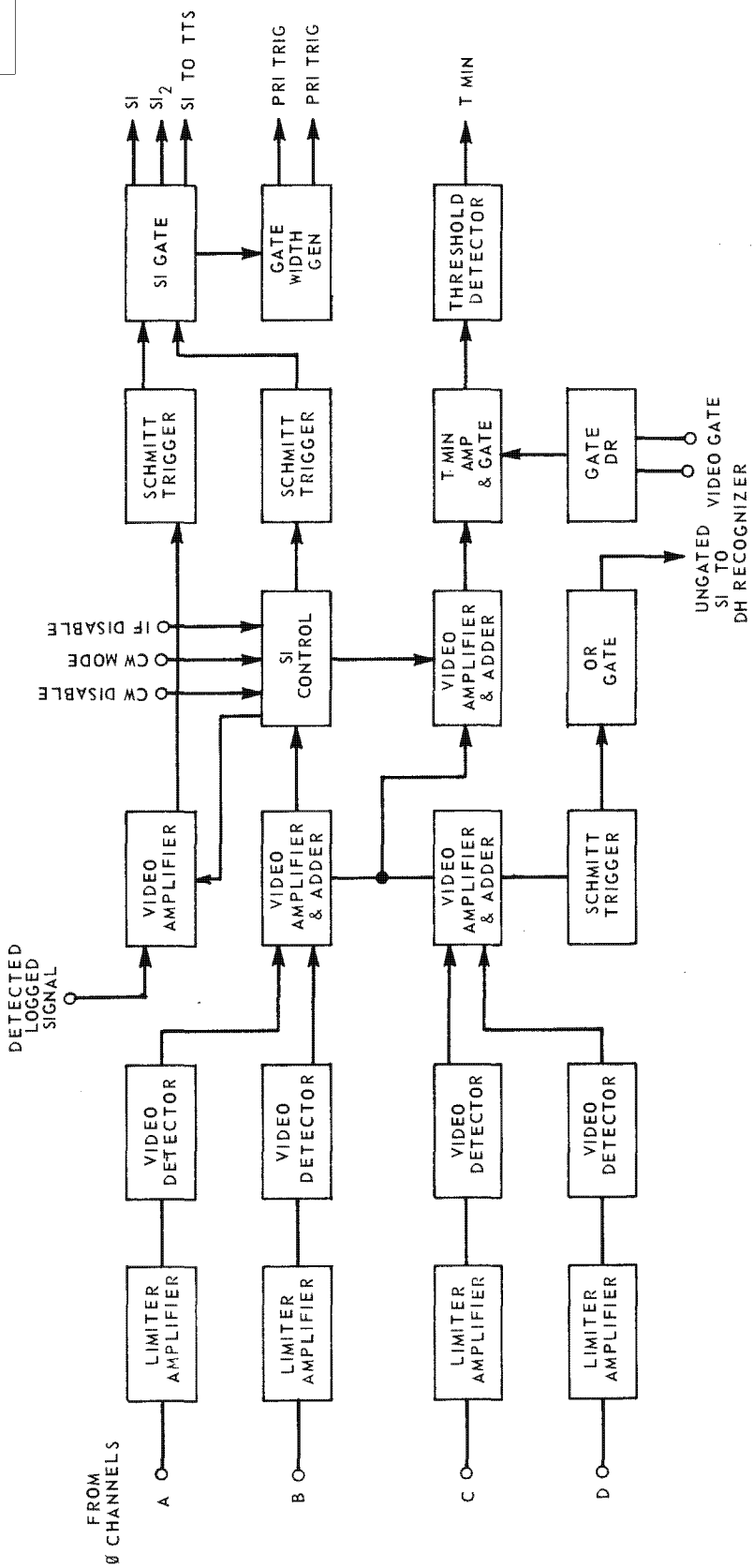

Figure 4.5-14. Signal-Indicate Generator

that CW is present and the CW mode will automatically be energized. The SI control receives three inputs from the data handler. One signal is called IF-disable, another CW-mode, and the third CW-disable. When IF-disable is a logic "1", CW-mode is a logic "0" and CW disable is either logic "1" or "0", the Schmitt trigger impulse will be clamped and no SI normal or CW can appear. A normal SI may appear if IF-disable is a logic "0", CW mode is a logic "0" and CW disable is either logic "1" or "0". If CW disable is a logic "0", CW mode operation is not possible and normal SI operation will be the only mode of operation. CW mode operation is accomplished by capacitively coupling the auxiliary detector logged output through a video amplifier to a Schmitt trigger. The detected CW will be blocked by the capacitor and only pulsed signals 15 db above CW will be able to trigger the Schmitt trigger.

4.5.10.2 Limiter Amplifier Module

An IF signal from a phase channel drives the limiter amplifier. This circuit was designed to have 6-db amplitude limiting. It functions as a linear IF amplifier up to Tmin + 3 db, then it maintains a constant output level of 2.0 volts peak-to-peak. This output drives the video detector.

4.5.10.3 Video Detector

The detector is a standard linear detector circuit using the base-to-emitter diode of a transistor for rectification. The circuit also contains a filter to remove the high

frequency ripple component from the detected wave. Detected output is coupled to an adder and then to a video amplifier.

4.5.10.4 Adder and Video Amplifier

The input of this module is a resistive adder. Signals from four video detectors are coupled into the adder where the corresponding signals and noise are added. The signals are added directly while the noise is added RMS. Therefore, an improved signal-to-noise ratio is the result. The signal is then amplified by a common-base video amplifier. The amplifier has approximately 22.5-db gain with a bandwidth of 8 MHz (at the 3-db points).

4.5.10.5 Schmitt Trigger

This is a commonly used Schmitt Trigger circuit that is triggered by the signal from the video amplifier. An output of 3.2 volts is obtained if the incoming pulse is greater than the triggering level. The output pulse width is proportional to the pulse width of the intercepted pulse. The Schmitt Trigger can be disabled through diode action controlled by the SI control.

4.5.10.6 SI Control

This module consists of three transistor circuits operating as switches and serves to disable the Schmitt Triggers. Refer to Table 4.5-9. The SI disable CW SI are logic signals from the data handler; the CW disable is a

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Table 4.5-9. SI Control Truth Table

TRUTH TABLE				
CW DISABLE	CW SI	IF DISABLE	NORMAL SI	SI IN PRESENCE OF CW
0	0	0	YES	NO
0	0	1	NO	NO
0	1	0	YES	NO
1	1	1	NO	YES

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logic signal from the relays. Logic 1 for CW SI disable is a voltage rise; for CWD, it is an open circuit. Logic 0 is low saturation voltage; for not CWD, it is a short circuit.

4.5.10.7 SI Gate

Two signal-indicate sources are combined in the SI gate to drive a darlington, low output impedance stage. One output, called SI_1, is sent to the data handler where the PW and PRI are measured. The data handler also uses this signal to start its programming sequences. Another output, called SI_2, is sent to the amplitude ratio subassembly for pulse width confirm measurements. A third output drives the gate width generator. Finally, another is used to generate the tag pulse in the TTS converter.

4.5.10.8 Gate Width Generator

This circuit consists of a 800-nsec monostable multivibrator. The output pulse is used to drive the gate width generators in the Real and Image subassembly and the dual gate driver in the amplitude ratio subassembly. This signal has been termed the primary trigger because it is the beginning of the gating operations for the IF assembly.

4.5.10.9 OR Gate

The OR Gate is similar to the SI Gate and is used to interface with the DH Recognizer Unit. The signal input is fed from a Schmitt Trigger not controlled by the SI control. The output is labeled the "ungated SI."

4.5.10.10 Tmin Amplifier and Gate

This module consists of a video amplifier and a ring diode gate. Its input from the video amp and adder is controlled by the SI control module to allow normal operation when CW is present and the DH is sampling four times. After CW operation is energized, Tmin confirm is not required.

4.5.10.12 Gate Driver

This module is the same as used in the phase channel described in paragraph 4.5.6.2.14.

4.5.10.13 Tmin Threshold

This module is made up of a level detector stage and a darlington stage. The output interfaces with the DH.

4.5.10.14 Summary of Technical Specifications

A summary of pertinent electrical specifications is presented in Table 4.5-10.

TABLE 4.5-10. SI GENERATOR SPECIFICATIONS

POWER INPUT				
-6 volt	+6 volt	+8 volt	-8 volt	+12 volt
INPUT SIGNAL				
a) IF Channel A-D		20 MHz with limiting occurring at Tmin + 6 db		
b) A/R		Pulsed 20 MHz - Logged		
c) Data Handler		4.75 $\pm$ .5V		
1) IFD		Volt logic level		
2) CWSI		Volt logic level -4.75 $\pm$ .5V		

TABLE 4.5-10. SI GENERATOR SPECIFICATIONS

Relay CWD	Open logic "1"
OUTPUT SIGNAL	
Primary Trigger	Video pulse 10 V 0-P 800-nsec wide
SI_1	3.5 ± 0.5 volt level with PW information
SI_2	Same as SI_1 but sets on a 0.7 V level
SI to TTS	Same as SI_2
Tmin	Video pulse 3.5 ± 5V, 200 nsec wide

4.5.11 Amplitude Ratio and Pulse Width Confirm Subassembly

4.5.11.1 Introduction

The amplitude ratio and pulse width confirm subassembly (A/R) (Figure 4.5-15) provides three bits of information for the data handler (DH) and sends one channel of information to the analog-to-digital converter (A/D).

A video signal whose amplitude varies directly as the log of the amplitude of the intercept burst at the C antenna is processed in the A/R and fed to the A/D for encoding.

Amplitude ratio measurements are accomplished by gating, detecting, and amplifying the C and F_2 logged IF signals. Outputs from the two branches are directed into a comparator circuit. A pulse, the amplitude of which is proportional to the difference between C and F_2 amplitude, is developed at the comparator's output. This difference pulse is amplified, and when the amplitude ratio of F_2 with respect

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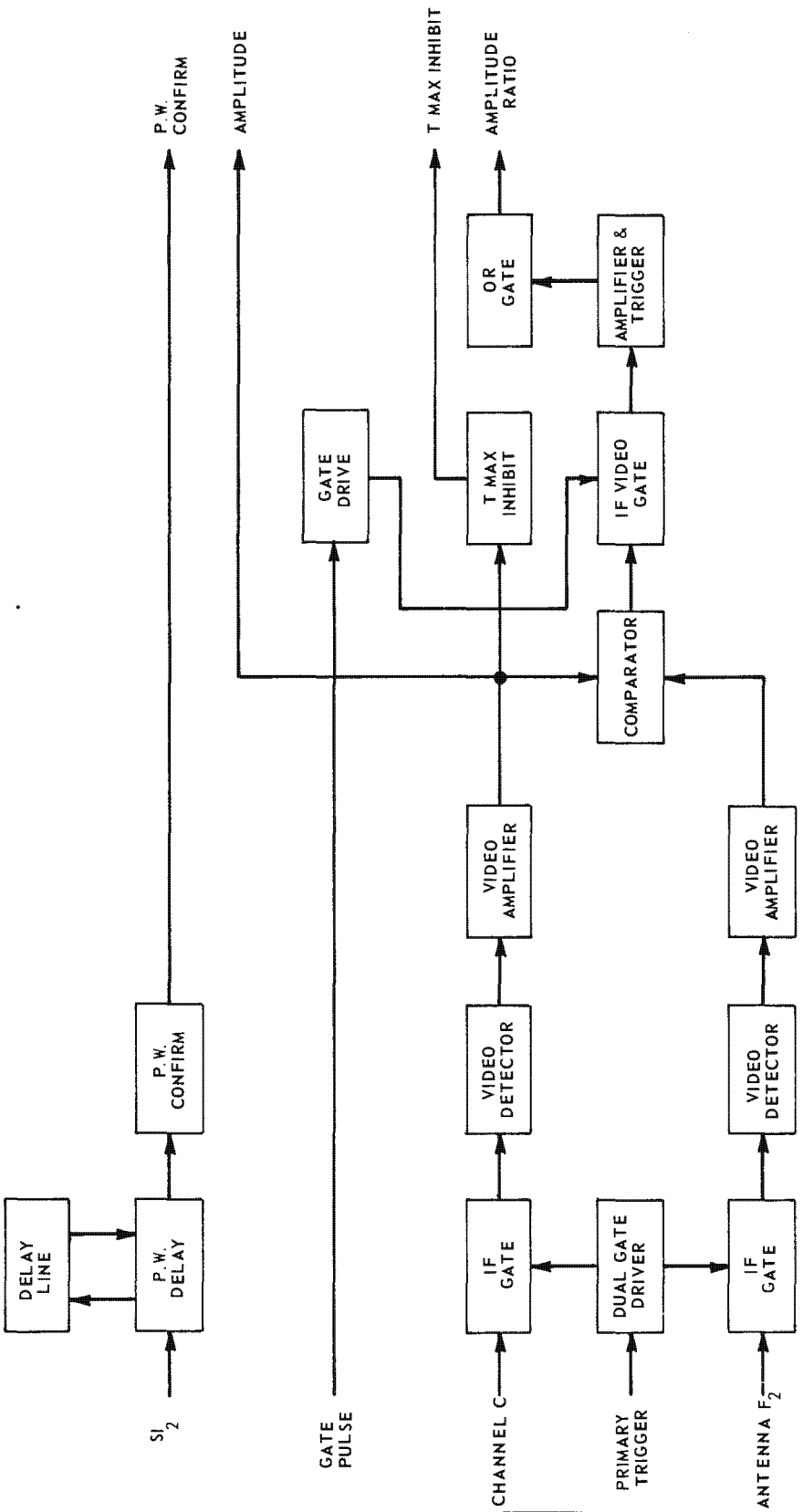

Figure 4.5-15. A/R and P-W Confirm Block Diagram

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to C is equal to or greater than 1.5 db, it triggers a Schmitt trigger. The Schmitt trigger output is coupled through an OR gate to the DH.

An inhibit signal derived from the C channel amplitude information is generated when the incoming signal strength is greater than the maximum signal that the system is designed to process. The inhibit pulse is coupled to the DH. This is the Tmax inhibit signal.

A confirm signal is generated whtn the width of the incoming intercept burst is sufficient for the system to process the intercept signal with accuracy. The circuit is driven from the signal-indicate generator subassembly and provides information for the DH.

In order to minimize the recovery time and maximize the duty cycle handling capabilities of the system, an IF analog gating technique is employed in the amplitude ratio subassembly. The first 800 nsec of an intercept signal, fed from the log IF subassembly, is allowed to pass through the C channel and F_2 channel IF gates. After the 800 nsec period, the gates are closed and the remainder of the intercept pulse (if any) is not allowed to pass to the C channel and F_2 channel video detectors.

The video detectors, video amplifiers, and associated circuits following the IF gates have a total recovery time of approximately 5 usec. Therefore, should the incoming

signal have a width of 500 nsec, the amplitude channel can accurately process this signal if its duty cycle is no higher than ten percent. However, if the signal pulse width is, for example, 600 usec, then the subassembly can process accurately this incoming signal if its duty cycle is as high as 99 percent.

In the following sections, the individual functional elements of the subassembly are discussed as to their intent and mechanics of operation. Since both C channel and F_2 channel sides of the amplitude ratio subassembly are identical up to the output of the video amplifiers, only one branch is described.

4.5.11.2 IF Gate

In the IF gate circuit, two transistors are connected in a series arrangement to provide a high impedance to an incoming signal when the gate is turned off and a low impedance when the gate is turned on. A signal is received from the log IF, gated, and the gated portion is coupled to a video detector.

4.5.11.3 Dual Gate Driver

A dual gate driver is employed to open the IF gates. This is the same type of gate driver used to open video gates in the IF phase channel. Two separate gate drivers, driven from the same primary trigger input, are used instead of one gate driver having two secondary windings. This arrangement is necessary to avoid IF cross-coupling in

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the common transformer and, hence, IF cross-talk between the two channels. The positive-going, 10-volt primary trigger pulse turns both transistors on in the dual gate-driver and develops a +1.2-volt pulse at the secondary of each transformer when loaded into the IF gates. One gate driver drives an IF gate in C channel, at the same time the other one is driving an IF gate in F_2 channel.

4.5.11.4 Video Detector

The received gated IF pulse is detected in the base-emitter diode section of a 2N918. Detection is achieved by biasing the transistor to act as a Class B amplifier. The rectified signal is picked off the emitter and fed into a low pass filter. An IF trap is placed in series with the low pass filter in order to obtain additional attenuation of the 20 MHz component of the detected signal. The detected video pulse is ready to be amplified.

4.5.11.5 Video Amplifier

The video pulse is amplified in the video amplifier module. The gain of the amplifier is adjusted such that a 40-db change in the RF assembly input level will produce a 5-volt change in the output video amplifier.

The amplifier consists of an emitter follower driving a common base amplifier. The amplifier in turn feeds a darlington circuit output stage. A pick-off point in the darlington circuit is used to drive a feedback amplifier.

The feedback amplifier is biased such that it will be driven to cut off by a signal having an amplitude of Tmin or greater. In other words, any signal within the dynamic range of the receiver will cause a constant amplitude negative going pulse to appear at the collector of the feedback amplifier transistor. The signal from the collector of the feedback amplifier is capacitive coupled to the base of the common base amplifier. This signal is reamplified through the stage and results in a positive offset voltage being added to the original signal. The function of the feedback amplifier circuit is twofold:

(1) It provides a means of adjustments so that the video amplifier's five (5) volt output range can be set to start at approximately one (1) volt.

(2) By varying the level of the feedback pulse, with temperature sensitive elements in the bias network of the feedback amplifiers, a method of temperature compensation is provided such that the overall gain of the video amplifier is held constant over the prescribed temperature range.

4.5.11.6 Comparator

The signals from antenna C and F_2 after being amplified provide the input signals to the comparator. The circuit compares the amplitude of the video signals from the

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C and F_2 antennas and delivers an output pulse having an amplitude proportional to the absolute difference between the signals being compared.

4.5.11.7 IV Video Gate

The comparator output is sampled in a diode analog sample gate. The sample gate is turned on, by a pulse from the gate driver, for approximately 110 nsec.

The 110 nsec amplitude ratio sample pulse is capacitively coupled to the amplifier and trigger.

4.5.11.8 Amplifier and Trigger

A common base amplifier amplifies the gated amplitude ratio video pulse. Adjustments are made in initial bench tests to set the gain of this amplifier such that its output will be sufficient to trigger a Schmitt trigger when the amplitude of F_2 is 1.5 db greater than the amplitude of the C channel. Two transistors plus associated components make up the Schmitt trigger. It is designed to have a high gain and low hysteresis in order to minimize the decision range of the circuit. The Schmitt trigger is isolated from the OR gate by an emitter follower circuit.

4.5.11.9 OR Gate

The same type as mentioned in 4.5.12.12.

4.5.11.10 Gate Driver

Another gate driver circuit is used to open and close an IF video gate in the amplitude ratio and Tmin section

of the subassembly. Only one transformer is required since it switches video signals which are not affected by cross talk. A positive 150-nsec gate pulse is coupled to this module output by coaxial cable from the Real and Image subassembly.

4.5.11.11 Tmax Inhibit

The Tmax circuit is designed to produce an inhibit signal when the logged amplitude pulse it receives from the C video amplifier indicates that the level of the intercept pulse is above the dynamic range of the receiver. This function is accomplished by feeding the C video amplifier output to a threshold device which turns on when the intercept pulse level is above Tmax. The threshold is followed by a saturation amplifier which drives an emitter follower output to the DH.

4.5.11.12 Pulse Width Delay

SI_2 is coupled from the signal-indicate generator to the input of this module. The incoming pulse drives an emitter follower which is coupled to the delay line module and also to an AND gate in the pulse width confirm module. Bias for this circuit is obtained from the DC component in SI_2.

Also included within this module is another emitter follower. This circuit receives its input from the output of the delay line which connects to the pulse width confirm AND gate.

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4.5.11.13 Delay Line

This is a module which contains several delay lines connected in series to make a total delay of 0.4 usec. Both the input and output of this module terminate in the gate width delay module.

4.5.11.14 Pulse Width Confirm

Inputs to this module are received from the pulse width delay module. The circuitry in this module is basically a logic AND gate, amplifier, and emitter follower output stage. A video pulse must be present on both inputs before the AND will produce an output. This output is amplified in a saturation amplifier such that it will produce a 3-volt video output pulse at the output of the emitter follower. This output is sent to the data handler to confirm that the intercepted pulse width is equal to or greater than 0.4 usec.

4.5.11.15 Summary of Technical Specifications

Pertinent electrical specifications are presented in Table 4.5-11.

4.5.12 Real and Image Logic Subassembly

4.5.12.1 Introduction

The Real and Image subassembly has two basic independent operations to perform.

1) Gating signals are generated in this unit for gating the signals in the IF assembly.
2) A confirm pulse is sent to the DH when a real

TABLE 4.5-11 A/R AND PW CONFIRM SPECIFICATIONS

POWER INPUT	
+6 volt -6 volt +12 volt +8.0 volt -8.0 volt	
INPUT SIGNALS	
C and F_2 (From Log IF)	20 MHz Level (Max) 3.0 VP-P Dynamic Range - 17 db
SI (From Signal Indicate Gen)	Video Pulse Level 3.5 ± 0.5 volt (0 to P)
Gate Pulse (From Real/Image)	Video Pulse Pulse Width 100 nsec
Primary Trigger (From Signal Indicate Generator)	Video Pulse Level 10V (0 to P) Pulse Width 800 nsec
OUTPUT SIGNALS	
PW Confirm (To DH)	Video Pulse Level - 3.5 ± .5 V (0 - P)
Amplitude (To A/D Converter)	Video Pulse Level - 6.0 Volt (0 - P) Max. Dynamic Range - 17 db Pulse Width - 600 nsec Max.
Amplitude Ratio (Inhibit to TTS)	Video Pulse Level - 3.5 ± .5 V (0 - P)
Amplitude Ratio (To DH)	Video Pulse Level - 3.5 ± 0.5 volt (0 - P)
Tmax Inhibit to DH	Video Pulse Level - 3.5 ± 0.5 V (0 - P)

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signal is received and when a real-or-image signal is received.

These operations are illustrated in the Real and Image Logic Block Diagram, Figure 4.5-16

Accurate pulse amplitude measurements are essential in this system. In an actual operation the pulse amplitude is not a constant height at all times within the pulse period. Therefore, a method has been derived to measure the amplitude of the pulse at a predetermined time within the pulse period where the amplitude information is reliable. The method used is a type of sample gating. The gating time was chosen to be in a region where the desired pulse amplitude is present. This time was chosen so that rise and fall time effects would not affect the measurement.

All signals sent to the data handler or the analog to digital converter are gated outputs. Gating is initiated by the primary trigger pulse generated in the signal-indicate generator.

4.5.12.3 Gate Delays

A gate delay places the gating time to the proper position within the information pulse. This circuit integrates the input pulse into a ramp. When the ramp reaches a certain predetermined level it drives a saturation amplifier into saturation. This output is a rectangular pulse whose width is approximately the length of time taken from the firing point

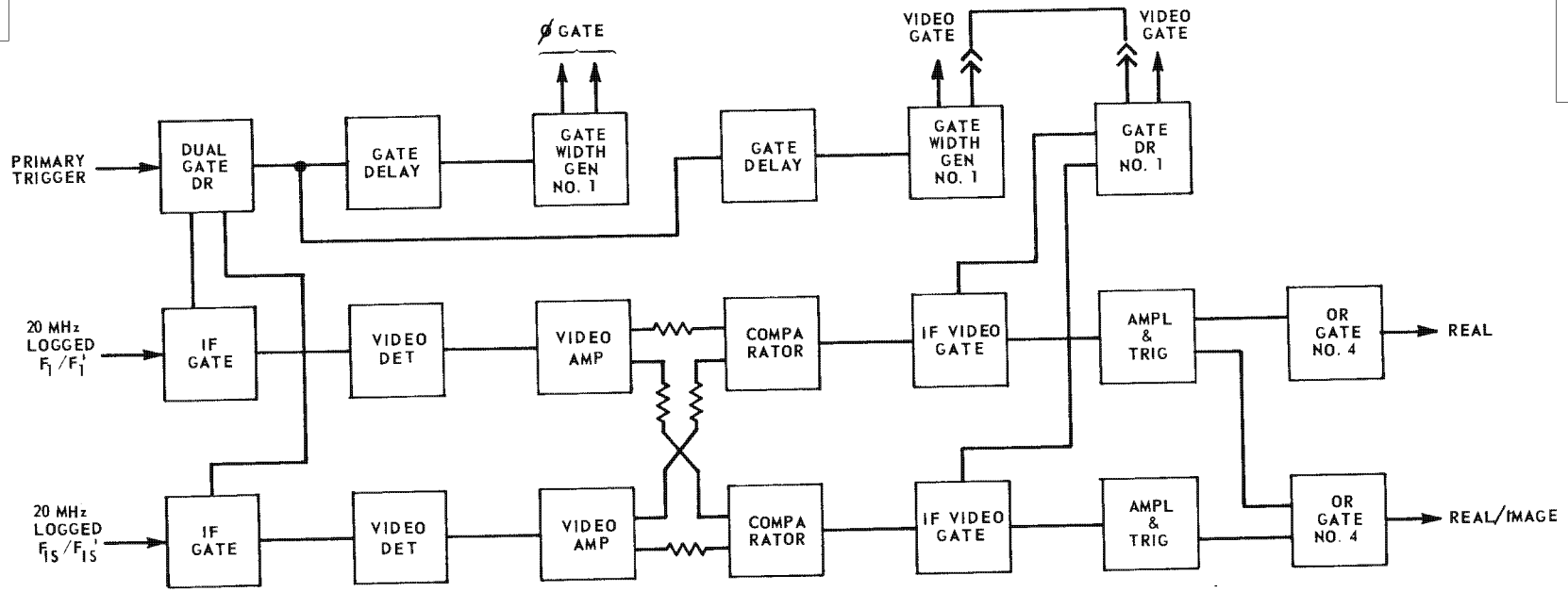

Figure 4.5-16. Real-Image Logic Block Diagram

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to the trailing edge of the incoming pulse. Because the shapes of the different output pulses to be gated are different, it is necessary to time the gating time for each output individually.

One gate delay is adjusted to have a delay of 130 nsec with respect to the primary trigger, and it drives the gate-width generator for the phase gate pulse.

Another gate delay is adjusted to have a delay of 250 nsec with respect to the primary trigger and it drives the gate width generator for the video gate pulse.

4.5.12.4 Gate Width Generator

This circuit is a one-shot multivibrator. The one-shot is triggered by a gate delay circuit and is designed to have an output of 10 volts and a predetermined pulse width. Each circuit has a different pulse-width because of the different requirements placed upon the gated outputs.

The Ø Gate gate-width generator is adjusted to have a pulse width of 200 nsec. Its output feeds the gate drivers in the IF phase channels and in the A/D converter. The video gate gate-width-generator is adjusted to have a pulse width of 110 nsec. Its output feeds the Tmin amplifier and gate in the SI module and the A/R and R/I video gates.

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4.5.12.5 IF Gate

In the IF gate circuit, two transistors are connected in series arrangement to provide a high impedance to an incoming signal when the gate is turned off and a low impedance when the gate is turned on. A signal is received from the log IF, gated, and the gated portion is coupled to a video detector.

4.5.12.6 Dual Gate Driver

A dual gate driver is employed to open the IF gates. This is the same type of gate driver used to open the video gates in the IF phase channel. Two separate gate drivers, driven from the same primary trigger input, are used instead of one gate driver having two secondary windings. This arrangement is necessary to avoid IF cross coupling in the common transformer and, hence, IF cross-talk between the two channels. The positive going 10-volt primary trigger pulse turns on both transistors in the dual gate driver and develops a +1.2 volt pulse at the secondary of each transformer when loaded into the IF gates. One gate driver drives an IF gate for the F_1 antenna signal unshifted and the other IF gate is used for the shifted signal from the F_1 antenna.

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4.5.12.7 Video Detector

The received gated IF pulse is detected in the base-emitter diode section of a 2N918. Detection is achieved by biasing the transistor to act as a Class B amplifier. The rectified signal is picked off the emitter and fed into a low pass filter. An IF trap is placed in series with the low pass filter in order to obtain additional attenuation of the 20MHz component of the detected signal. The detected video pulse is ready to be amplified.

4.5.12.8 Video Amplifier

The video pulse is amplified in the video amplifier module. The gain of the amplifier is adjusted such that a 40-db change in the RF assembly input level will produce a 5-volt change in the output video amplifier.

The amplifier consists of an emitter follower driving a common base amplifier. The amplifier in turn feeds a darlington circuit output stage. A pick-off point in the darlington circuit is used to drive a feedback amplifier. The feedback amplifier is biased such that it will be driven to cut off by a signal having an amplitude of Tmin or greater. In other words, any signal within the dynamic range of the receiver will cause a constant amplitude negative going pulse to appear at the collector of the feedback amplifier transistor. The signal from the collector of the feedback amplifier is capacitive coupled to the base of the common base

amplifier. This signal is reamplified through the stage and results in a positive offset voltage being added to the original signal. The function of the feedback amplifier circuit is twofold:

(1) It provides a means of adjustments so that the video amplifier's five (5) volt output range can be set to start at approximately one (1) volt.

(2) By varying the level of the feedback pulse, with temperature sensitive elements in the bias network of the feedback amplifiers, a method of temperature compensation is provided such that the overall gain of the video amplifier is held constant over the prescribed temperature range.

4.5.12.9 Comparator

The signals from Antenna F_1 and F_{1s} after being amplified by the video amplifiers provide the input signals to the comparator. The circuit compares the amplitude of the video signals from the F_1 and F_{1s} antennas and delivers an output pulse having an amplitude proportional to the absolute difference between the signals being compared. Since the signals are logarithmic, the difference between the signals will produce a constant output level through the dynamic range if the signals differ by a constant value throughout the range.

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4.5.12.10 IF Video Gate

The comparator output is sampled in a diode analog sample gate. The sample gate is turned on, by a pulse from the gate driver, for approximately 110 nsec.

The 110 nsec amplitude ratio sample pulse is capacitively coupled to the amplifier and trigger.

4.5.12.11 Amplifier and Trigger

A common-base amplifier amplifies the gated amplitude-ratio video pulse. Adjustments are made in initial bench tests to set the gain of this amplifier such that its output will be sufficient to trigger a Schmitt trigger when the amplitude of F_1 is 2 db greater than F_{1s}. Two transistors plus associated components make up the Schmitt trigger. It is designed to have a high gain and low hysteresis in order to minimize the decision range of the circuit. The Schmitt trigger is isolated from the OR gate by an emitter follower circuit.

4.5.12.12 OR Gate

Outputs of two Schmitt Triggers are connected to an OR gate for the Real or Image confirm. A pulse from either one or both Schmitt triggers will produce an output pulse of the same width and having an amplitude of 0.9 times that of the input. The J11 output from this module is called a Real-Image confirm. This output is coupled to the data handler to indicate that there is a signal being detected that is

desired, and that processing should be continued.

4.5.12.13 Gate Driver

Basically this is a switching circuit where the load, which is the IF video gates are transformer-coupled with the switching transistor. This circuit provides the power to open the gates when a video gate pulse is received. Two gates can be driven from the two secondary windings in the transformer.

4.5.12.14 Summary of Technical Specifications

Pertinent electrical specifications are presented in Table 4.5-12.

TABLE 4.5-12. REAL-IMAGE LOGIC SPECIFICATION

INPUT POWER		
+6 volt	-6 volt	+12 volt	+8 volt	-8 volt
INPUT SIGNALS		
F_1		20 MHz
F_{1s} (from Log if A33)		3.5 volts p-p at Tmax
Primary Trigger		Video Pulse Level 10.0 volt (0-P) P.W. 800 nsec
OUTPUT SIGNAL		
Real confirm or Image confirm (to Data Handler)		3.5 v $\pm$ .5 (100 nsec)
Gate Pulse (to Amp. Ratio and SI Generator)		Video Pulse Level 7.5 volt (0-P) P.W. 150 nsec
Phase Gate Pulse (to all phase channels and A/D)		Video Pulse Level 6.5 volt (0-P) P.W. 220 nsec

4.5.13 Tone Tag Signal (TTS) Subassembly

4.5.13.1 Introduction

The TTS performs the following functions:

(1) Provides a predetected video signal no greater than 0.7-volt p-p through 40 db in the dynamic operating range.

(2) Provide the predetected signal with a 3 db pass band from 0.5 to 5.5 MHz with the center of the predetected pass band corresponding to the center of the phase channel pass band (20 MHz).

(3) Provide an adjustable gain on command from the data handler in three 10-db power steps, so that the signal anywhere in the dynamic range is made to fall in the 0.19-volt p-p to 0.6-volt p-p range. In the absence of a command the gain is at the most sensitive step.

(4) Provide two reference tones; one at 6 MHz ±5 KHz and one at 46.875 KHz ±100 Hz, with adjustable amplitudes.

(5) A tag pulse when the emitter being received is inside of the A/R circle.

Refer to Figure 4.5-17 for the following modular breakdown description.

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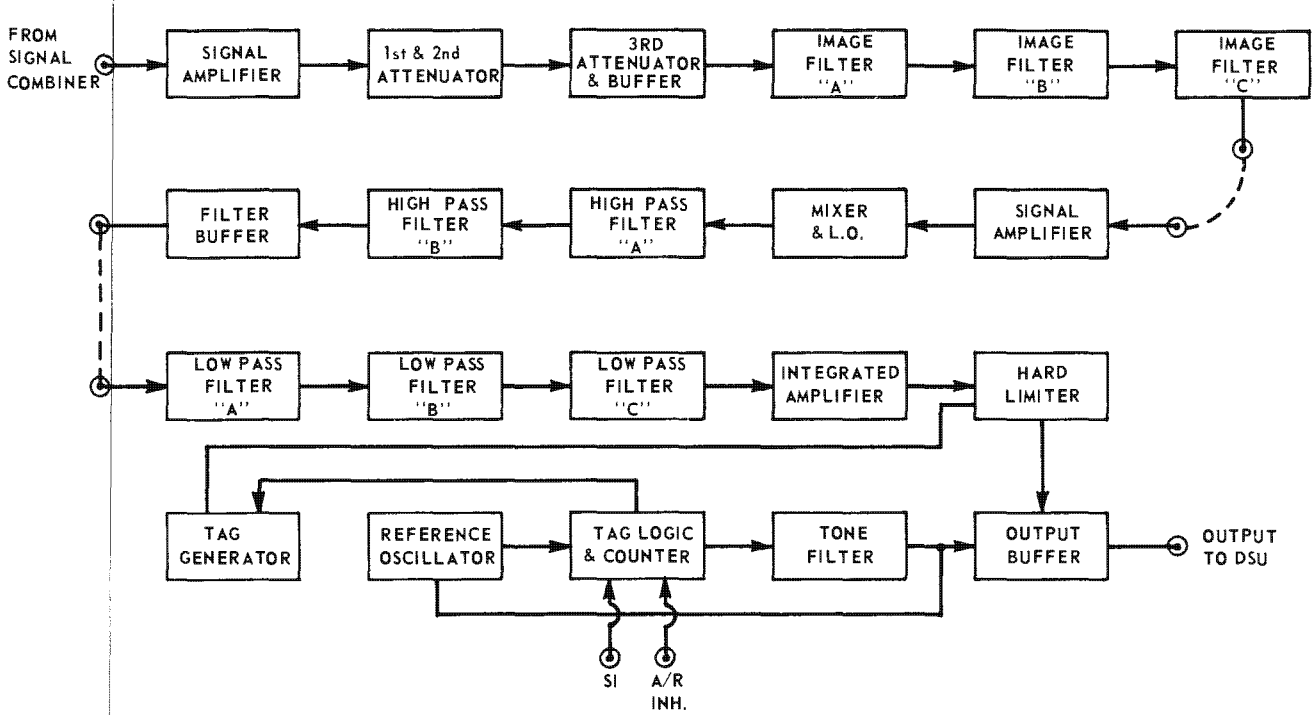

Figure 4.5-17. TTS Converter Block Diagram

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4.5.13.2 Signal Amplifier

The signal amplifier is a wide-band grounded-base amplifier with a peaking coil to compensate the frequency response of the attenuator circuit stages that follow. Amplify gain is approximately 20 db.

4.5.13.3 First and Second Attenuator

This attenuator is an L pad attenuator where the loading per section is introduced by forward biasing a diode which is in series with the loading resistor. Biasing on the first section introduces 10-db attenuation on the signal. Biasing on the first and second sections will introduce 20-db attenuation of the signal. This sequence is required for proper 10-db steps.

4.5.13.4 Third Attenuator and Buffer

The third section of attenuation is the same circuit as the first and second section. Biasing on all three sections will produce 30-db signal attenuation. The buffer section is a darlington circuit for impedance match to the image filter and also an isolation between the attenuators and the image filter.

4.5.13.5 Image Filter

The image filter is an 8-element elliptical function filter designed for not more than 3-db attenuation at 17 MHz and not less than 10-db attenuation at 16.75 MHz. This is to attenuate the image foldover so that the predetected

signal at 0.25 MHz will be 10 db or more attenuated. The image filter is made up of 3 sections each in an individual cavity.

4.5.13.6 Mixer and LO

The mixer is a diode quad balanced mixer and the oscillator is a 17-MHz crystal controlled oscillator.

4.5.13.7 High Pass Filter

The high pass filter is a 3-section Butterworth with its 3-db cut-off at no more than 0.5 MHz and 10 db or greater at 0.25 MHz. Each of the three sections is placed in an individual cavity.

4.5.13.8 Filter Buffer

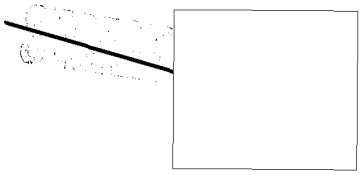
The filter buffer is a darlington circuit for isolation and impedance matching between the high pass filter and the low pass filter.

4.5.13.9 Low Pass Filter

The low pass filter is an 8-element elliptical function filter designed for a 3-db cut-off at 5.5 MHz and a 10-db or more attenuation at 5.75 MHz. This filter is also made up of three sections with each section in a cavity.

4.5.13.10 Integrated Amplifier

The integrated amplifier is an operational linear amplifier using a uA702 wide band DC amplifier whose gain is adjusted between 20 - 30 db as required.



4.5.13.11 Hard Limiter

The hard limiter consists of an emitter follower driver and grounded base linear amplifier and followed by an output emitter follower. The hard limiting is performed by the grounded base linear amplifier going to cut off on the positive cycle and the output emitter follower being cut off on the negative cycle. This signal will then be attenuated so that at 0.6 volt p-p, the signal will be in the linear region and at 0.7 volt p-p will be in hard limiting.

4.5.13.12 Tag Generator

The tag generator consists of a burst oscillator and a broadband tuned 250 Kc circuit. The Cos^2 wt. envelope is approximated by adjusting the trigger pulse width, by setting the decaying rate of the burst oscillator and by the broad band characteristics of the 250-KHz tuned circuit. See Figure 4.5-18.

4.5.13.13 Reference Oscillator

The reference oscillator is a crystal controlled 6-MHz oscillator. This will provide the 6-MHz tone and will also provide a pulse at a 6-MHz rate to the counter to derive the 46.875-KHz tone.

4.5.13.14 Tag Logic and Counter

The counter is a ripple-carry binary counter using the DTUL 950 pulse triggered binary. There are seven stages for a 128 counter.

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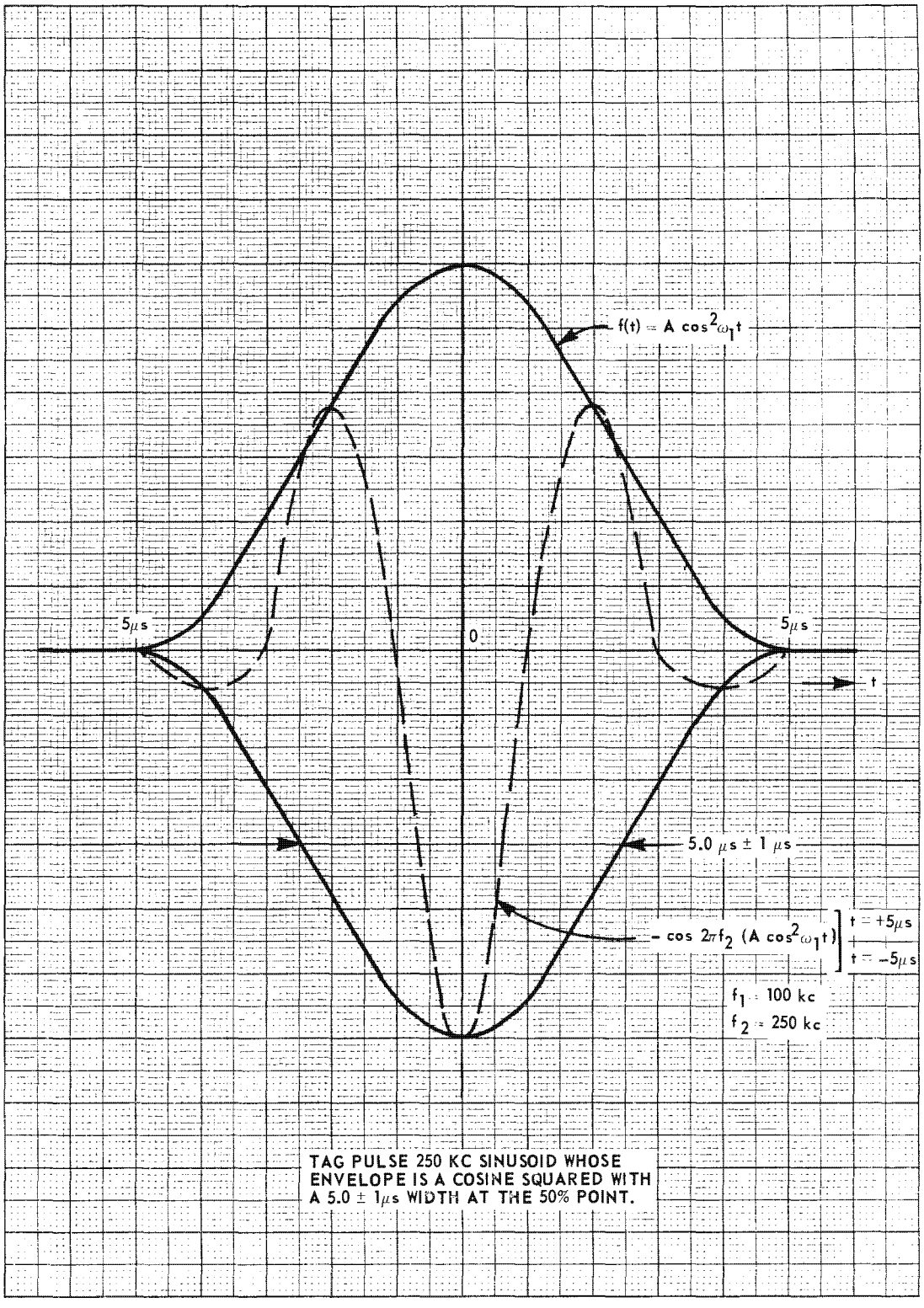

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Figure 4.5-18. Tag Pulse

The tag logic uses a DTuL 946 quad two-input gate element, a DTuL 950 and two DTuL 951 monostable multivibrator. Figure 4.5-19 shows a block diagram and a pulse timing chart.

When an SI pulse is received at t_o, the leading edge (after being inverted by the 946) will set the flip-flop to logic 1, if it is not already set. If at t_a an A/R inhibit appears, the leading edge will also be inverted by the 946 and the flip-flop will be reset to logic 0 if it is not already reset. At t_1 (the trailing edge of the SI pulse) the 2.5-usec one-shot will be triggered and its trailing edge at t_2 together with logic 1 on the flip-flop, initiates the 6.8-usec pulse for the tag-pulse trigger. Since the flip-flop was at logic 0 due to the AR inhibit pulse, the 6.8-usec one-shot will not be triggered. The following SI at t_n and no A/R inhibit show how the tag pulse will be initiated with the flip-flop at the logic 1 level.

4.5.13.15 Tone Filter

The tone filter is an active low pass 50 Kc filter similar to the type used in the phase channel called a phase filter.

4.5.13.16 Output Buffer

The output buffer has an input emitter follower where the tag tones are fed in and then resistively added to the predetected signal and tag pulse if any. The output is an NPN-PNP emitter follower darlington connection for impedance

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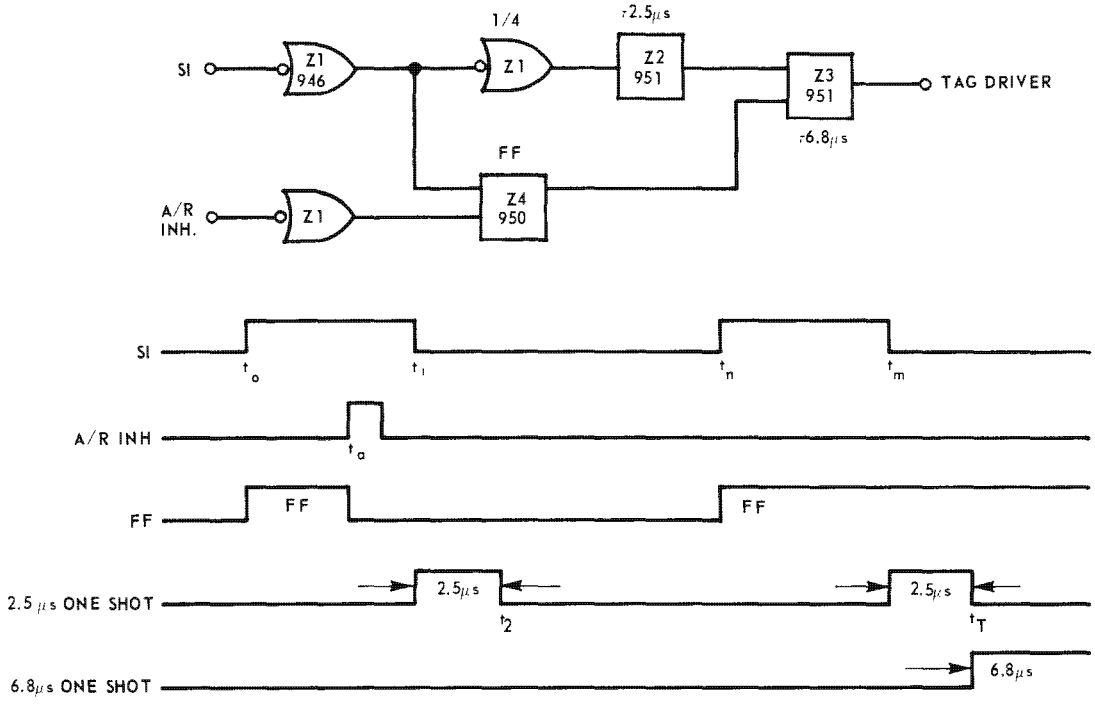

Figure 4.5-19. Tag Logic

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match and for 0 volt bias at the output for X coupling. The impedance match is selected to 75±5 ohms.

4.5.13.17 Summary of Technical Specifications

Pertinent specifications for the TTS subassembly are presented below in Table 4.5-13.

TABLE 4.5-13. TTS SUBASSEMBLY SPECIFICATIONS

INPUT POWERS	+8 v	+6 v	-6 v
INPUT SIGNALS			
Preamp Aux. Output			-28 dbm @ Tmax 20 MHz
SI_p (SI from Sig.Gen.)			Video Pulse 3.5 ± .5 volts 24 usec max.
A/R Inhibit (from A/R)			Video Pulse 3.5 ± .5 volts 150 nsec wide
Set Gain (10, 20 & 30 db ATTN)			Logic "1" .8 v Logic "0" .3 v
OUTPUT SIGNALS			
Signal Out (to recorder)			3 MHz ± 2.5 MHz @ -3 db 600 mv p-o max.
6 MHz Tone			6 MHz ± 5 Kc Adjustable Amplitude 2.5 mv to 50 mv

TABLE 4.5-13 (CONT'D)

46.875 Kc Tone	46.875 KHz ± 100 Hz Adjustable Amplitude 2.5 to 50 mv
Tag Pulse	Cosine square pulse envelope of 250 Kc centered at 250 Kc Amplitude 0.28 ±.02 volts Pulse width 5 usec @ 50% of envelope 2.5 ± 1 usec after trailing edge of received signal with respect to 10% point of envelope.

4.5.14 Recognizer Amplitude Threshold Subassembly

4.5.14.1 Introduction

The recognizer amplitude threshold performs the following functions over the 40-db dynamic operating range.

(1) Provide an amplitude confirm video pulse when the signal is above a level that can be set on command to Tmin, +5, +10, and +15 db with respect to system Tmin.

(2) Provide a video pulse from three threshold detectors when the signal is at the different level in the dynamic range. One threshold detector for Tmin +30 db and above, another

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for Tmin +20 db and above and a third one for Tmin +10 db and above.

A modular breakdown description of recognizer amplitude threshold is discussed next. Refer to Figure 4.5-20.

4.5.14.2 Buffer Amplifier Module

The buffer amplifier is a grounded-base linear amplifier similar to the DC amplifier in the phase channels. The input to the buffer amplifier is a gated logarithmic signal from the A/R log amplitude channel.

4.5.14.3 Threshold Driver

The threshold driver consists of four emitter followers to drive the individual threshold detectors. The threshold driver provides the proper attenuation to the signal so that all fixed threshold detectors can be made identical. Each driver will also provide isolation between the threshold detectors.

4.5.14.4 Fixed Threshold Detector

The fixed threshold detector is a diode temperature compensated Schmitt trigger with a similar Zener emitter follower output for DC coupled output and low emitter resistor as used in the SI generator for integrated circuits interfacing. The threshold detectors are AC coupled at the input since it receives only gated pulse.

4.5.14.5 Variable Threshold Detector

This is the same as the fixed threshold detector except that its threshold bias may be controlled.

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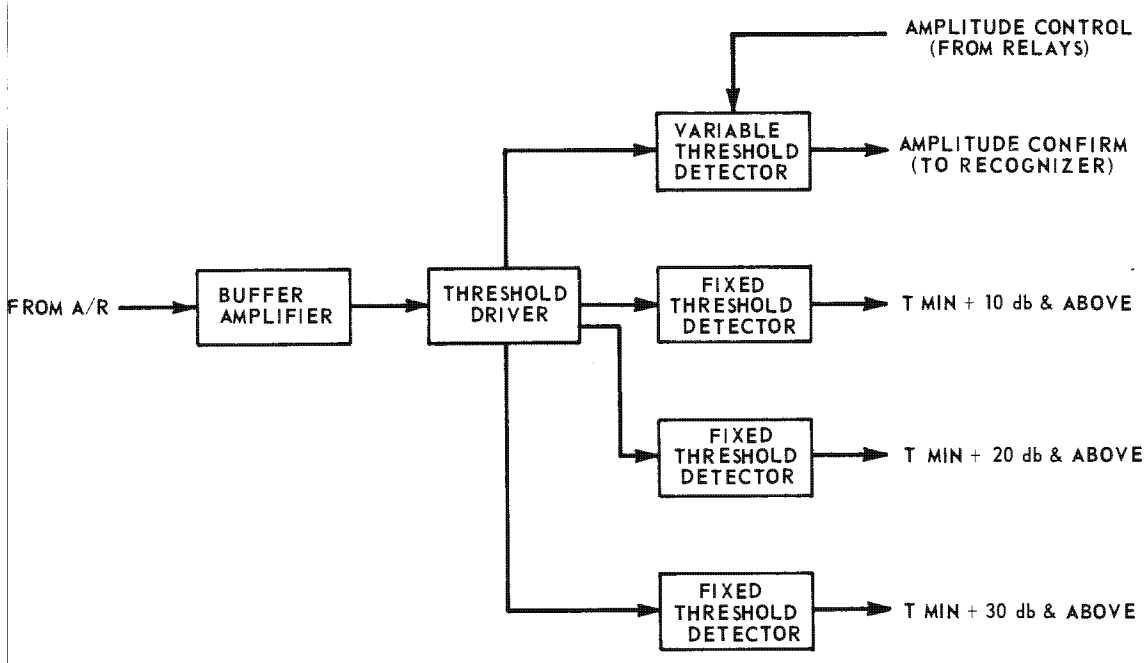

Figure 4.5-20. Recognizer Amplitude Threshold, Block Diagram

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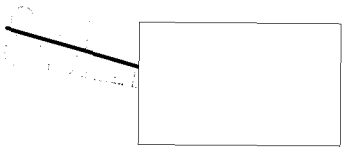

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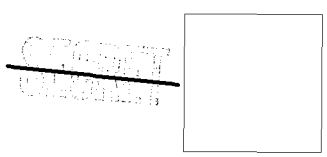
4.5.14.6 Summary of Technical Specifications

Pertinent specifications for the recognizer amplitude threshold are presented below in Table 4.5-14.

TABLE 4.5-14. RECOGNIZER AMPLITUDE-THRESHOLD SPECIFICATIONS

INPUT POWER	
+12 v	-8 v
INPUT SIGNALS	
Dynamic Range	40 db
Input Level	Video 1.8 V to 280 mv
Pulse Width	Gated 800 nsec max.
Recovery time	Less than 5.0 usec
Relay Ground	For Tmin, +5 db, +10 db and +15 db
OUTPUT SIGNALS	
Amplitude Confirm	Video pulse -3.5±.5 v (600 nsec max.)
Tmin + 10 db	Video pulse -3.5±.5 v (600 nsec max.)
Tmin + 20 db	Video pulse -3.5±.5 v (600 nsec max.)
Tmin + 30 db	Video pulse -3.5±.5 v (600 nsec max.)
Variable (Tmin, +5 db, +10 db, +15 db)	

4.5.15 Analog-to-Digital Converter



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4.5.15.1 Introduction

The analog to digital converter subassembly, Figure 4.5-21, receives phase, fine frequency and signal amplitude information. It holds the fine-frequency and amplitude information until a command is give to encode the information into a four-bit binary code and presents the binary coded information to the data handler. The phase information is sampled and held in the phase channels before being sent to the analog digital converter.

Ten signals are received in parallel from the IF subassemblies. Eight of the signals have amplitudes which correspond to phase information and the two remaining pulses have an amplitude which is proportional to the signal strength and fine frequency of the particular emitter being measured. A trigger pulse (phase gate) is received coincident with the IF signals. This pulse triggers a gate driver which serves to open the sample-and-hold gate for amplitude and fine frequency. The outputs of the sample and hold of the 10 signals serve as DC signals, from low impedance sources, to the commutator gates.

Each commutator gate receives a trigger signal from the data handler. The signals are spaced at 960 nsec intervals and are on separate lines, Figure 4.5-22. The individual commutator gates open for a period of approximately 100 nanoseconds. This results in a train of 10 gated pulses separated by 960 nanoseconds with the amplitude of the

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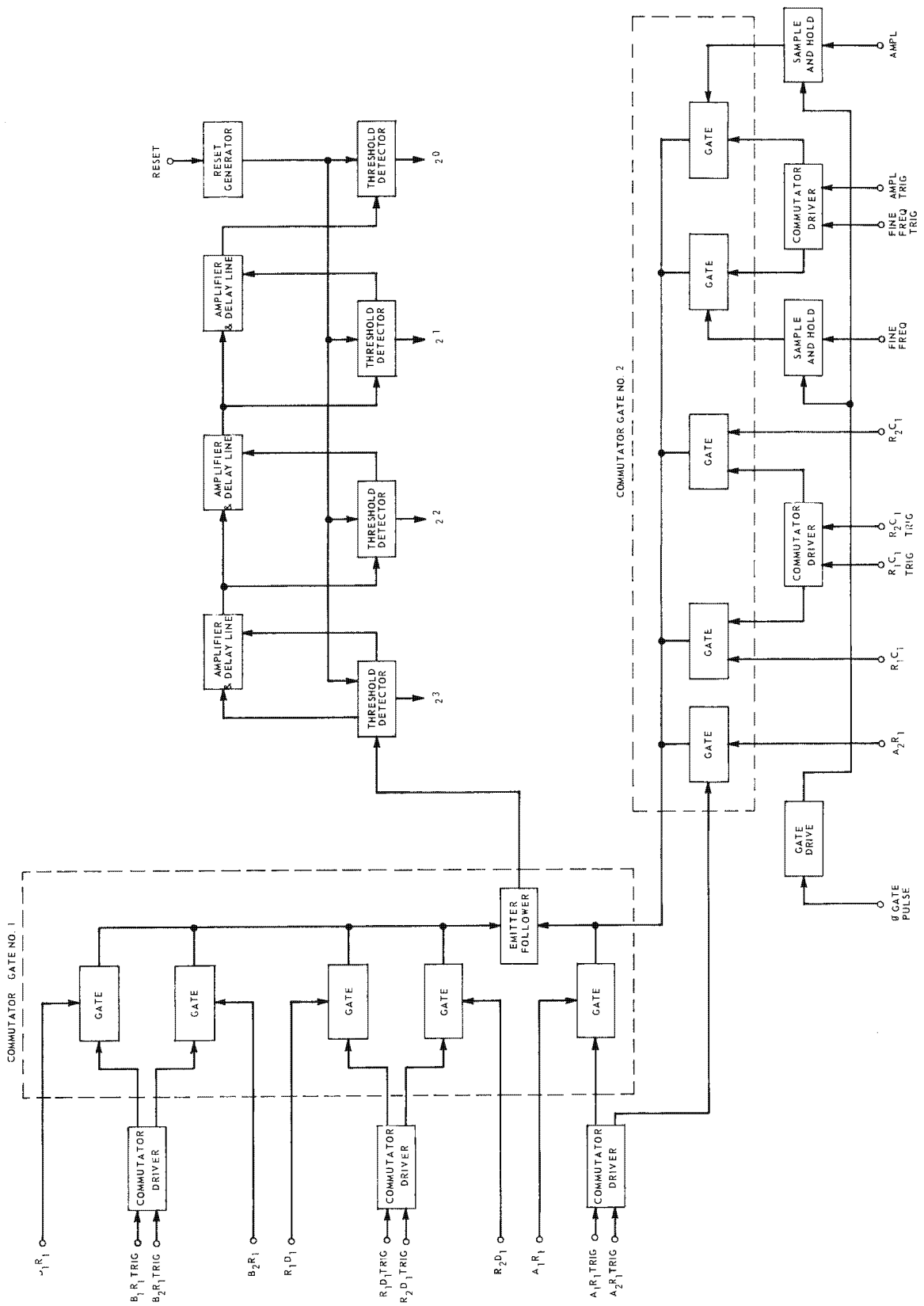

Figure 4.5-21. Analog-To-Digital Converter

individual pulses being proportional to a particular sample and hold output. These 10 pulses are presented serially to the four-bit analog-to-digital converter.

The analog-to-digital converter portion of the subassembly encodes each input pulse into a four-bit binary code. The input pulse is from 0 to +5 volts in amplitude and approximately 100 nanoseconds in time. The output "1" bit is in the form of a 4-volt pulse approximately 200 nanoseconds in time. A logic 0 level is the absence of a pulse.

The analog-to-digital section, consists of four threshold detectors, three amplifiers and a reset generator. The encoding is performed in a serial manner. (The most significant bit is encoded first and so on until the least significant bit is encoded.) A reset trigger pulse is received from the data handler approximately 480 nanoseconds after each input signal pulse to the A/D converter. This trigger pulse is processed into a 30-nsec spike which serves to reset each threshold detector in preparation for the next input signal.

The weight of the most significant bit is one-half full scale, 2.5 volts. An input signal of 2.5 v will cause the detector to change state and the output will be interpreted as a "1" bit. Conversely, for an input signal of less than one-half full scale, the detector will not change state and the output will be interpreted as a "0" bit. If the detector is in the "0" state a reference voltage of zero volts is

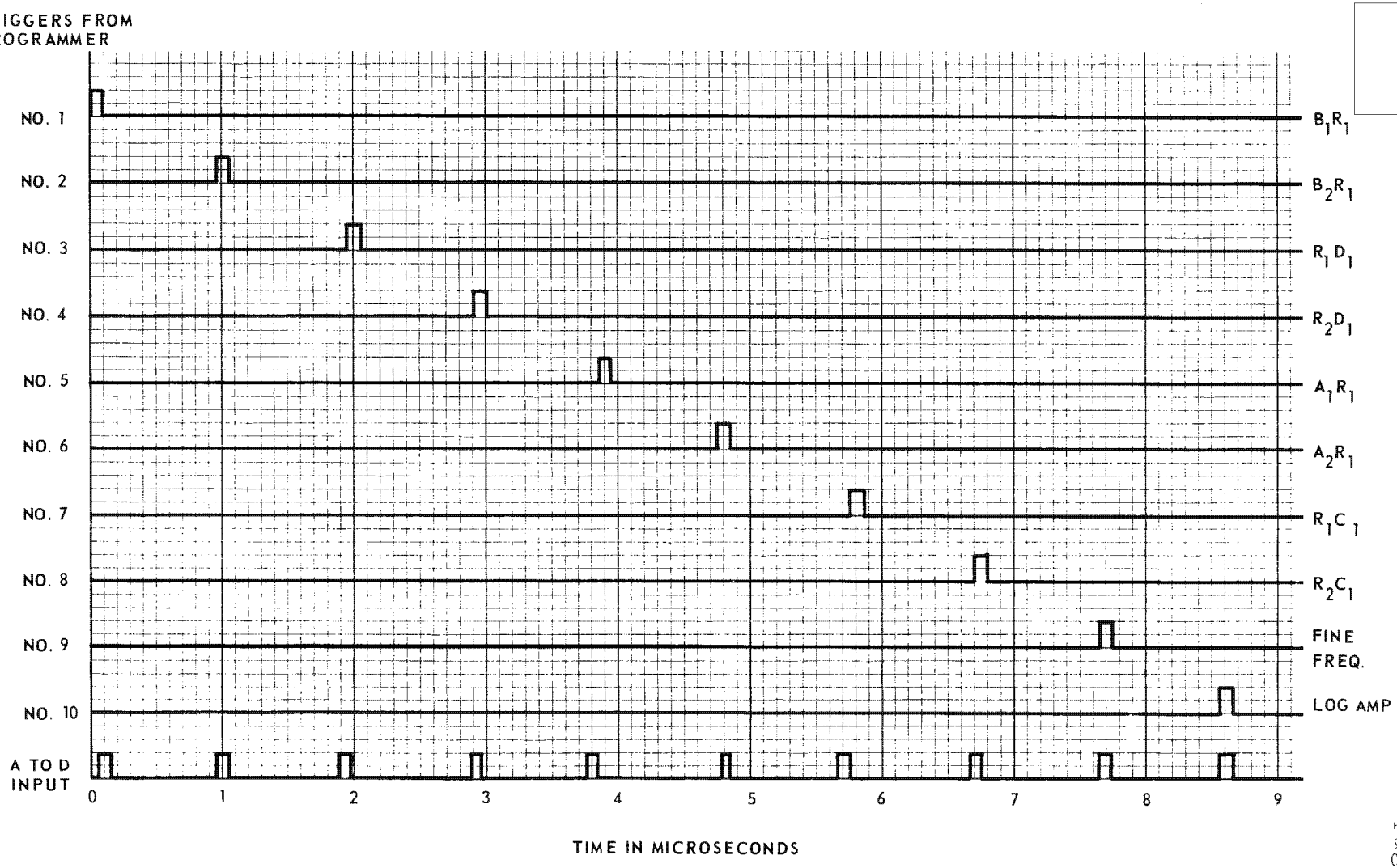

Figure 4.5-22. Commutator Timing Diagram

TABLE 4.5-15. INPUT VOLTAGE VS. OUTPUT CODE

ANALOG INPUT VOLTAGE DECISION LEVEL	A TO D OUTPUT BINARY CODE	READ OUT INTERPRETED AS
	0000	.15625 ± .15625
.3125	0001	.46875 ± .15625
.6250	0010	.78125 ± .15625
.9375	0011	1.09375 ± .15625
1.2500	0100	1.40625 ± .15625
1.5625	0101	1.71875 ± .15625
1.8750	0110	2.03125 ± .15625
2.1875	0111	2.34375 ± .15625
2.5000	1000	2.65625 ± .15625
2.8125	1001	2.96875 ± .15625
3.1250	1010	3.28125 ± .15625
3.4375	1011	3.59375 ± .15625
3.7500	1100	3.90625 ± .15625
4.0625	1101	4.21875 ± .15625
4.3750	1110	4.53125 ± .15625
4.6875	1111	4.84375 ± .15625

applied to the next amplifier to be summed with the incoming signal. If the threshold detector is in the "1" state, a reference voltage of -2.5 volts is applied to the next amplifier to be summed with the incoming signal. The reference voltage serves to subtract the weight of the first bit from the signal.

Each succeeding stage of the A/D operates in a similar manner. Figure 4.5-23 illustrates the A/D timing and Table 4.5-15 illustrates the input voltage versus the output code.

4.5.15.2 Sample and Hold Module

The fine frequency input signal to the sample and hold is a pulse from 0 to +10 volts in amplitude with a pulse width of 200 nanoseconds. For the amplitude information the pulse amplitude is from 0 to +6.0 v. The gate driver, triggered by the pulse gate pulse, serves to open the sample gate which allows the "hold" capacitors to charge to the input voltage.

The first transistor stage in the Sample and Hold module is a constant-current generator which serves to subtract the "pedestal" voltage from the incoming signal.

The sample and hold output circuits serve to present a high impedance to the "hold" capacitor and a low impedance to the commutator gate.

4.5.15.3 Gate Driver (same as described in paragraph 4.5.12.13)

4.5.15.4 Commutator Driver and Commutator Gates

Each commutator gate receives a trigger on a separate line from the programmer section. Each gate driver opens its associated gate and lets 100 nsec of amplitude information through to the analog to digital section. The timing diagram illustrates the commutator timing. See Figure 4.5-22. Each commutator gate consists of a ring diode gate driven by a series of circuits which serve to shape the input trigger from the data handler. The ring diode gate is opened for 100 nanoseconds regardless of the pulse width from the data handler.

4.5.15.5 Threshold Detector

The input from the commutator consists of 100-nsec pulses from 0 to +5 volts in amplitude. Each threshold detector is set to change states when its input exceeds 2.5 volts in amplitude. The threshold detector furnishes an output reference voltage to the summing network. This reference voltage is 0 volt when the input to the threshold detector is less than 2.5 volts, and changes to -2.5 volts when the input exceeds +2.5 volts.

The threshold detector utilizes a tunnel diode biased just below its peak current point. A 2.5-volt input signal furnishes just enough current to trip the tunnel diode to its high voltage state. This change in voltage is amplified and coupled out as a "one" bit to the data handler. The voltage change is also processed and coupled into the associated amplifier as a -2.5 volt reference level.

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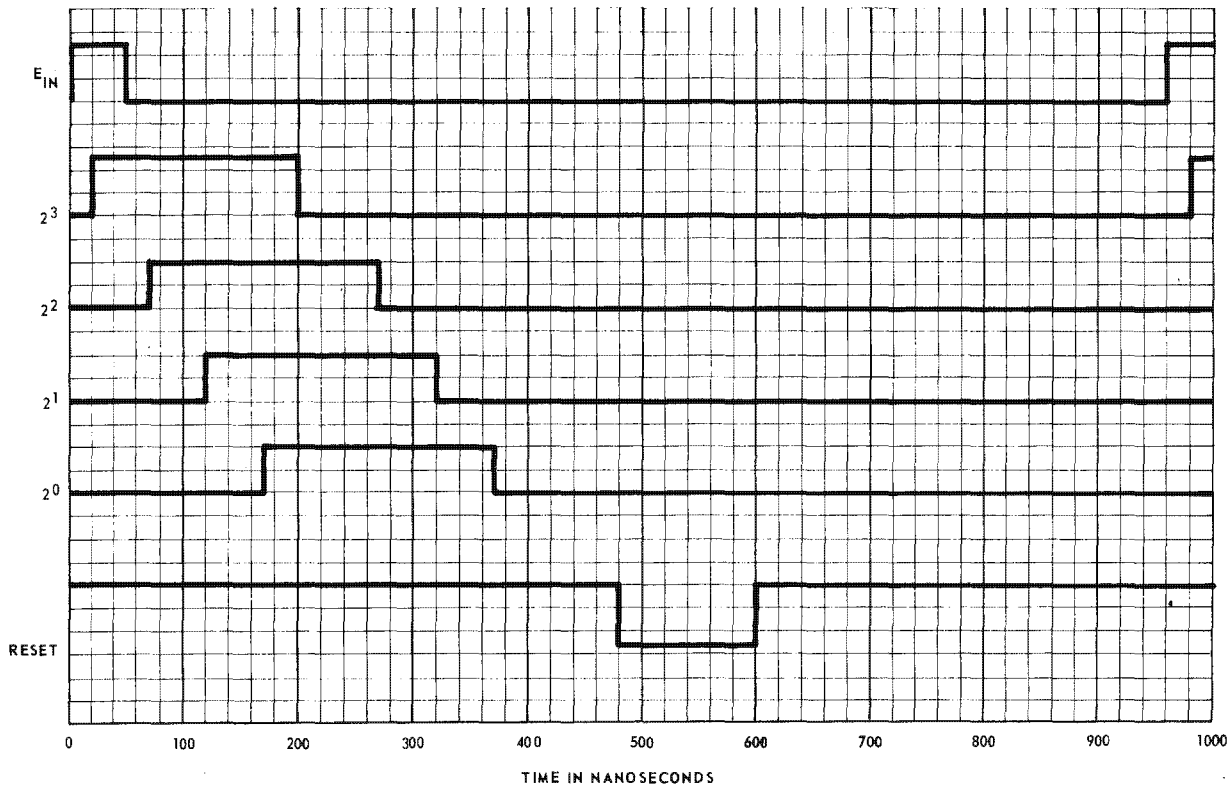

Figure 4.5-23. Analog-To-Digital Timing Diagram

TABLE 4.5-16. A/D CONVERTER SPECIFICATIONS

INPUT POWER		
	+8 volts	-8 volts
INPUT SIGNALS		
	Gate Pulse	6.5 v PW 220 nsec
	8 Phase Inputs (From Phase Channels)	Amplitude -2.5 v to +7.5 v
	1 Log Amplitude (From Amplitude Ratio)	Amplitude - 0 to 6 volts 600 nsec max.
	10 Input Trigger Pulses (From DH)	Amplitude -3 volts PW - 210 nsec
	Reset Pulse (From DH)	Amplitude - 3 volts PW - 120 nsec
	Frequency Encode Pulse (From Freq. Confirm Channel)	9.0 volt max. Video Pulse 220 nsec wide
OUTPUT SIGNAL		
	4 Binary Outputs (To DH)	A one(1) is represented by 3.5 $\pm$ .5 volt pulse, PW = 200 nsec A zero (0) is zero output

50X1

4.5.15.6 Amplifier Module

The input signal to the first threshold detector stage is also applied to the first amplifier, (Figure 4.5-21) The signal is delayed by 40 nsec in order to allow the associated threshold detector to make its "decision". Following the delay line, the signal is summed, in a resistive network, with the reference voltage from the threshold detector.

The gain of the stage from the input of the delay line to the output to the next stage is

$$A = 2\ (e_{in} + e_{reference})$$

The reference voltage is zero if the associated threshold detector is in a zero state and is -2.5 volts if the associated detector is in a "one" state.

4.5.15.7 Reset Generator

The reset generator receives a signal from the data handler approximately 480 nanoseconds after each commutator trigger. This signal is processed into a 30 nanosecond trigger pulse which serves to reset each threshold detector.

4.5.15.8 Summary of Technical Specifications

Pertinent electrical specifications are presented in Table 4.5-16.

4.6 Data Handler Assembly

4.6.1 Introduction

The Data Handler contains the logic circuits necessary for parallel-processing of input signals. Digital measurement and conversion circuits which generate codes for such signal parameters as pulse width, amplitude, pulse repetition interval, D/F location, and frequency are contained in this assembly. The vehicle analog voltage inputs for pitch and roll are also converted to digital format and stored. See Figure 2.1-1. The functional sections of the Data Handler are as follows:

a) Phase Combiner - Accepts two 4-bit binary codes (unshifted and shifted phase) from the A-D converter and combines them into a single 5-bit digital code that is unambiguous over the complete range of 360 degrees.

b) Phase Coder - Combines the 5-bit fine phase code with the 5-bit coarse phase code from the phase combiner to produce a 7-bit code for use in addressing the space window logic.

The Coder also monitors the inputs from the Phase Combiner and generates an "x coordinate" or "y coordinate" inhibit signal if the inputs indicate that the emitter is located

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outside the system field of view.

c) Space Window Logic - A scratch pad memory which stores the buffer storage address of the first pulse data for each emitter in the field of view.

d) Inhibit Logic - Monitors inhibit and confirm signals from the IF section and the FOV inhibit from the Coder/Combiner and generates a mode-dependent master inhibit signal if all confirm signals are not received or if any inhibit is received.

e) Programmer - Contains logic for system control under the various modes of operation. It initiates processing of incoming signals, generates timing signals for Calibrator, Phase Coder/Combiner, Attitude Encoders and Dwell Timer. Also initiates generation of all time-attitude words, identifies the data words, and provides change frequency commands to the local oscillator control logic.

f) PRI Encoder - Digitizes the time interval between confirmed input signals from a given source.

g) Buffer Storage Control Logic - Controls loading, spacing and shifting of the digitized

information to the CSU, through the output register, and contains the parity generator which provides even parity in bits 65, 104, 143, and 182 of each data word.

h) Buffer Storage - Stores up to 64 complete data words and serves as a high speed temporary data buffer which permits parallel processing of incoming signals.

i) System Clock - Provides the various timing pulses for subsystem operation.

j) Pulse Width Encoder - Measures the width at the input signal between specified limits. It provides a 64 increment, (6-bit) linear code for pulse widths up to 8 u sec. For greater than 8 u sec PW, the output reads all ONES.

k) Time Encoder - Counts incoming pulses from the vehicle at 8 pulses per second. Provides a 20-bit binary register to give elapsed time in 1/8-second increments to a maximum of one day. Also provides a calender register of 3 bits to give elapsed time in days to a maximum of 8 days. Both registers can be re-set on command from the vehicle.

l) Attitude Encoder - Consists of two identical A/D converters which are used to digitize

the incoming analog pitch and roll signals.

m) Test Generator Logic - Provides modulation pulses and an enable level to the R.F. calibrate oscillator at specified time intervals and for specified durations. Output of the calibrate oscillator is fed into the R.F. strip line and processed in the same manner as a received signal. Since all parameters of the calibrate signal are known, a real-time check of system operation is obtained.

n) Data Handler Interface Logic - Provides discrete component gating to interface the integrated circuit logic to the vehicle input/output signal levels.

o) Marker Word Generator - Provides a 48-bit word output consisting of time, frequency, and other status information. This word appears at the output in 3 LRZ form and is available both for DSU recording and for direct readout through the wide-band Data Link.

p) Scan Control - Consists of the LO Counter and the partial scan control logic. The partial scan control logic provides the necessary circuitry to allow the system to search

through either one or both of two variable length segments in the frequency scan band. The length and position of the partial scan segments are selectable and may be placed anywhere in the frequency band so long as the segment limits do not overlap.

The LO counter is a binary counter and counts Change Frequency Command (CFC) pulses to provide an output which is used with a D/A converter to control the frequency of the system Voltage Controlled Oscillators. The output from this counter also provides the frequency information which is inserted in the Marker Words and in the EOB data words.

q) Relay Logic - Interfaces with the Vehicle Command Computer to provide input commands to the system.

r) Telemetry Unit - Consists of circuits necessary to isolate and condition the signal required to provide indications of voltage levels, temperatures and operation of the system.

4.6.2 Phase Combiner

The purpose of the Combiner is to remove ambiguities from the phase information (over a 360° interval) by 50X1

combining the quantized output of one phase detector with the quantized output of a second phase detector whose input is the first detector input shifted 90 degrees. See Figures 4.6-1 and 4.6-2. The Phase Combiner output and corresponding A-to-D Converter outputs are shown in Figure 4.6-3. From these transfer characteristics, it can be seen that each quantized phase detector output is unambiguous over a 180 degree range. By combining the two 4-bit outputs to obtain a fifth bit, it is possible to derive phase code which is unambiguous over the range of 360 degrees. From Figure 4.6-3 it can be noted that for the fine phase at least one of the A-to-D outputs is either 0000 or 1111 over the range of 0 to 360 degrees. By detecting which output is 0000 or 1111, it is possible to derive the required fifth bit of phase information.

The coarse phase output is very similar to the fine phase output except for change of gain. The effect of this gain change is to change from the condition that at least one output is 0000 or greater than 1001.

The combiner receives 4-bit input words from the A-to-D converter. Each four bits of information represents the quantized value of the phase detector outputs. Words are received in the following order:

1. Fine phase Y
2. Fine phase Y shifted 90 degrees
3. Coarse phase Y

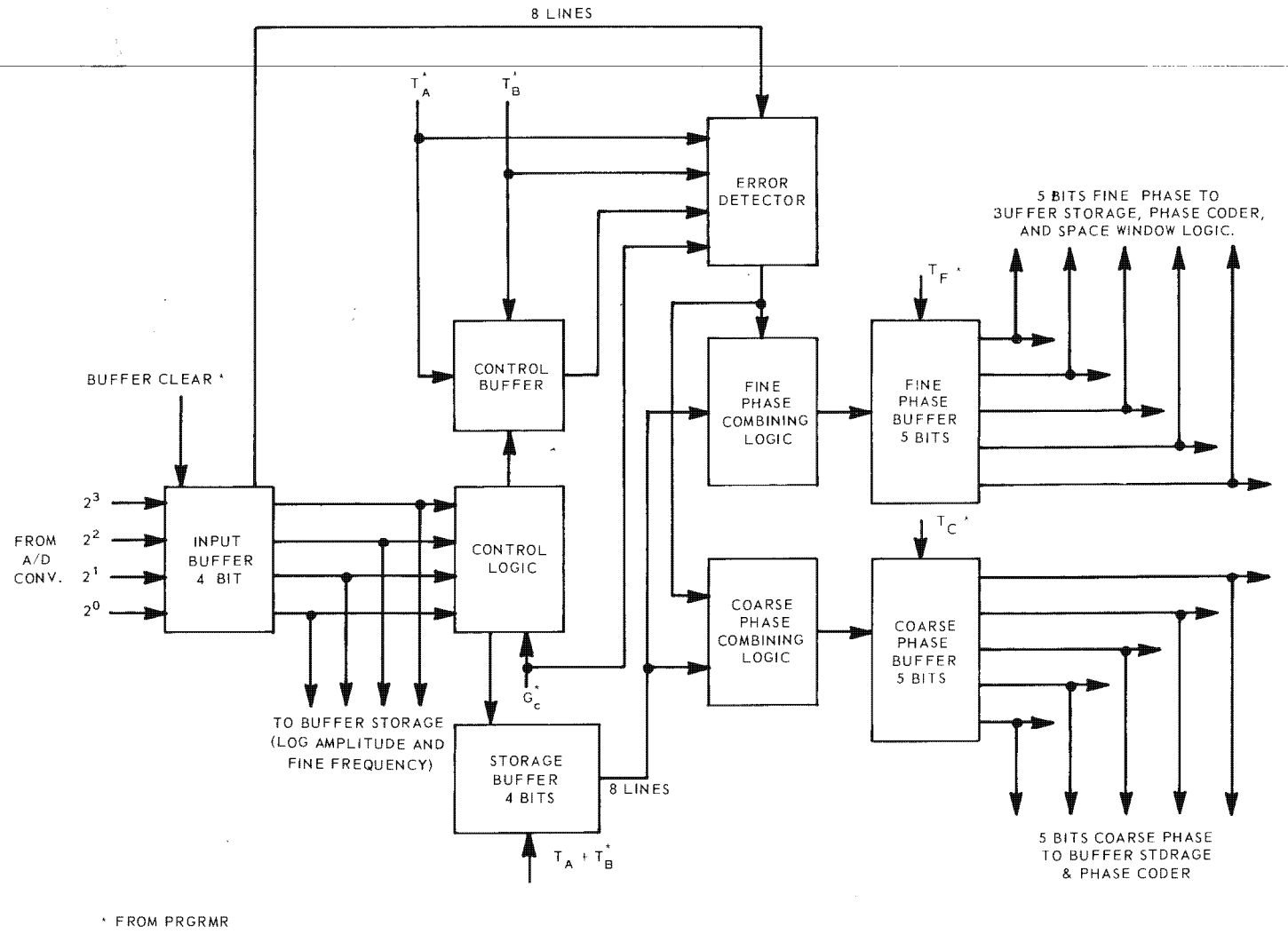

Figure 4.6-1. Phase Combiner Block Diagram

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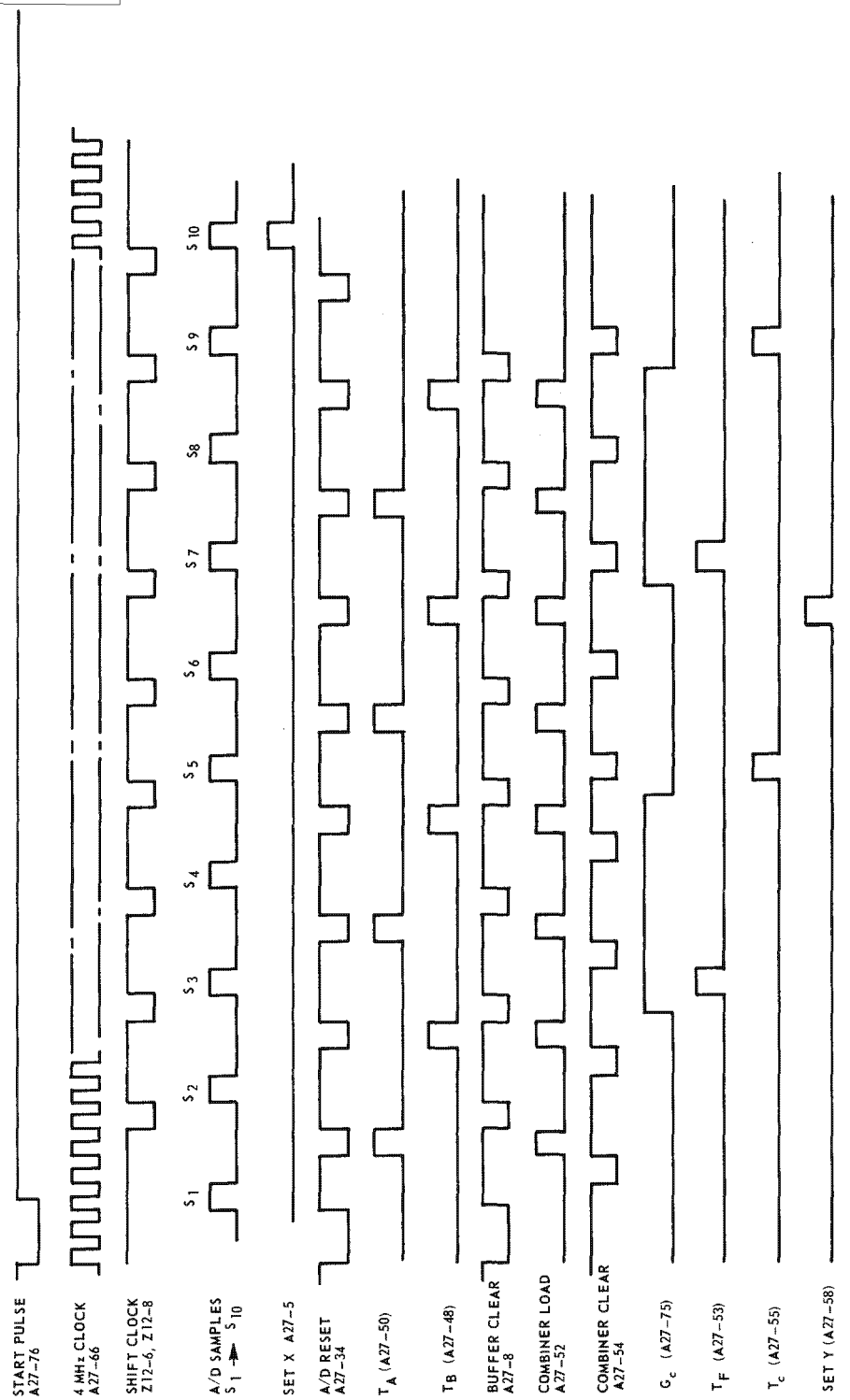

Figure 4.6-2. Phase Combiner Timing Diagram

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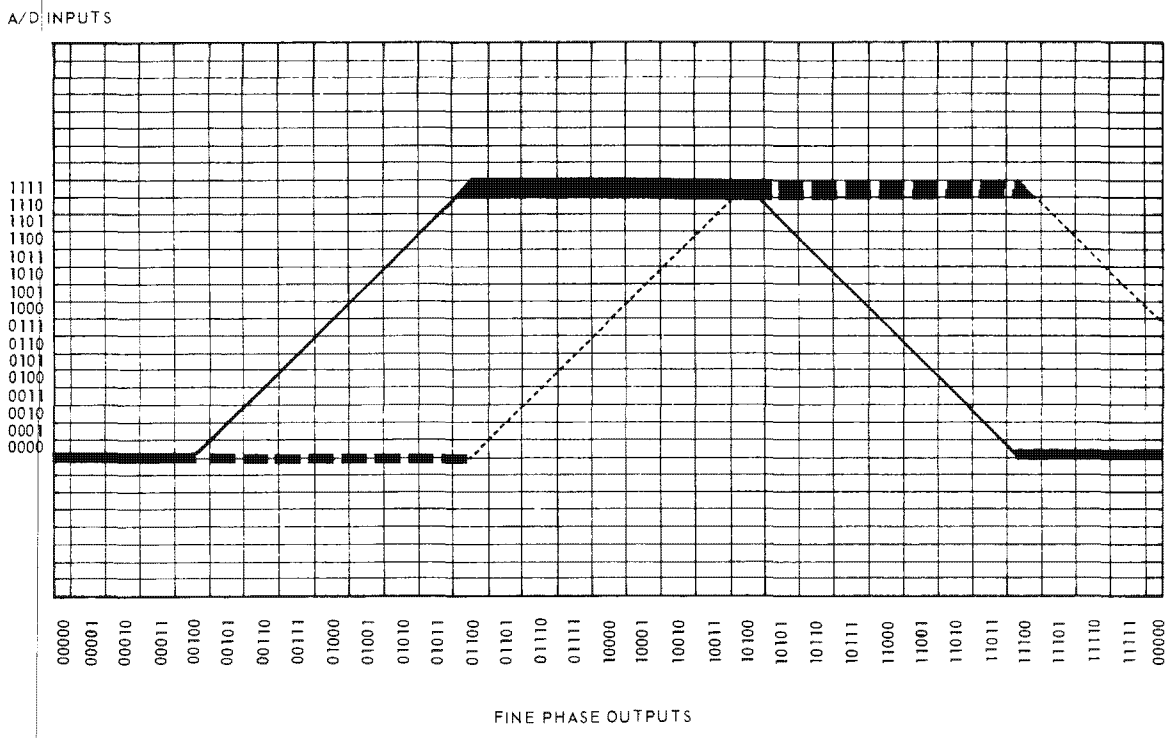

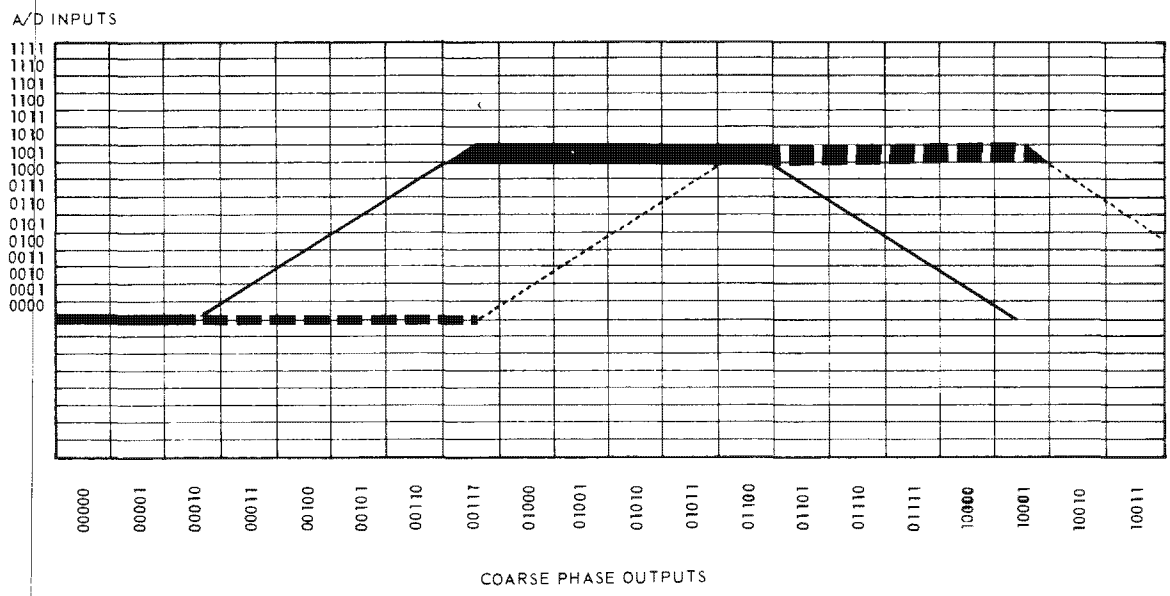

Figure 4.6-3. Phase Combiner Outputs

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4. Coarse phase Y shifted 90 degrees
5. Fine phase X
6. Fine phase X shifted 90 degrees
7. Coarse phase X
8. Coarse phase X shifted 90 degrees
9. Fine Frequency data
10. Amplitude information

The timing diagram in Figure 4.6-2 illustrates the following sequence of events.

1. Unshifted Y_f data loaded into input buffer.
2. Storage and control buffers cleared by Combiner Clear.
3. A/D Converter reset and control or Storage buffer set as determined by Control Logic Limit Detecting gates.
4. Input Buffer cleared.
5. Steps 1, 3, and 4 repeated for shifted Y_f data.
6. Combined Y_f data loaded into 5-bit buffer.
7. Steps 1 through 6 repeated for Y_c data during the interval between sample pulses S_3 and S_5.
8. Steps 1 through 6 repeated for X_F and X_C data during the interval between S_5 and S_9.

The A-to-D output is received by the input buffer which consists of Z24 through Z28 of combiner card, section A

(4124-64201). Prior to receiving each data word from the A-to-D converter, this buffer is cleared; therefore, a pulse on any input line, which represents a logical one, sets the corresponding flip-flop, and it remains in the "one" state until the buffer is cleared again. Timing pulses to the combiner are synchronized with sample pulses to the A to D converter.

The Control Logic shown on the block diagram is composed of limit detecting gates which control the loading of the Storage and Control buffers. Gate Z18-8 detects the presence of the limit 1111 at the input while Z18-6 detects the presence of 0000 at the input. Gate Z8-8 detects the presence of the limit 1001 or greater at the input during a coarse phase input.

Z2-11 and Z4-3 are limit detecting buffer outputs which are loaded during the unshifted sample. Z4-3 indicates the presence of 1111, (1001 or greater during coarse phase) during the unshifted sample. Z2-11 indicates the presence of 0000 during the unshifted sample. Z2-8 and Z4-8 perform the same function during the shifted sample. Z2 and Z4 are cleared by the combiner clear which occurs as shown in the timing diagram for the programmer "A" timer.

The outputs of the input buffer are gated via Z10 and Z20 to the storage buffer (Z1, Z2, Z11, and Z12 on board 64202) which stores information contained in the input buffer, except when it is blocked by the limit detecting gates.

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If both the shifted and the unshifted samples are blocked by the limit detecting gates, the buffer stores 0000, the value to which it is cleared by the combiner clear.

In addition to the input buffer, Section A (Board 64201) of the Coder/Combiner contains the logic for detection and correction of measurement errors. In normal operation, the Combiner receives 4-bit codes for unshifted and shifted phase for a given pair of phase channels.

Since the operation of the Combiner is dependent upon one of the phase curves being 0000 or 1111 (1001 or greater for $\emptyset_c$) while the other phase curve has a value in the encoding range; it is necessary to have an error detector circuit to detect if both curves, shifted and unshifted phase, are in the encoding region. Such a condition could only occur in the area of the cross over points, that is, in the vicinity of output codes 00100, 01100, 10100, or 11100. The combiner error detector senses that both the shifted and unshifted phase curves have values in the encoding region (within $\pm 3\frac{1}{2}$ increments of a crossover point) in which case the output buffers and the limit detecting buffers are reset and the error detector forces the appropriate cross over code to appear at the combiner output by selecting the appropriate values of E and F as indicated in Table 4.6-1. For errors greater than $3\frac{1}{2}$ increments, the Combiner output is 00000.

Sections B and C are gates which decode the

information from Section A into the combined output. Two bits are generated from the limit detector buffers and modified by the error detector for use in the decoding. These two bits are labeled E and F in the following table in which the relationship to the limit detector buffer outputs is shown.

TABLE 4.6-1

COMBINER ERROR DETECTOR OPERATION

Unshifted = 1111	Unshifted = 0000	Shifted = 1111	Shifted = 0000	EF	Combined Ø
0	1	0	0	00	315° -45°
0	1	0	1	00	45°
0	0	0	1	01	45° -135°
1	0	0	1	01	135°
1	0	0	0	10	135° -225°
1	0	1	0	10	225°
0	0	1	0	11	225° -315°
0	1	1	0	11	315°

Considering this, and defining A, B, C and D to be the storage buffer outputs with A being the most significant bit, then the logical equations for the fine phase combiner output are as given below: (A_F = MSB)

$$A_F = EF + E'F' (AB+AC+AD)+E'F'(A+B'C'D'+BCD)$$

$$B_F = E'F'(AB+AC+AD)+E'F(A+B'C'D'+BCD)+$$
$$EF' (A'BD'+A'C'D+A'B'C)+EF(A'+B'C'D')$$

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$$C_F = (EF+E'F')(AB+AD+AC)+(E'F+EF')(A'C'+A'B'+A'D')+(A'B'C'D')$$

$$D_F = (EF+E'F')(BC'D'+B'D+B'C)+(E'F+EF')(BC'+BD'+B'CD)$$

$$EF = CD' + DC'$$

Gating for the fine phase combiner is provided by Z1 through Z9 and Z18 on Section C (Board 4124-64203). Buffers for these outputs are provided by Z10 through Z17.

Additional gating is required for the coarse phase data, as the Phase Coder requires the output codes for both coarse and fine phase to be straight binary. The logic equations for the coarse phase combiner and the intermediate bit G are: (A_C = MSB and A, B, C, D are the storage buffer outputs).

$$G = A'B' + A'BC'D'$$

$$A_C = EFGB'(CD)' + E'F'G'$$

$$B_C = EF' + EF\left[G' + G(B+CD)\right]$$

$$C_C = F\left[G' + A'B'CD + A'BC'D'\right] + EF'(S=1) + E'F(U=1)$$

$$D_C = E'F'\left[(S=0) + G'\right] + E'F(A'B'C' + B'C'D' + A'B'D' + A'BCD) + EF\left[A'B(CD)' + A'B'CD\right] + EF'G'$$

$$E_C = (E'F' + E'FG)(CD' + C'D) + E(CD + C'D')$$

In these equations, the functions U and S refer to the limit condition of the unshifted and shifted data as indicated by the Control Buffer outputs. Gating for the coarse phase combiner is provided by Z1 through Z20 of board 4124-64202.

Output of this gating is buffered by Z18 through Z25 on board 4124-64203. Amplitude information is provided for the buffer storage directly from the input buffer. Frequency data is stored in a 2-bit auxiliary buffer on Card A6B.

Since the x phase data is processed immediately after the y phase data and both sets of combined data are required by the SWI addressing logic and are required in the output data word, it is necessary to transfer the y phase data to another buffer so that both x and y data can be retained. This transfer is made at the same time that the FOV logic is sampled. The y phase buffer is located in the Buffer Storage logic section, on board 4124-64226.

4.6.3 Phase Coder

The function of the Phase Coder is to provide two additional bits of phase information which, when added to the 5-bit combiner output, provides a 7-bit binary code that unambiguously describes the X or Y co-ordinate of a point in the system field of view. This code is produced from the coarse and fine phase codes which are generated in the Phase Combiner. The block diagram of the Phase Coder is shown in Figure 4.6-4. Refer to the Coder schematic, drawing No. 4124-64004 for additional details. The coarse and fine phase data are clocked into the Phase Combiner buffers by the appropriate pulse (T_f of T_c) from the A timing generator and the buffer outputs are used by the coder. Encoding action is such as

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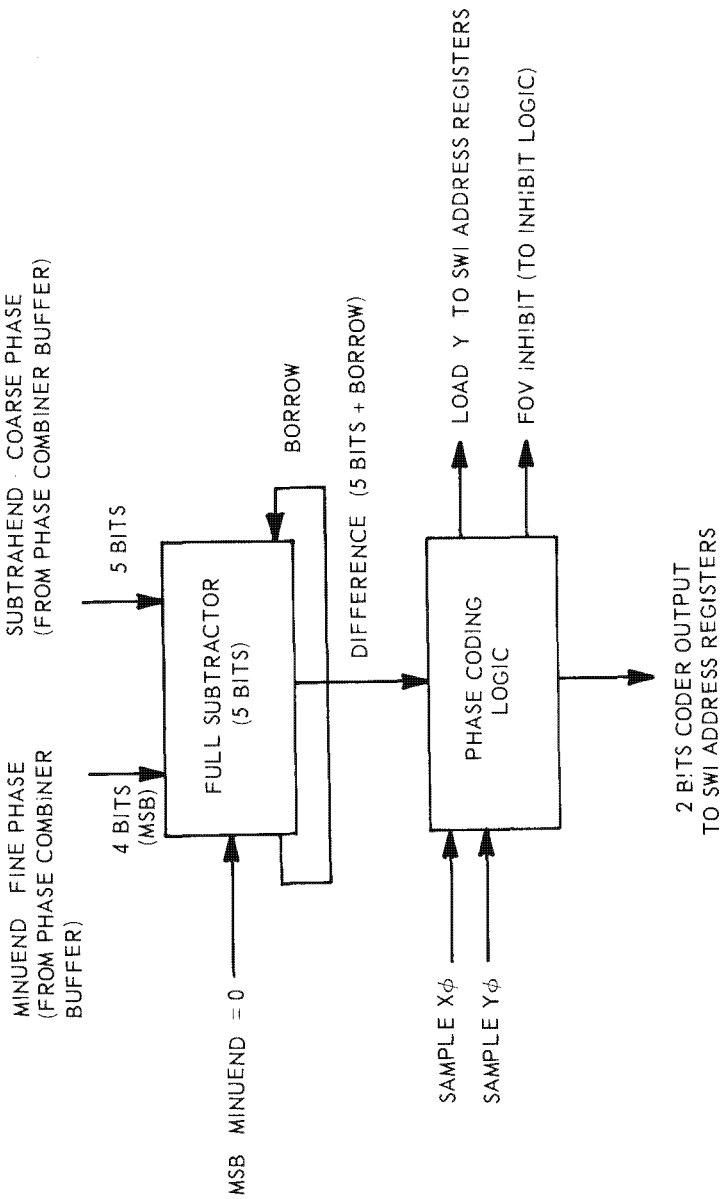

Figure 4.6-4. Phase Coder, Block Diagram

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to give an output code (T U V W X Y) consisting of two bits (T and U) generated in the Coder and the four bits of the fine phase from the Combiner. Calculations are also made to determine if the point described by the coarse and fine phase inputs is within the boundary of the field of view. If the point lies outside the field of view, a field-of-view (FOV) inhibit command is issued via the inhibit logic circuitry to stop the processing of information. Figure 4.6-5 is a representation of the system field of view.

Implementation of the FOV logic in the Coder can be greatly simplified from the straight combinational logic approach by recognizing the relationship between the absolute values of the 5-bit codes for coarse and fine phase. It can be seen that if the values of the fine phase are divided by two and the corresponding coarse phases than subtracted from them, the absolute differences obtained fall into ranges that can be used to generate a non-ambiguous phase code for the range -900° to + 900° (Horizon-to-Horizon). For this system, the range -720° to + 720° was chosen. This range can be obtained by generating two bits of phase (T and U) which, as previously mentioned, are the two most significant bits of phase and then determining which 360° interval the phase is in according to the following:

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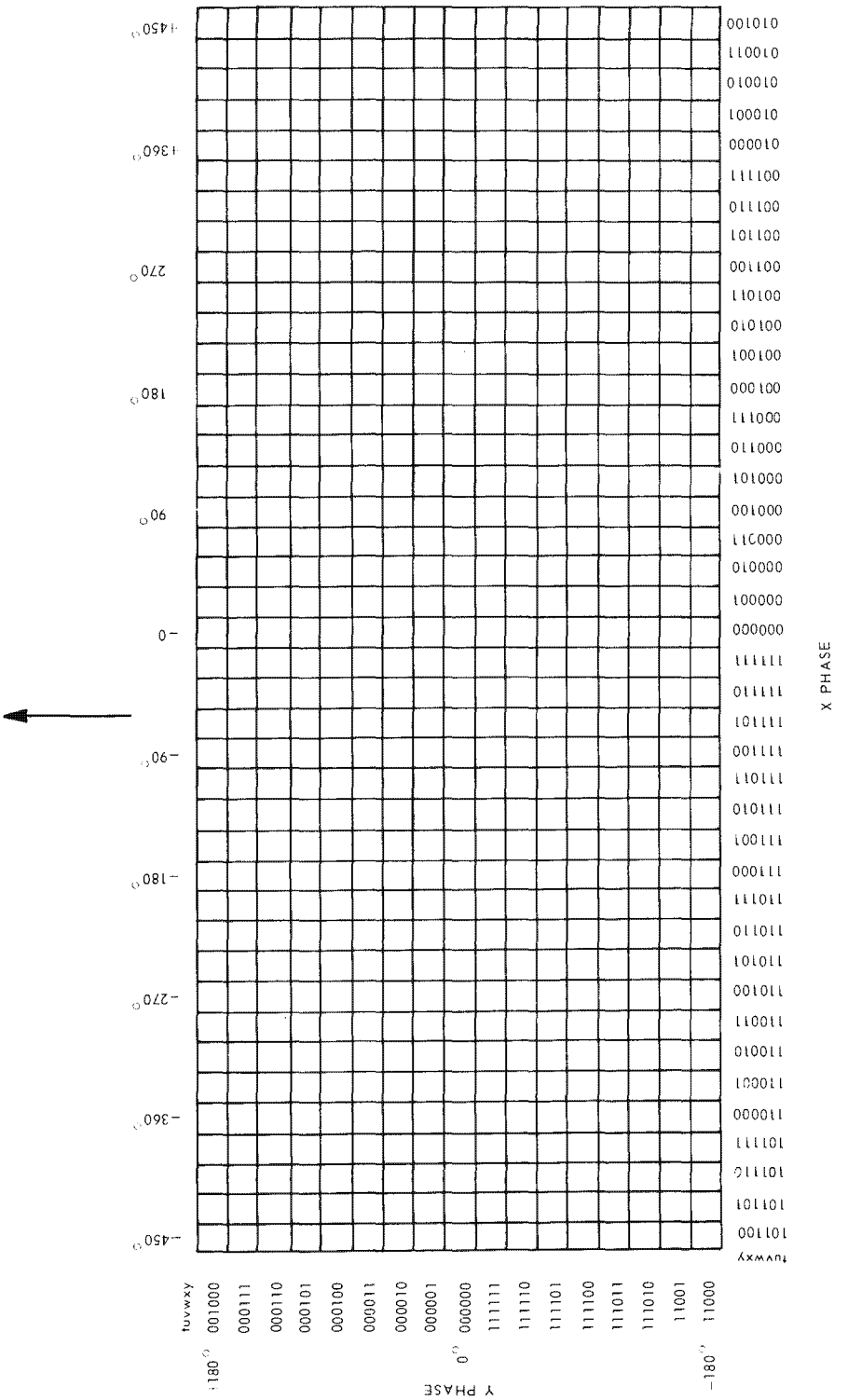

Figure 4.6-5. System Field of View

[redacted]

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OUTPUT	LOCATION IN FIELD OF VIEW
T U	Fine Phase Degrees
00	0 to +360
01	+360 to +450
10	-450 to -360
11	-360 to 0

Ranges for the absolute difference between the fine phase (divided by two) and the coarse phase are given in the following table as an aid to understanding operation of the Coder logic:

TABLE 4.6-2 PHASE CODER AMBIGUITY REMOVAL LOGIC

MSB Borrow = 1 Ranges for A-B	TU	MSB Borrow = 0 Ranges for A-B	TU
00000 to 00001	00	00000 to 00010	00
00010 to 00101	11	00011 to 00110	01
00110 to 01001	10	01011 to 01110	10
01110 to 10001	01	01111	11
10010 to 10011	00		

As seen from the Phase Coder Simplified Block Diagram of Figure 4.6-4, implementation is accomplished with a 5-bit full subtractor with end around borrow which produces an absolute difference. The end around borrow is produced whenever the minuend is smaller than the subtrahend and results

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in an output which is the compliment of the absolute difference. Using this borrow to tell whether to use the true absolute difference or the complement of the absolute difference, the phase bits T and U are obtained by combinational logic networks.

As previously mentioned, the fine phase must be divided by two before the subtraction process. This is accomplished by a binary shift in the full subtractor in which the four MSB's of fine phase are entered into the subtractor as bits 2 thru 5 of the minuend. The most significant bit of the minuend is hard wired to a binary zero. The borrow from the MSB of the subtractor is returned to the "Borrow In" input for the LSB. This is shown in both the Block Diagram of Figure 4.6-4 and the schematic for the full subtractor 4124-64004. The modules which make up the subtractor logic are Z13-Z28.

The 5 bit difference from the subtractor and the MSB borrow are used by the Phase Coding Logic (modules Z1-Z12) to generate the 2-bit coder output used by the SWI address logic. In addition a FOV inhibit is sent to the Inhibit Logic if the signal being processed is out of the FOV in either the X or Y direction. The Load Y signal is sent to the SWI address register only if the Y phase data is found to be in the FOV. Inhibit sample pulses are synchronized by the "A" timing generator in the Programmer to occur at the instant that the

FOV data has been processed. Combiner processing of the X and Y phase data is done serially.

Since Y phase data is processed first, if it generates a FOV inhibit there is no need to wait for X phase data to be processed. An Inhibit is generated immediately and processing of the signal which produced the Y FOV Inhibit is aborted. The following equations describe the logic conditions which generate FOV Inhibits.

$$\text{Y inhibit} = J_y \left[TUA_F + T'U'A'_F \right]$$

$$\text{X inhibit} = J_X \left[T'U' + TU + TU' \left(A_F B_F\right) + T'UA'_F B_F' \right]$$

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4.6.4 Space Window Index Logic

The Space Window Index (SWI) logic (Figure in conjunction with its associated memory, provides a space-oriented reference for sorting and correlating interleaved pulses from multiple emitters. Storage for the sorting operation is provided by the SWI memory, a seven plane stack of ferrite core arrays, each array consisting of 16 cores in the Y axis and 40 in the X axis. This 16 x 40 matrix represents the Field of View of the system, with each core thus representing an area equal to the resolution elements in each axis. The memory is addressed by the coded phase data from the Coder-Combiner, so that information written into the memory at a given location (given combination of phase codes) can be read out when the same phase data recur, i.e., when another pulse is detected from the same location in the Field of View. This technique permits identification of incoming pulses by relating their direction of arrival with those of preceding pulses.

The SWI memory is normally cleared at the end of each frequency step, so that multiple emitters at the same location can be resolved if their frequencies are different. If no data exists at the selected location, the pulse is defined as a first pulse from that particular emitter. This causes a "Space Window" to be generated, by writing into the memory seven data bits in each of nine addresses in a 3 x 3 array. These addresses consist of the one which was originally

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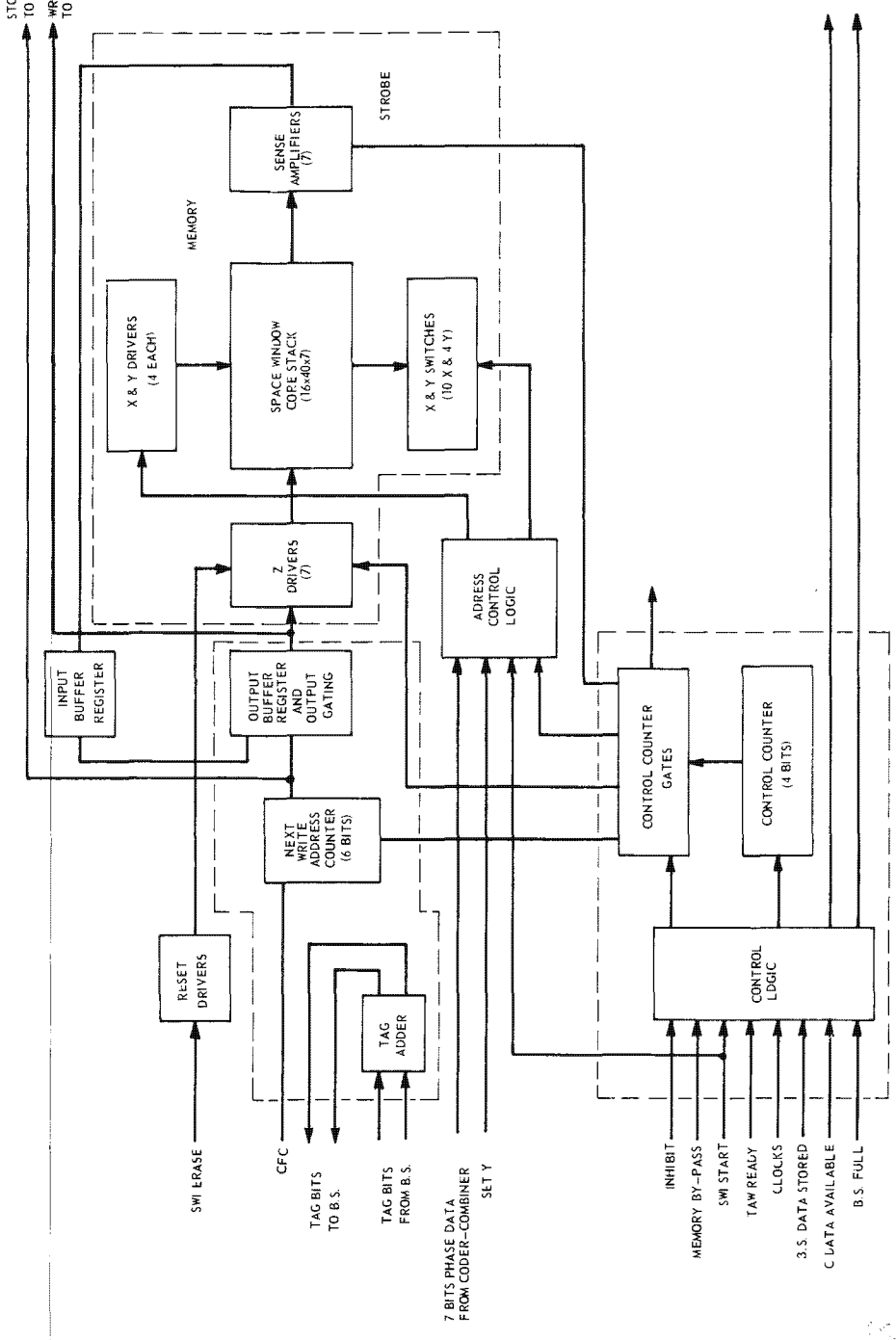

Figure 4.6- Space Window Index

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interrogated, plus the eight cores surrounding it. The purpose of the "Space Window" is to allow better correlation of data in the presence of noise, i.e., the phase codes may change slightly for successive pulses, causing any of the nine addresses to be selected, and data for these pulses will all be grouped together in the Buffer Storage Memory. The seven SWI data bits consist of a tag bit, which is always a ONE, and six bits of Buffer Storage address. These six bits define the location in the Buffer Storage which is reserved for data from the particular emitter.

When an arriving pulse causes the memory to be interrogated at an address which is part of an existing Space Window, the seventh plane will contain a ONE. This indicates to the logic that at least one other pulse has been received from the same location. The remaining six bits define the Buffer Storage address at which the previous data have been stored. The Buffer Storage memory can thus be interrogated to determine the exact number of pulses already received, and also to obtain the data necessary for computation of Pulse Repetition Interval (PRI).

The SWI logic section is bypassed for Time-Attitude Words (TAW's) and in the Memory By-Pass Mode. In these modes, a Load Command is sent immediately to the Buffer Storage, and the memory interrogation and space window generation routines are not employed.

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[redacted] The SWI logic consists of two complete logic assemblies in the data handler, plus one side of a third. The major logic groups are the Control Logic, the Memory Address Logic, and the Buffer Storage Address and Tag Logic. The core memory and its drive and sense circuits are discussed in detail in Section

4.6.4.1 SWI Control Logic

The SWI Control consists of a four-bit Control Counter, associated decoding gates, and logic for accepting and generating the various commands and control levels. The logic is synchronized by the 250 KHz output of the System Clock, producing a basic clock interval of 4.0 microseconds.

Receipt of a "TAW Ready " signal from the Programmer initiates a Load sequence. (See Flow Chart of Figure). The TAW flip-flop in the Control Logic is set to state $(30)_4$(quadral notation). If in the Memory By-Pass Mode, this produces a Load Command to the Buffer Storage. If the system is in normal mode, a "READ" signal is sent to the Next Write Address Counter (NWAC), sampling its outputs and advancing the count by one. At the end of the clock cycle, the Control Counter advances to $(31)_4$, generating a Load Command and disabling the clock line to the Control Counter.

At the completion of the Buffer Storage Load routine, a "Data Stored" indication is received. This causes a C_{xy} signal to be generated which initializes all buffers in

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the control logic and control counter, and initiates a System Reset in the Programmer Logic.

When processing intercept data (see Waveforms of Figure 4.6), the SWI logic sequence is initiated with a SWI START pulse. The READY flip-flop in the Control Logic is then set within 4 microseconds. On the next clock cycle, a R_{xy} enable will be generated in the Control Counter gating and sent to the Address Control Logic to enable reading of the SWI location specified by the encoded phase data.

At the completion of the "Read xy" cycle, the Control Counter advances to state $(01)_4$, and the tag read from the seventh plane of the SWI memory is examined.

If the tag is zero and the Buffer Storage is not full, the Control Counter remains in state $(01)_4$. If the tag is zero and the Buffer Storage is full, the Control Counter is preset to state $(23)_4$.

Assuming that the SWI tag is zero and the Buffer Storage is not full, a Read pulse is produced to sample and advance the Next Write Address Counter (NWAC), and a series of Read-Write pulses is produced to "paint" a "Space Window" around the SWI memory core which is at the x and y co-ordinates for the source being processed. This "Space Window" is a 3 x 3 array of cores in each plane. The position of this 3 x 3 array in the 16 x 40 core SWI Memory plane coincides with the emitter location in the 32 x 80 code (fine phase)

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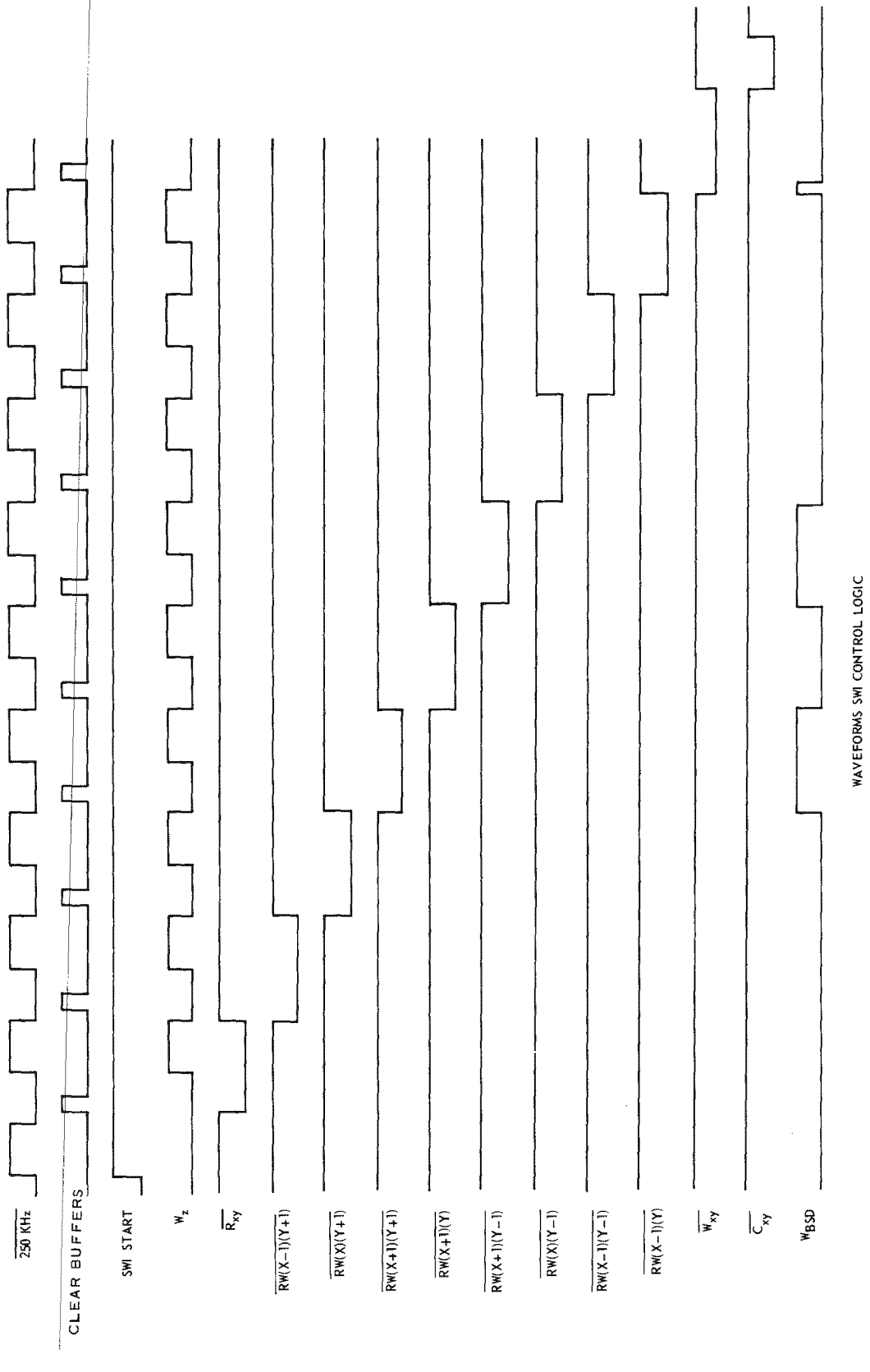

Figure 4.6- SWI Control Logic Waveforms

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field of view. Thus, each time a signal is received from a particular emitter, the same "space window" will be interrogated in the SWI. The dimension in the three-dimensional SWI memory array contains the 6-bit Buffer Storage Address where data about a particular source is located, and a 1-bit tag which is set to a ONE for the first and subsequent pulses from a given source during a specified dwell period (frequency step). In this way the SWI memory translates field of view location to Buffer Storage Address. The Buffer Storage contains two additional tag bits which are updated with each pulse processed, to provide the sub-word address for 1st, 2nd, 3rd, and 4th pulse data. Each data word (TAG Word) is a composite of the data obtained during one dwell period, data being added for each pulse up to the fourth. Pulses after the fourth in a given dwell are disregarded as far as writing additional data is concerned.

The sequence of Read-Write enable pulses required to write the space window, and the Control Counter states where they occur are shown in Table

TABLE

Read-Write Enable	Control Counter State
$(x-1)(y+1)$	$(01)_4$
$(x)(y+1)$	$(02)_4$
$(x+1)(y+1)$	$(03)_4$
$(x+1)(y)$	$(10)_4$
$(x+1)(y-1)$	$(11)_4$
$(x)(y-1)$	$(12)_4$
$(x-1)(y-1)$	$(13)_4$
$(x-1)(y)$	$(20)_4$

After the "Space Window" has been "painted in the SWI memory, the Control Counter advances to state $(23)_4$. This generates a Write (X) (Y), storing the seven bits of data in

the originally interrogated cores.

The Control Counter then advances to state $(30)_4$, generating a clear signal, which resets the X and Y address registers, the Z register, and the DATA and READY flip-flops in the Control Logic. Reset of the READY FF generates resets for the four Control Counter Stages. This returns the counter to state 0, and the SWI logic is prepared to receive a new command. The Clear pulse also initiates System Resets.

If the Buffer Storage Full indication had been present, the Control Counter would have been set directly to state $(23)_4$, as discussed above. In this situation, the action of generating Write (X) (Y), and all subsequent steps, proceeds exactly as discussed in the preceding paragraphs.

If the seventh plane of the memory had contained a ONE when location (X)(Y) was interrogated (Control Counter in states 0 and 1), it would indicate that the selected location was a part of a previously generated space window. In this case, the remaining six planes will contain the Buffer Storage memory address in which the previously obtained information is stored. The Control Logic will detect that the SWI Tag at location XY is a ONE and will generate a Buffer Storage Interrogate Tag Command when the Counter advances to $(01)_4$.

This command causes the Buffer Storage Logic to read the tag sections (see Paragraph 4.6.8) of the address defined by the six bits read from the SWI memory. These sections contain seventeen bits of FTOA information for PRI computation,

plus two tag bits which define the number of pulses already received from this particular space window. The decimal equivalent of the two-bit binary number is equal to one less than the number of pulses already received, e.g., a 10 condition (decimal 2) indicates that three pulses have been received, etc.

When the Buffer Storage has completed readout of the tag section, it generates a "C Data Available" indication. If the two tag bits are both ONE, indicating that data concerning four pulses have already been stored, the Control Counter is preset to state $(23)_4$. This produces a Write (X)(Y) and a return to a Ready State, as discussed above.

If the tag bits are not both ONES, a Load Command is generated to store the data concerning the received pulse in the Buffer Storage memory. On receipt of the Data stored indication, the Control Counter is preset to state $(23)_4$, and the remainder of the sequence proceeds as described above.

4.6.4.2 Memory Address Logic

The SWI memory addressing logic performs the function of decoding the phase data to select the appropriate drive lines for the core memory, then producing enables for the selected lines with the correct timing and pulse width. The memory is a conventional coincident current type with selection being performed at both ends of the drive wires. This requires that two driver circuits (one source and one sink) be selected and enabled for each axis. For this discussion, a source will

be designated as a driver, and a sink will be designated as a switch.

For Y axis selection of switches and drivers, only the four MSB of the five bits of fine phase data are used, along with an enable pulse (set Y). Set Y samples the data lines, storing the states in the four RS flip-flops. The outputs of the flip-flops drive the decoding logic which energize the memory drivers and switches. Outputs from the Control Counter gates perform the addition and subtraction enables to the addressing logic as the Space Window is written.

The outputs which are selected for the various combinations of input codes are shown as follows (assuming enable of (X)(Y), either Read or Write):

INPUT				OUTPUT #1		INPUT				OUTPUT #1	
2^4	2^3	2^2	2^1	Driver	Switch	2^4	2^3	2^2	2^1	Driver	Switch
0	0	0	0	1	1	1	0	0	0	1	3
0	0	0	1	2	1	1	0	0	1	2	3
0	0	1	0	3	1	1	0	1	0	3	3
0	0	1	1	4	1	1	0	1	1	4	3
0	1	0	0	1	2	1	1	0	0	1	4
0	1	0	1	2	2	1	1	0	1	2	4
0	1	1	0	3	2	1	1	1	0	3	4
0	1	1	1	4	2	1	1	1	1	4	4

The above relationships are modified when any function involving (Y$\pm$1) is enabled. This modification can

be visualized as simply adding or subtracting one bit from the four-bit address code shown in the table. One bit is added during (Y+1) functions, and one bit is subtracted during (Y-1). For example, a code address of 0011 (decimal 3) would select Driver #4 and Switch #1, during (Y) functions. During (Y+1) functions, however, this code would select Driver #1 and switch #2, i.e., the same selection as would result from an input code of 0100 (decimal 4) during (Y) functions. This code address would select Driver #3 and switch #1 during (Y-1) functions.

The four-bit buffer register is reset at the completion of a processing cycle by a Clear signal from the Control Logic.

The portion of the X addressing between -360° and 0° is similar to that described for the Y axis (-180° to +180°). The discussion of the decoding technique for the Y axis is applicable to this portion of the X axis also, with all X and Y designations interchanged. The main difference here is that the 2 MSB of the 7-bit FOV address are used for X and not used for Y. Also, the input at Bit 5 is inverted for the Y axis, and not for the X axis, and the switch designations shown in the table as 1 through 4 are changed to 2 through 5, respectively, for the X axis.

The remaining portion of the X-axis selection logic is addressed differently than for Y. This logic uses

[redacted]e four most significant bits of the encoded phase data, consisting of the two MSB's of the fine phase, plus two additional bits generated by the Coder-Combiner, which indicate the proper quadrant of the field of view. A discussion of the generation and significance of these bits is included in the Coder-Combiner section, para. 4.6.3.

The four-bit address register in this logic is set by Set X and cleared by Clear (X)(Y), as was the case for the four-bit buffer for the other portion of the X addressing.

Four OR gates are included in this logic for combining the outputs of this logic with that of the other X selection logic. These are necessary in that enables for switches 2 and 5 may be generated by either set of logic and they must be combined to cover the FOV.

The outputs of this portion of the addressing logic, for all combinations of input data, are shown in the following table:

TABLE SWI ADDRESSING LOGIC (X FUNCTIONS)

INPUT 2^6 2^5 2^4 2^3	OUTPUT	INPUT 2^6 2^5 2^4 2^3	OUTPUT
0 0 0 0	S6	1 0 0 0	-
0 0 0 1	S7	1 0 0 1	-
0 0 1 0	S8	1 0 1 0	-
0 0 1 1	S9	1 0 1 1	S1
0 1 0 0	S10	1 1 0 0	*
0 1 0 1	--	1 1 0 1	*
0 1 1 0	--		
0 1 1 1	--		

[redacted]

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The dashes indicate invalid code combinations, and the asterisks indicate codes for which the selection gates in the other portion of the logic are enabled. These states are valid only when (X) functions are involved. For (X+1) and (X-1) functions, the logic is modified to effectively add or subtract one bit from the actual phase code. For (X+1) functions, the following table applies

TABLE SWI ADDRESSING LOGIC (X+1 FUNCTIONS)

INPUT 2^6 2^5 2^4 2^3	OUTPUT	INPUT 2^6 2^5 2^4 2^3	OUTPUT 0
0 0 0 0	S7	1 0 0 0	-
0 0 0 1	S8	1 0 0 1	-
0 0 1 0	S9	1 0 1 0	-
0 0 1 1	S10	1 0 1 1	-
0 1 0 0	-	1 1 0 0	-
0 1 0 1	-	1 1 0 1	-
0 1 1 0	-	1 1 1 0	-
0 1 1 1	S2	1 1 1 1	S6

The outputs for the (X-1) functions are shown in the following table:

TABLE SWI ADDRESSING LOGIC (X-1) FUNCTIONS)

INPUT 2^6 2^5 2^4 2^3	OUTPUT	INPUT 2^6 2^5 2^4 2^3	OUTPUT
0 0 0 0	S5	1 0 0 0	-
0 0 0 1	S6	1 0 0 1	-
0 0 1 0	S7	1 0 1 0	-
0 0 1 1	S8	1 0 1 1	-
0 1 0 0	S9	1 1 0 0	S1
0 1 0 1	-	1 1 0 1	-
0 1 1 0	-	1 1 1 0	-
0 1 1 1	-	1 1 1 1	-

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4.6.4.3 Buffer Storage Address and Tag Logic

The balance of the SWI logic consists of a six-bit ripple counter, a seven-bit buffer register, a six-bit output buffer logic for updating the Buffer Storage tag bits, and gating to provide enable pulses for the inhibit (Z axis) drivers in the SWI memory.

The six-bit counter is reset only by the initial reset (RSI delayed) from the Programmer and is advanced by the Read NWAC pulse. This pulse is normally at ground, and, when it becomes high, the present state of the counter is transferred via six NAND gates into the six most significant bits of the output buffer register. The outputs of this register provide the Buffer Storage with the correct address for storage of information.

As discussed above, generation of a Read NWAC indicates that a pulse from a previously undetected emitter is being processed, or that a TAW is being stored. The NWAC state defines the next unused address in the Buffer Storage memory, so that the transfer of this address into the six bits of the output buffer register conditions the Buffer Storage to store the new data in that address. When the Read NWAC returns to ground, the six-bit counter is advanced one step, thus placing it in the proper state to define the next unused Buffer Storage address.

The contents of the NWAC are sampled at each

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Change Frequency Command (CFC). The address thus sampled, and sent to the Buffer Storage logic, defines the first Buffer Storage address which will be used during the next frequency step. This is used by the Buffer Storage to stop the transfer of data from the core memory to the Core Storage Unit, and the address is defined as the Stop Readout (SRO) address. Details of this operation are included in the Buffer Storage logic discussion.

When the SWI memory is interrogated, the contents of the selected address are placed in the seven-bit input buffer register. A ONE in the seventh (tag) plane results in a ONE indicating that pulses have been previously detected from the selected coordinates (see Para. 4.6. . The remaining six bits define the Buffer Storage address which was used for storage of the previous pulse data, and condition the buffer storage logic for Tag Interrogation and storage of new data.

Writing of the seven bits into the memory is controlled by the inhibit driver gates. Inputs to these gates are from the output buffer for Tag equal zero and from the input buffer for Tag equal ONE. These gates are enabled by a Write Z pulse from the Control Logic, and produce a ground-true inhibit pulse to the memory drivers for each bit which is a ZERO. The output buffer register is reset at the completion of the processing cycle. Input Buffers are reset after each Write pulse and before the next Read pulse.

The inhibit driver for the seventh plane is normally disabled by the Buffer Storage Full level so that a ONE is written into this plane on every Write cycle. If the Buffer Storage is full, however, data concerning new emitters cannot be accepted. In this case, the seventh plane is written with the same logic state which was read out.

The Tag Logic performs the addition of one to the tag bits read from the Buffer Storage. For a first pulse from a given location, the seventh plane register stage will contain a ZERO, thus causing the two tag bit outputs to be ZERO. For subsequent pulses from the same emitter, the tag bits follow the relationship shown below:

INPUT		OUTPUT	
MSB	LSB	MSB	LSB
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

If both input tag bits are ONEs, this indicates that four or more pulses have already been processed from the same location.

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4.6.5 Inhibit Logic

The purpose of the inhibit logic is to keep the data handler from reading out erroneous information. This is accomplished by using the inhibit and confirm signals generated in the IF assembly in conjunction with inhibits generated within the data handler. It is desirable to have the capability of disabling one or all the inhibits and confirms. This is accomplished by the use of Relay Commands which are controlled from the ground. Table gives a description of the inhibit and confirm signals and the commands which disable them.

4.6.5.1 Theory of Operation

The logic (see Figure 4.6-) is designed to receive all confirm signals and no inhibit signals at the inputs to the buffers, or an inhibit will be generated. In other words, if any one of the four confirm buffers has not been set, or if the inhibit buffer has been set by any one of the three inhibit signals (when the "Inhibit Enable" buffer is set), an INHIBIT will be generated.

The "Inhibit Enable" buffer is set by (55), the fifth coder combiner sample pulse. This allows approximately five microseconds after leading edge of the intercept signal for all Inhibit/Confirm signals to be received from the IF, which is very adequate. If an inhibit is generated at this time, further processing is aborted, and a system reset is generated to clear all buffers.

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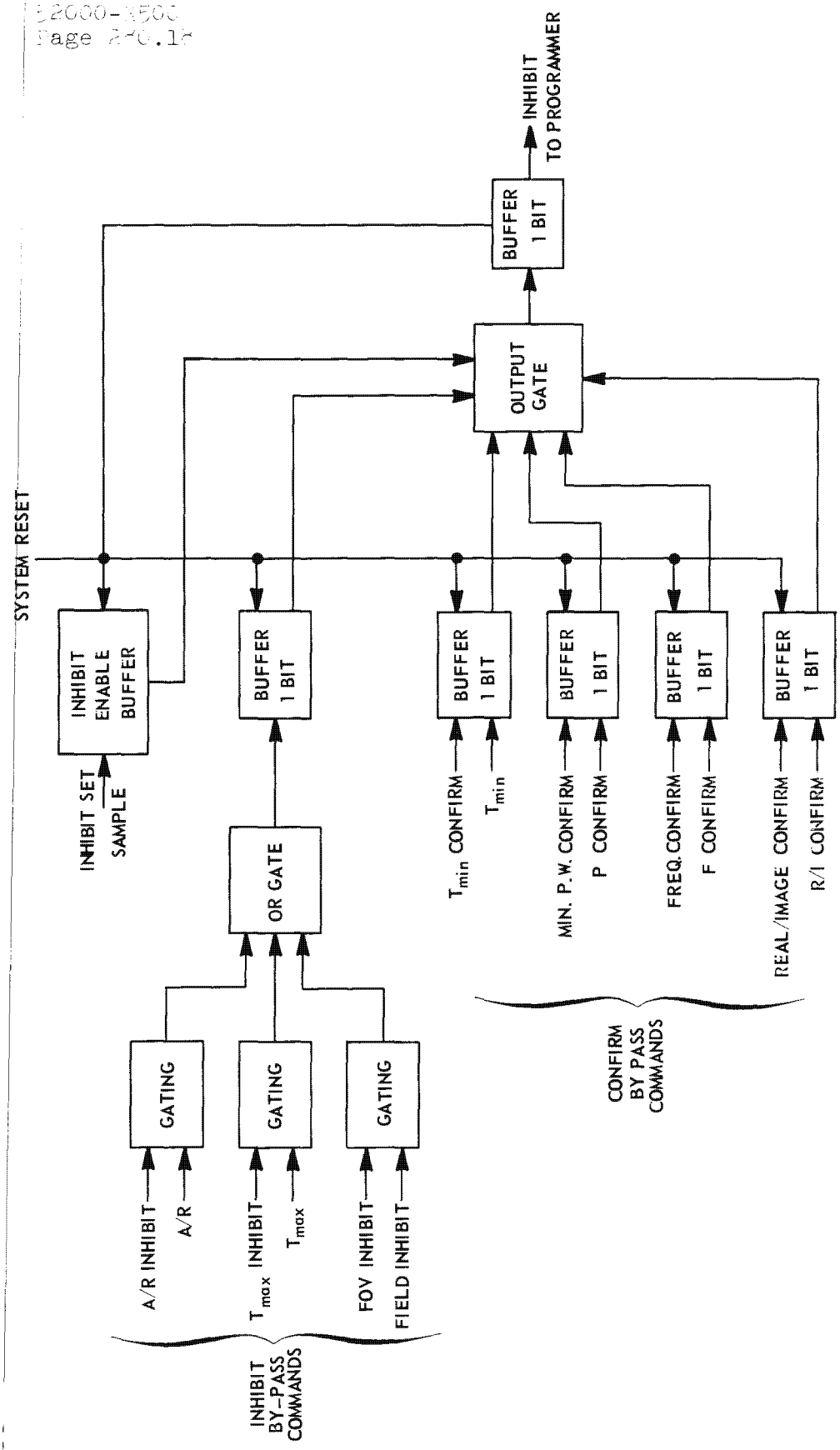

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TABLE 4.6-

INHIBIT AND CONFIRM SIGNALS

INHIBIT/CONFIRM	SOURCE	PURPOSE	RELAY COMMAND TO DISABLE INHIBIT/CONFIRM
Amplitude Ratio Inh.	I.F.	F2/C 4 db = Inhibit F2/C 0 db = No Inhibit	A/R Inhibit
*Tmax Inh.	I.F.	Inhibits if the Signal level at antenna is greater than -53 dbm	Tmax
*Tmin Conf.	I.F.	No Confirm if signal level at antenna is below -93 dbm @ 23° off boresight	Tmin
Freq. Conf.	I.F.	No Confirm if I.F. frequency is not 20 Mc ±1.5 Mc	F Conf.
Field of View Inh.	D.H.	Inhibit if emitter location is outside the FOV	Field Inh.
Min. Pulse Width Conf.	I.F.	No Confirm if pulse width of signal is less than 0.4 usec	P Conf.
Real/Image Conf. Nominal at minimum threshold	I.F.	No Confirm if the signal is not 20 Mc above or below the L.O.	R/I Conf.

* Subject to threshold level change

If no inhibit and all confirms are received from the IF, the system will continue to process until a field of view inhibit is received (in either the X or Y dimension) or processing is complete.

One point should be made clear at this point. If an inhibit is generated it does not cause a system reset until the trailing edge of the pulse being processed. The generation of the inhibit does stop further processing, however. In this way, if a CW source is received, the system will wait until the end of the 24 microsecond period (which identifies CW) to generate the system reset. This allows identification of the CW source, even though it may produce inhibits, and allows the system to process other signals in the presence of such a CW source, if they are of sufficient amplitude.

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4.6.6 Programmer

Operation of the System Programmer is described in Flow Chart form in section . The various sections of the programmer are: The "A" Timing Generator, System Reset Generator, Programmer Control Logic, and the Delay and Dwell Timers. Detailed operation of the hardware for these sections is described in paragraphs 4.6.6.1 through 4.6.6.4.

4.6.6.1 Coder/Combiner Timing Generator

It is the function of the timing generator shown in Figure 4.6- to provide all necessary timing signals for the A/D Converter, Phase Coder, Space Window Logic, and Inhibit logic during the phase encoding operation. Inputs to the generator are the 4 MHz clock, a START signal from the Programmer and a System Reset also from the Programmer. Outputs are shown in the timing diagram of Figure .

Each time a START pulse is received, the timing generator produces a fixed series of timing pulses and then shuts down and waits for the next START pulse. The Count Control logic enables the 4 MHz clock to be gated to a four bit ring counter. Both the four bit ring counter and the ten bit SR are preset by preset drivers so that the first F/F in each register contains a logical one and all others contain logical zeroes. Using this technique the four bit ring counter outputs will be 250 nanosecond pulses occurring at a 1 MHz rate. One of the ring counter outputs provides the 1 MHz clock to the 10 bit shift register.

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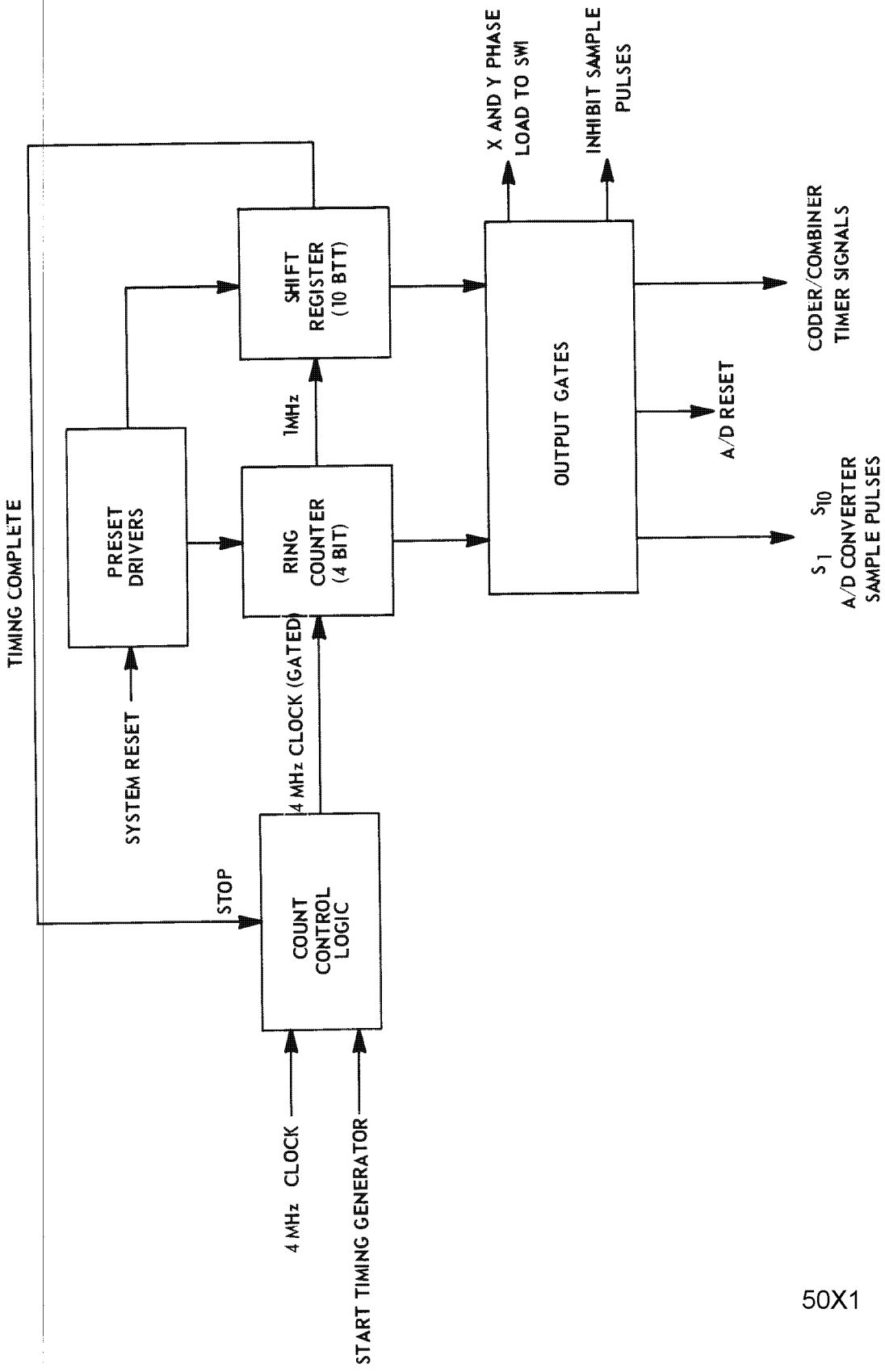


50X1

Outputs of the ten stages of the shift register will be 1.0 microsecond pulses occurring in time sequence. These outputs are used to sequentially interrogate AND gates to obtain the A/D timing pulses S1-S10. Since positive true pulses are required by the A/D converter, inverting buffers are provided. The remaining timing pulses shown in the Timing Diagram of Figure are obtained by logic operations using the register outputs. Termination of the timing sequence occurs either by interruption (SYSTEM RESET) or after all timing pulses have been generated. An interrupt of the sequence may occur as a result of any inhibit generated by the I.F. Assembly or by a Field of View Inhibit generated by the Data Handler.

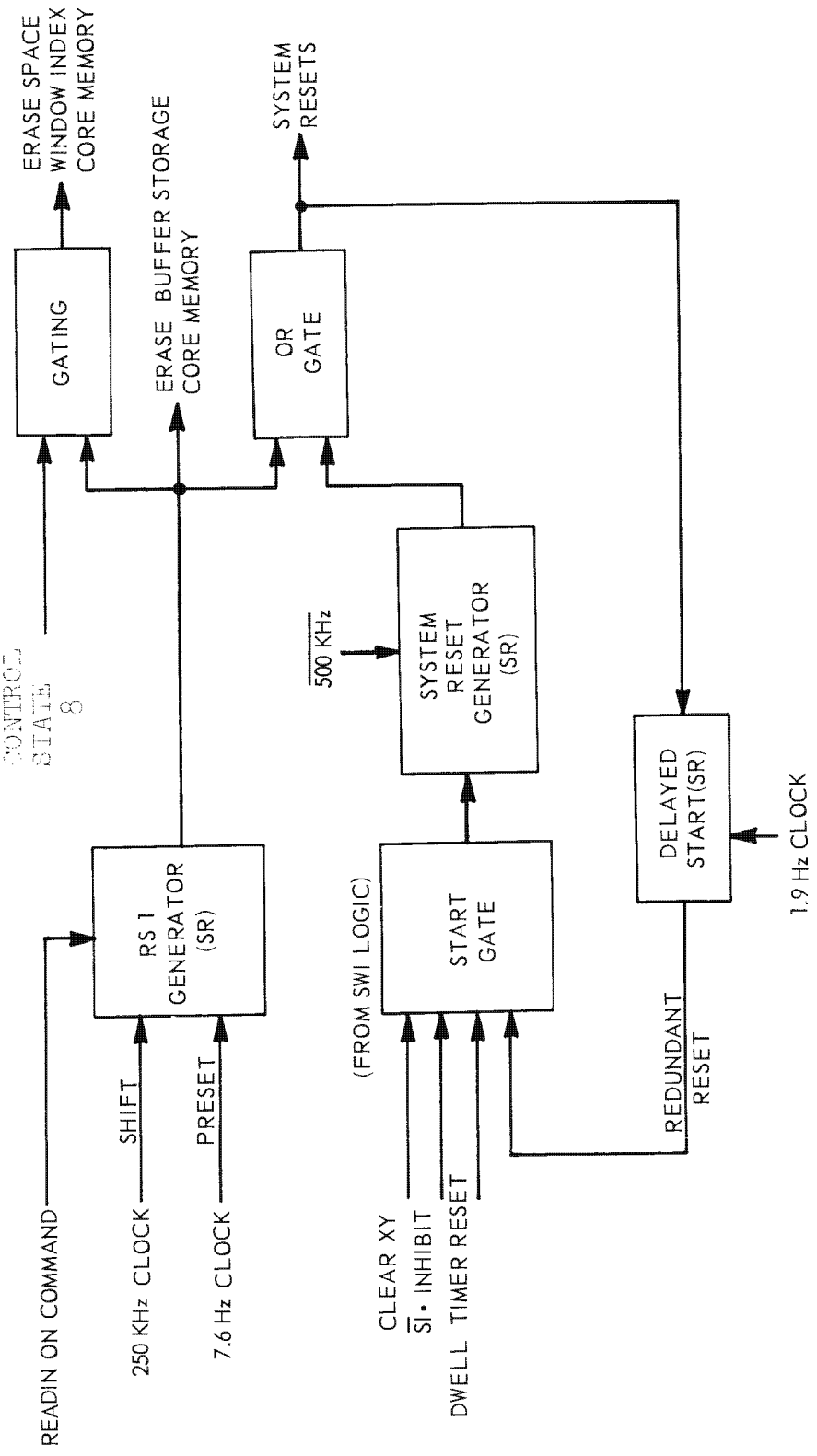
4.6.6.2 System Reset Generator

System resets are generated to clear the storage flip-flops of the system so new data can be processed. They occur under the following conditions:

1. Initial turn-on of primary power (before P/L on command is received).
2. After processing each pulse
3. When an inhibit is generated by reception of an "invalid" pulse.
4. At the end of each dwell period.
5. After 500 milliseconds if none of the above occurs.

A block diagram of the System Reset Generator is shown in Figure 4.6- .

50X1



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Timing of vehicle commands has been programmed so that there will always be a one second delay between application of primary power and issuing the readin ON command. During this interval, system resets called RS1 resets are generated to erase the Space Window and Buffer Storage core memories. These resets are 4 microsecond pulses occurring at a 7.8 Hz rate. (See Figure 4.6- .) Since the erase currents are quite large, they are time staggered to allow one cycle of the 250 KHz clock between erase pulses.

Generation of RS1 pulses is accomplished by setting the first stage of a five stage shift register to a ONE with the other four stages cleared. After the register has been preset, the logical ONE is propogated down the string with each shift pulse and logical ZEROES are shifted into the register. Resulting outputs are shown in the RS1 Generator portion of Figure 4.6- .

Normal system resets are generated by a second shift register arrangement. Here, the first stage is SET and the second stage is cleared by a START pulse. This START pulse is produced by a logical OR of the input functions (See START GATE inputs on Figure 4.6-). Thus, a normal System Reset is produced on the next positive transition of the 500 KHz clock after the start pulse. The SWI memory is erased after every CFC as well as during RS1. Therefore, an OR gate is provided to produce this function.

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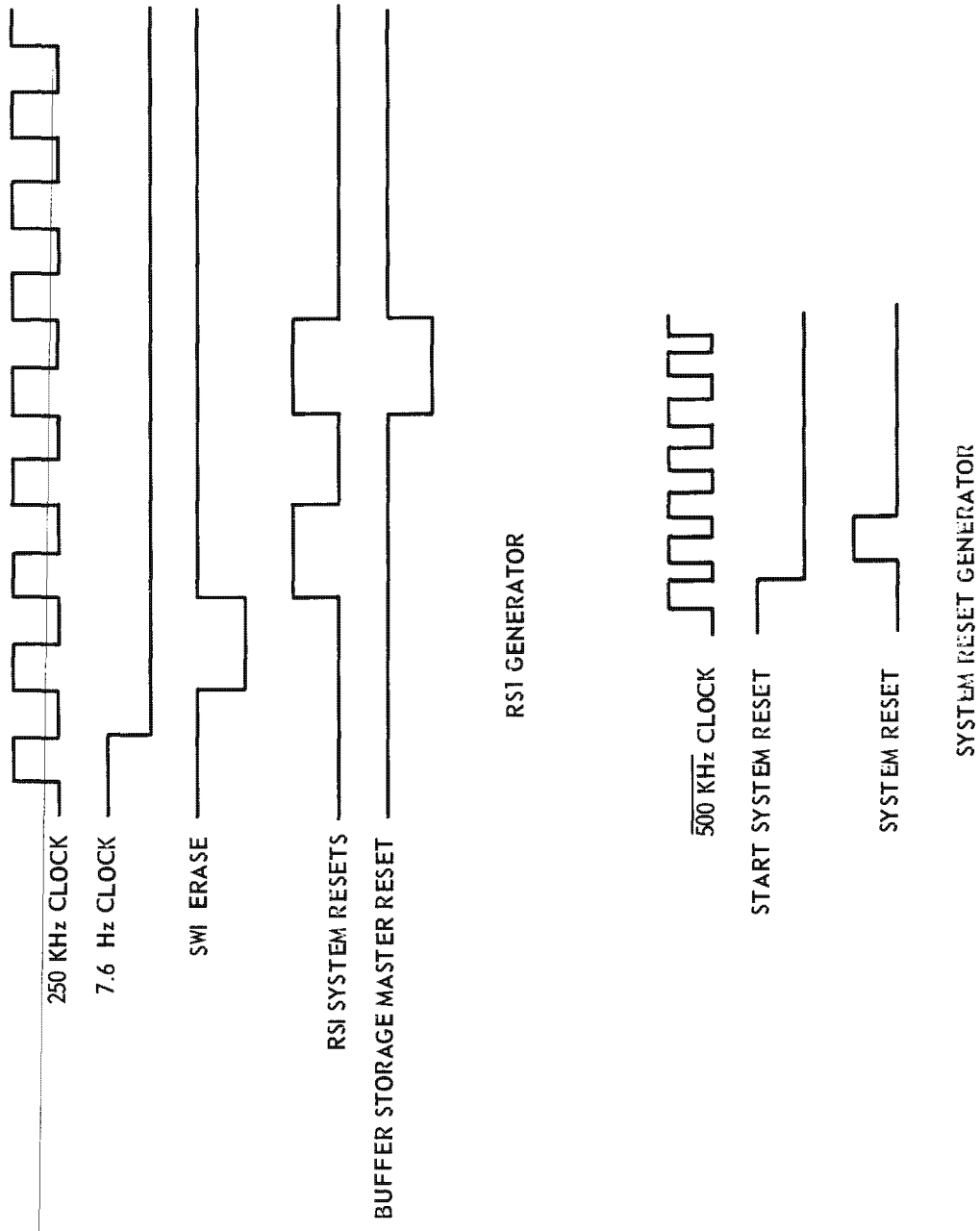


50X1

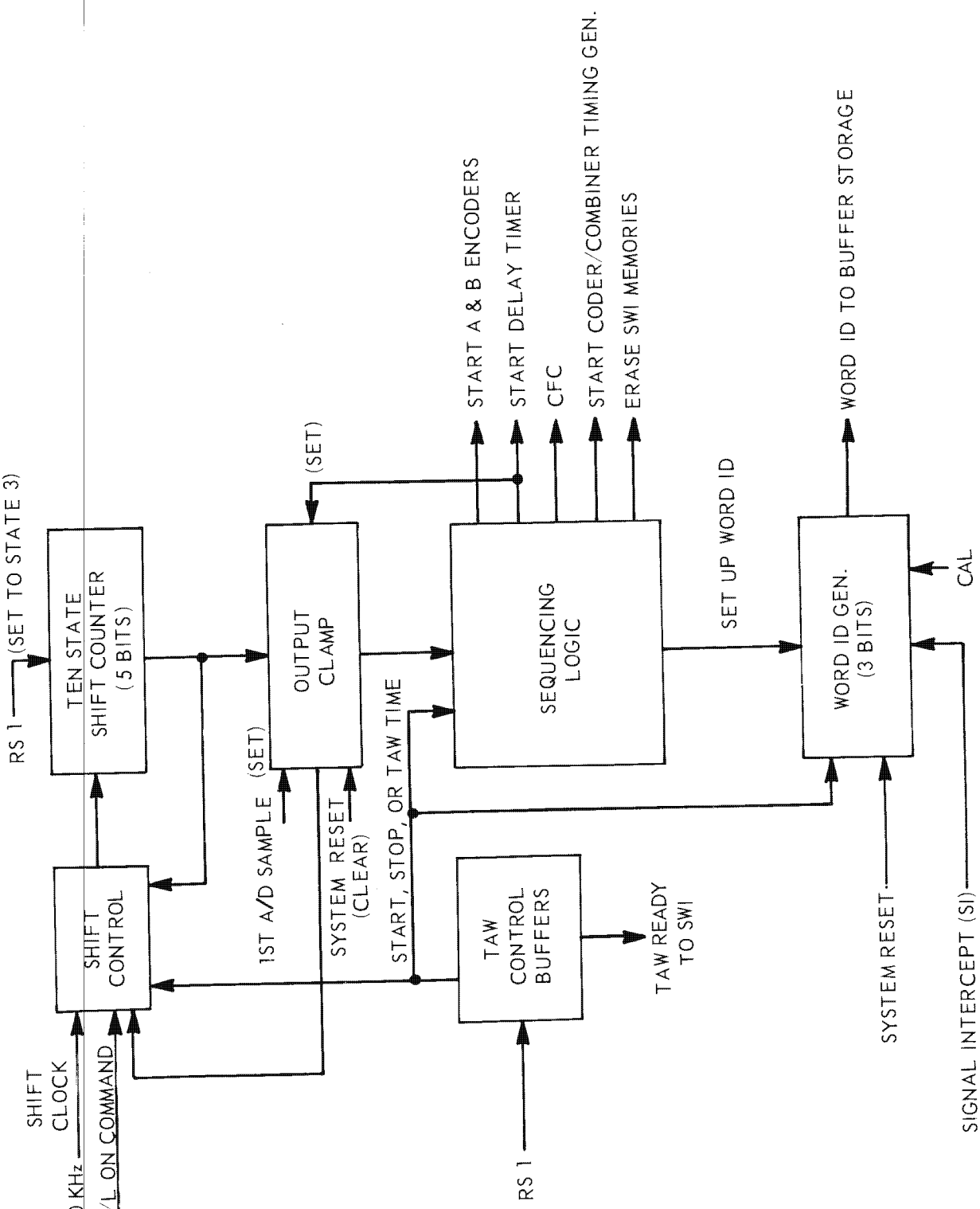
4.6.6.3 Control Logic (Programmer)

This logic provides a direct implementation of the Programmer Control routine as shown on the block diagram of Figure 4.6- . The ten state shift counter the sequencing logic, TAW control buffers and the word ID generator keep track of the type of data being processed and initiate operation of various measurement and timing devices during the processing cycle. The ten state shift counter logic contains ten gates which determine when the counter is to be shifted to the next state by the 500 KHz clock. When a pause is required in the control routine to perform some function such as to write a TAW (Start delay timer) or process an intercept, (1st A/D sample) the output clamp effectively holds the control counter outputs to control state zero until the processing is complete. At this time a system reset releases the clamp.

The TAW control buffers enable gates in the sequencing logic to set the word ID generator on TAW words, and to start the delay timer and pitch and roll (A & B) encoders.

The word ID generator contain the three bits of data which, when modified by the buffer storage tell whether a data word contains a TAW word or intercept word according to Table 4.4-5.

50X1



50X1

TABLE 4.4-

WORD IDENTITY GENERATOR

CODES			WORD IDENTITY
0	0	0	Calibrate Intercept (1,2,3, or 4 pulses)
0	0	1	One Pulse Normal Intercept (Memory By-Pass Mode)
0	1	1	Two Pulse Normal Intercept
1	0	1	Three Pulse Normal Intercept
1	1	1	Four Pulse Normal Intercept
0	1	0	Stop
1	0	0	Start
1	1	0	Time-Attitude (or Status)

4.6.6.4 Delay and Dwell Timers

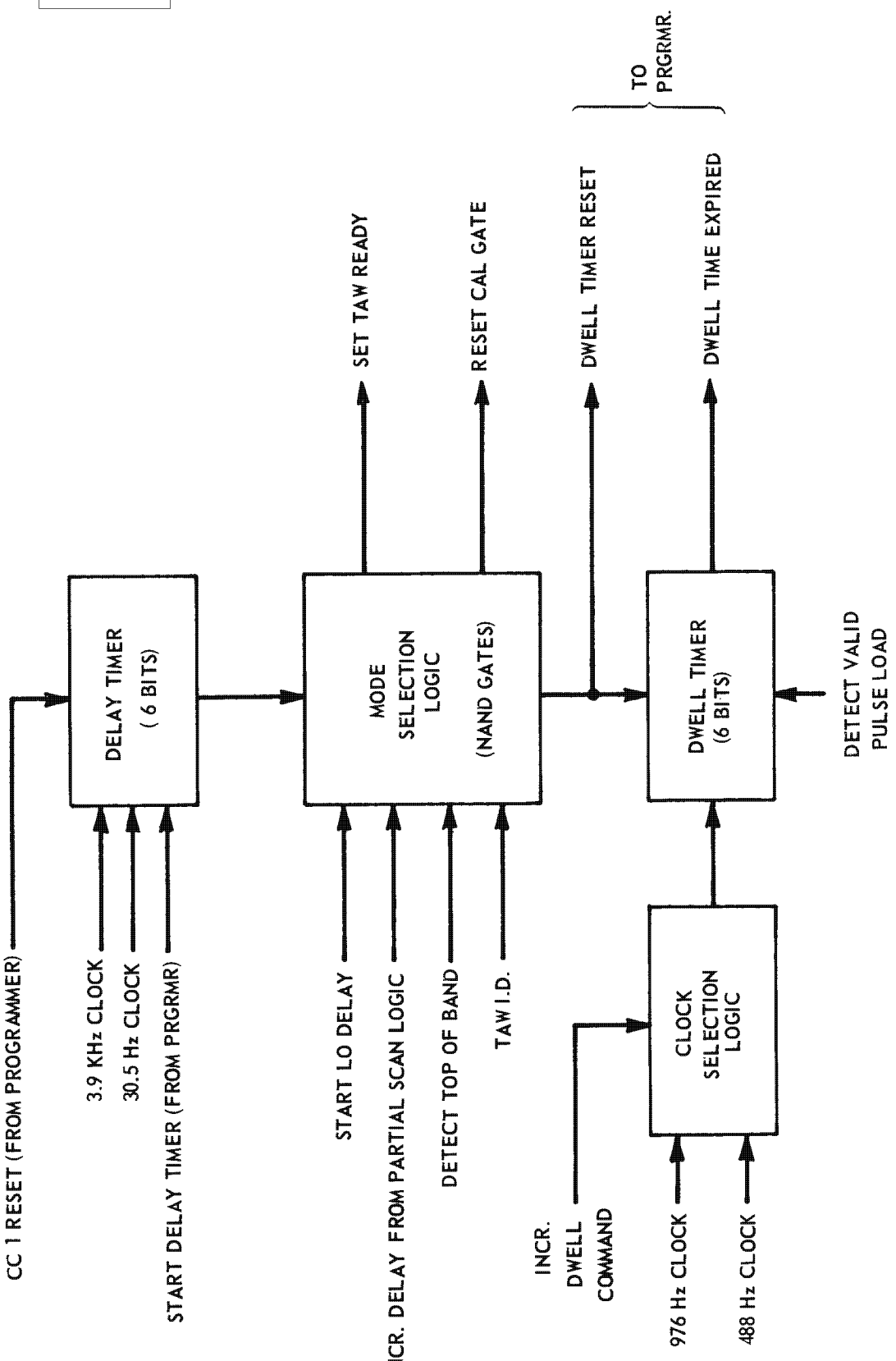
The function of the Delay Timer is to provide either 2, 4, or 262 millisecond delays for use by the system Programmer. The 2 millisecond delay is used only to allow a settling time for the Local Oscillator when a "normal" frequency change is made. The 4 millisecond delay is used for the following:

1. Attitude encoding
2. Calibrate pulses being generated

The 262 millisecond delay is used when going from the high end of a frequency band to the low end of a band, or,, when operating in partial scan and going from the upper end of partial band to the low end of a partial band.

A block diagram of the Delay and Dwell Timers is shown in Figure 4.6- . The Delay Timer is a six stage ripple counter. Output of the last stage is used to block clock pulses whenever it is a logical ONE. In this state, no further counting is done until a START pulse is received which clears the last stage of the ripple counter, and removes the inhibit on the clock line.

NAND gates in the Mode Selection Logic detect when the ripple counter reaches a count of 8 and 16 respectively, corresponding to a delay of 2,262 or 4 milliseconds from the START pulse. Only one of the NAND gates will produce an output for each START pulse. Neither the 2 or 262 msec LO



Delay is selected unless the start LO Delay signal is received signifying that the LO is changing frequency. Normally the 2 millisecond delay is selected except when the LO is changing from the top of a frequency band (whole or partial) to the bottom of a band. At this time a 262 millisecond settling time is required. At the end of either the 2 or 262 millisecond delay a Dwell Timer Reset is generated.

The 4 millisecond delay time is used for attitude encoding and generation of CAL pulses. The Cal Gate Reset is always generated at the end of a 4 millisecond delay. The TAW Ready signal is only generated when a TAW ID is detected.

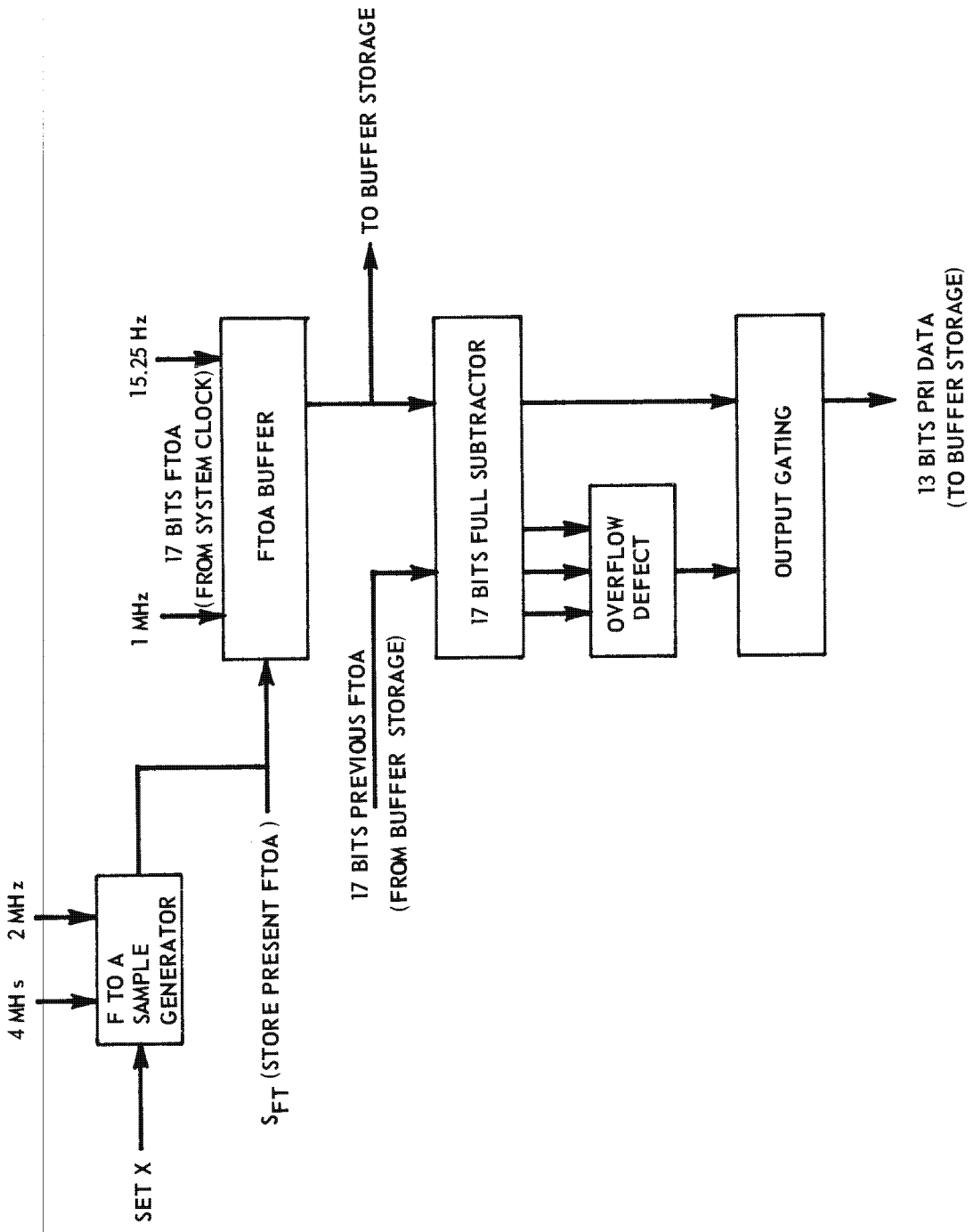
The Dwell Timer is a six stage ripple counter. Clock selection logic is provided. Normally, the 976 Hz clock is used, but the 488 Hz clock may be selected by the Increase Dwell Time command. Outputs of the last stage of the Dwell Timer indicate when the Dwell Time has expired.

50X1

4.6.7 Encoder "D" Pulse Repetition Interval (PRI)

The D encoder shown in the block diagram of Figure 4.6- , consists of an FTOA (fine time of arrival) sample generator, a 17 bit FTOA Buffer, a 17-bit full subtractor, an overflow detector, and output gating. The FTOA Buffer receives 17 bits of time data from the system clock, storing this data on receipt of a SFT command from the FTOA sample generator. This stored time is transmitted to the Buffer Storage as fine time of arrival of a pulse. The time of arrival of the last prior pulse of the same pulse train is received from the buffer storage and is subtracted from the time of arrival of the pulse being studied. The 13 bit difference from stages 2-14 is stored in the Buffer Storage core memory as PRI (Pulse repetition interval). The 3 MSB of the difference are logically OR'd together in the overflow detector, and cause the PRI to read all ZEROES if overflow occurs. Thus, the range of the PRI encoder is from 56 microseconds (minimum system processing time for a valid pulse) to 8192 microseconds, before overflow occurs. The overflow detect circuit will indicate overflow from 8.192 to 65.5 milliseconds. Since the maximum dwell period is 45 milliseconds, there can never be any "wrap-around" of the PRI encoder caused by a measured PRI greater than the overflow detect period.

50X1



50X1

4.6.7.1 FTOA Sample Generator

The purpose of the FTOA Sample Generator is to generate a narrow (250 nsec) sample pulse, synchronized to the system clock. This pulse is used to strobe system clock outputs into the FTOA buffers at such a time that none of the stages in the system clock chain is changing state. Since the highest frequency in the FTOA data is 1 MHz, the sample must be synchronized to the 2 MHz clock. The function used for the sample is 4 MHz . $\overline{2\ \text{MHz}}$. Set X . The function (Set X) occurs on the tenth coder/combiner pulse, after all confirm/inhibit decisions have been made and the pulse has been determined "valid". Thus, on the next occurrence of 4 MHz . $\overline{2\ \text{MHz}}$ the sample pulse is generated. This sample allows a propagate time through the system clock divider chain of 250 usec (from the leading edge of the 1 MHz LSB to the leading edge of the sample). At this time no counter stage should be changing. Since the first five stages of the counter are high speed flip-flops (10-20 nsec max. propagate time) and the remaining 15 stages are a single propagate shift counter, no problems can occur.

50X1

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50X1

4.6.8 Buffer Storage Logic

The Buffer Storage Logic, in conjunction with its associated memory, provides temporary storage of intercept data and payload status (Time-Attitude) information. Figure 4.6-6 shows, in greatly simplified form, the relationship between the Buffer Storage Logic and the Space Window Logic discussed in the preceding section.

A Signal Intercept (SI) or a Time Attitude Word (TAW) command initiates a storage cycle. The SWI Control Logic interrogates the SWI memory (if the storage cycle is for an intercept) to determine further action. The Buffer Storage Control Logic is then commanded to read the tag section of the address indicated, or to store data in the indicated address. In the case of a Tag Interrogate, the Buffer Storage interrogates the specified memory address, reading the tag bits to the SWI logic and the previously stored FTOA data to the PRI encoder.

Generation of a Load Command to the Buffer Storage, whether preceded by a Tag Interrogate or not, causes the logic to begin a storage routine. Appropriate input gates are enabled, and the sampled data placed in core storage. The input gates are then changed, and the new data placed in an adjacent memory area. This process continues until the correct amount of information has been stored, at which time the Buffer Storage logic generates a signal which returns the system to a "Ready" condition. The gates which are enabled on each step are deter-

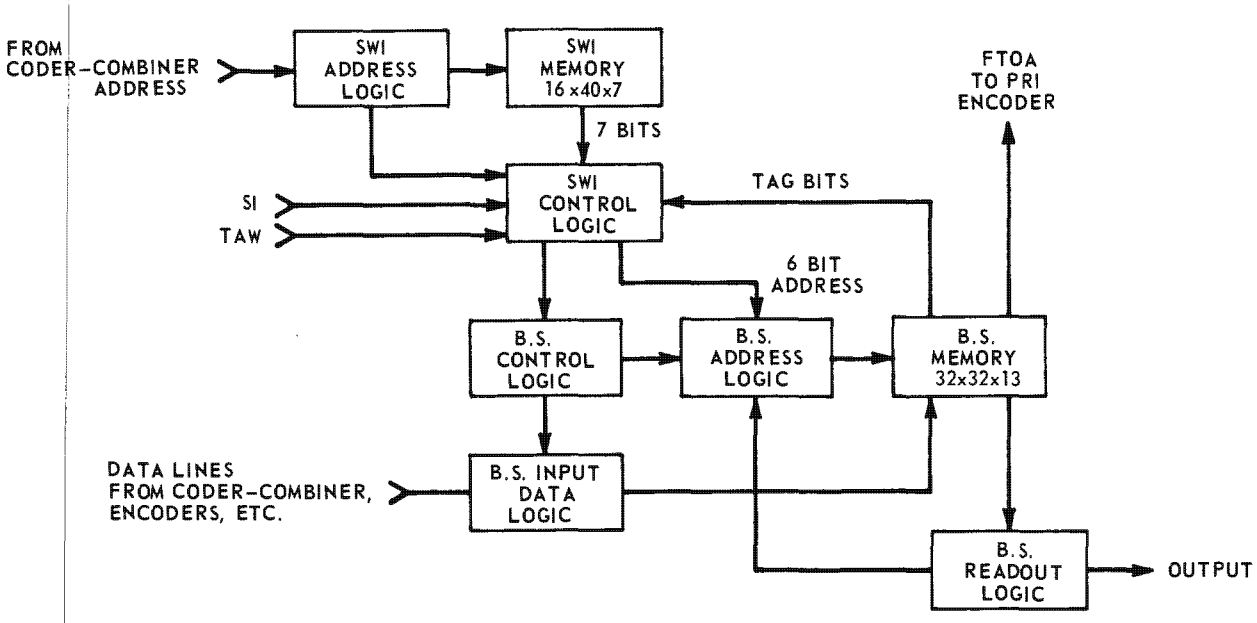

FIGURE 4.6-6 BUFFER STORAGE LOGIC BLOCK DIAGRAM

mined by the condition of the tag bits, and by the type of word (Intercept or Time-Attitude) which is being stored.

The Buffer Storage Readout Logic is enabled when a SWI erase command is generated by the programmer. The memory is sequentially interrogated, and the data read out in serial. Readout ceases when the interrogation logic reaches the last address in which valid data have been stored. New data can be accpeted and stored during the transfer operation, without degradation or loss of information.

Figure 4.6-7 shows the Buffer Storage in more detailed form. The assembly numbers shown refer to the data handler assemblies which perform the function indicated. In addition to these assembly numbers, certain minor sections of the logic are provided on assemblies A17, A18, and A24. These assemblies are shared by various portions of the system logic.

The Buffer Storage logic is synchronized by the timing pulse generator, which produces a multiphase clock, derived from the crystal-controlled System Clock. The timing logic also generates a strobe pulse for the same amplifiers in the Buffer Storage core memory.

The Command and Interface Logic forms the control interface with the SWI logic, the Programmer, and certain vehicle command lines. The Load Command, Tag Interrogate Command, and the tag bits from the SWI logic are accepted by the logic, which generates the appropriate Read, Write and

50X1

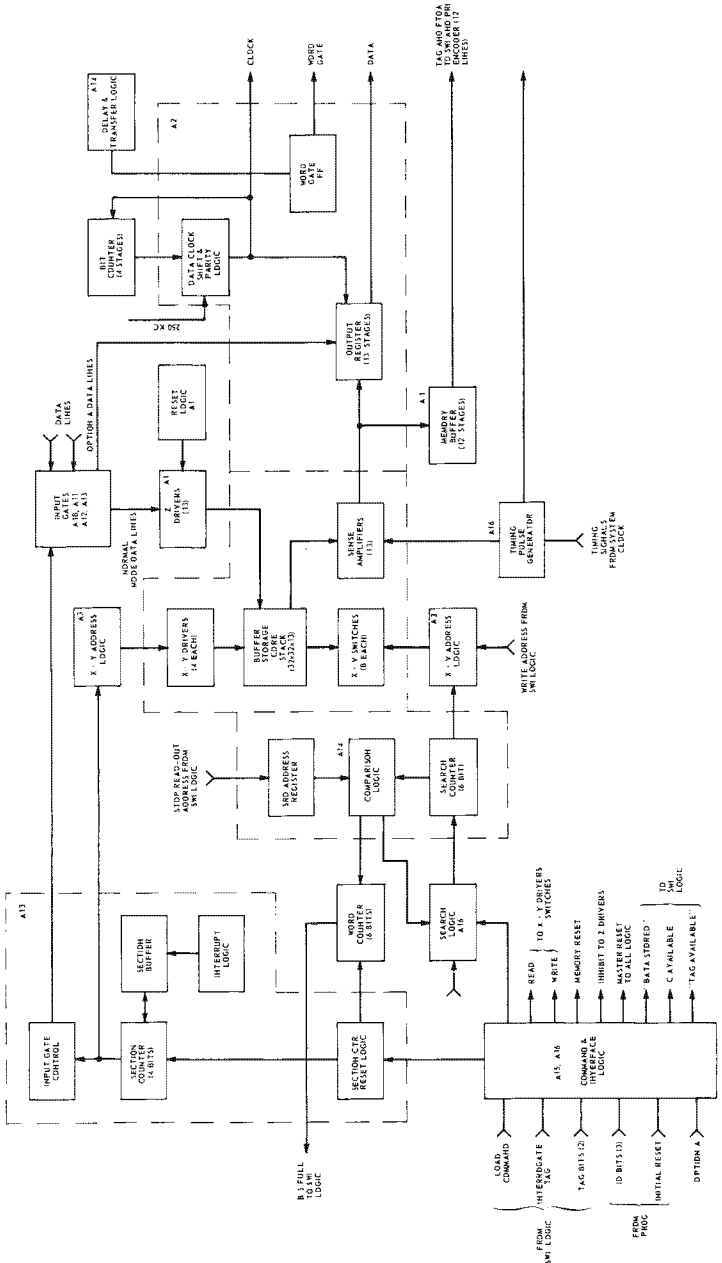

FIGURE 4.6-7 BUFFER STORAGE OVERALL BLOCK DIAGRAM

50X1

Inhibit enables to the memory selection logic. At the completion of a Load or Tag cycle, the appropriate "resume" indication (either "Data Stored" or "C Available") is generated.

The Word Identification (ID) bits are generated by the Programmer. These bits are employed both in the logic and in the output data word to indicate the type of word being generated or processed. The significance of these bits, and their translation, are discussed in paragraph . The Initial Reset is generated by the Programmer during the period between application of power and enabling of the payload. These pulses produce a Master Reset (MR) to normalize all the Buffer Storage logic, and also generate a Memory Reset which clears the core memory, magnetizing all cores in the ZERO direction. Vehicle command "Option A" conditions the logic to bypass the core memories.

The Section Counter, located on A13A, is a four bit ripple counter which controls the selection of memory drivers. The two least significant stages select one of four Y axis drivers, while the remaining two select one of four X axis drivers. This selection is accomplished by gating located on assembly A3. The Section Counter also controls the selection of input data lines, via the Input Gate Control logic, located on the B side of A13. This logic produces various control levels which enable appropriate groups of input gates at each step of the Section Counter. The Section Buffer and the

Interrupt Logic provide the capability of accepting new data during Transfer. As the Section Counter is employed during both Load and Transfer, it is necessary to return the counter to its original state if a Load interrupts a Transfer cycle. The four bit buffer stores the Section Counter state during Load, and the Interrupt Logic sets that state into the counter at the completion of the Load.

The Section Counter is preset at the initiation of the Load routine, under the control of the tag bits and the ID bits, which define the type of word being stored and the portion of the word which is currently available. The Load Subroutine Flow Diagram, Figures 4.6-8 and 4.6-9, shows the action of the preset Logic for the various combinations of tag bits.

The Input Gates, located on assemblies A10, A11, A12, and A13B form thirteen OR gates (one for each bit in the subword). These gates consist of two input (one data line and one enabling control level) NAND gates. Each of the thirteen OR gates has a selectable output arrangement. In normal mode, the outputs are routed to the memory inhibit driver logic. In Option A (Memory Bypass) mode, another set of thirteen outputs is enabled, which sets the input data directly into the Output Register. See Figures 4.6-10 and 4.6-11.

The Search Counter and associated logic are employed during the search routine to provide the six bits of memory address which are supplied by the SWI logic. See Figures 4.6-12 and 4.6-13.

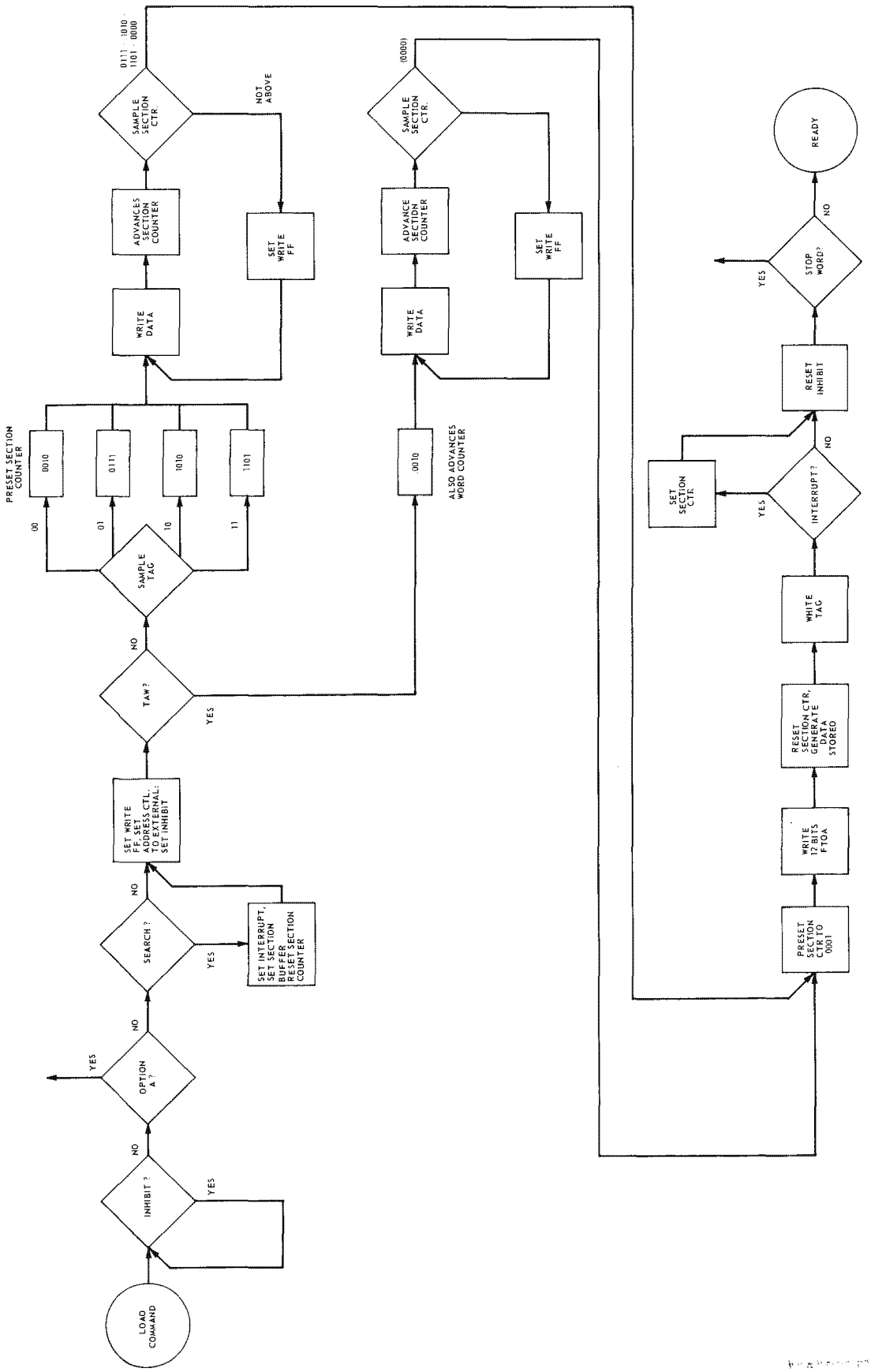

FIGURE 4.6-8 LOAD ROUTINE FLOW CHART

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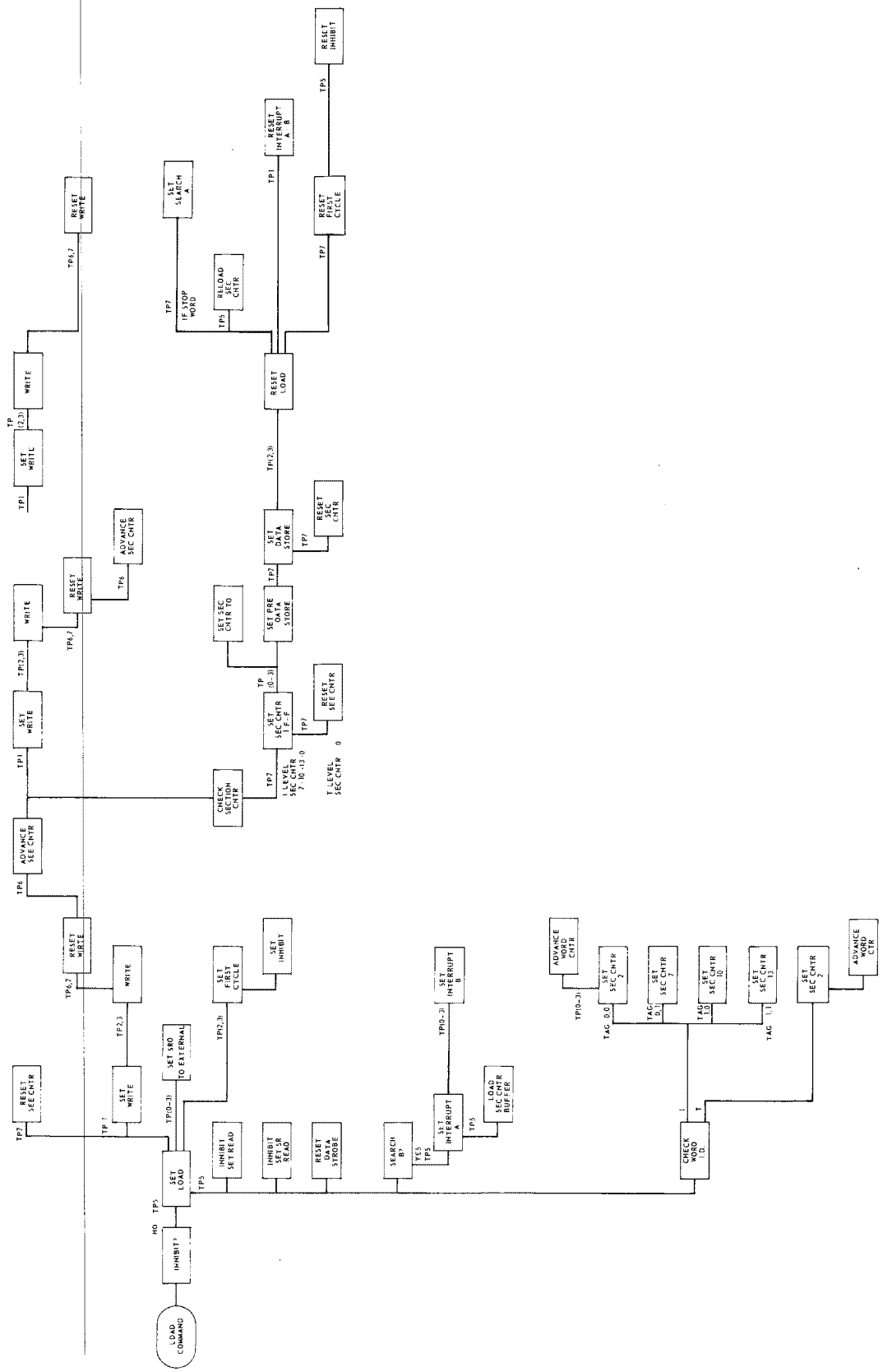

Figure 4.6-9. Load Routine Timing

50X1

50X1

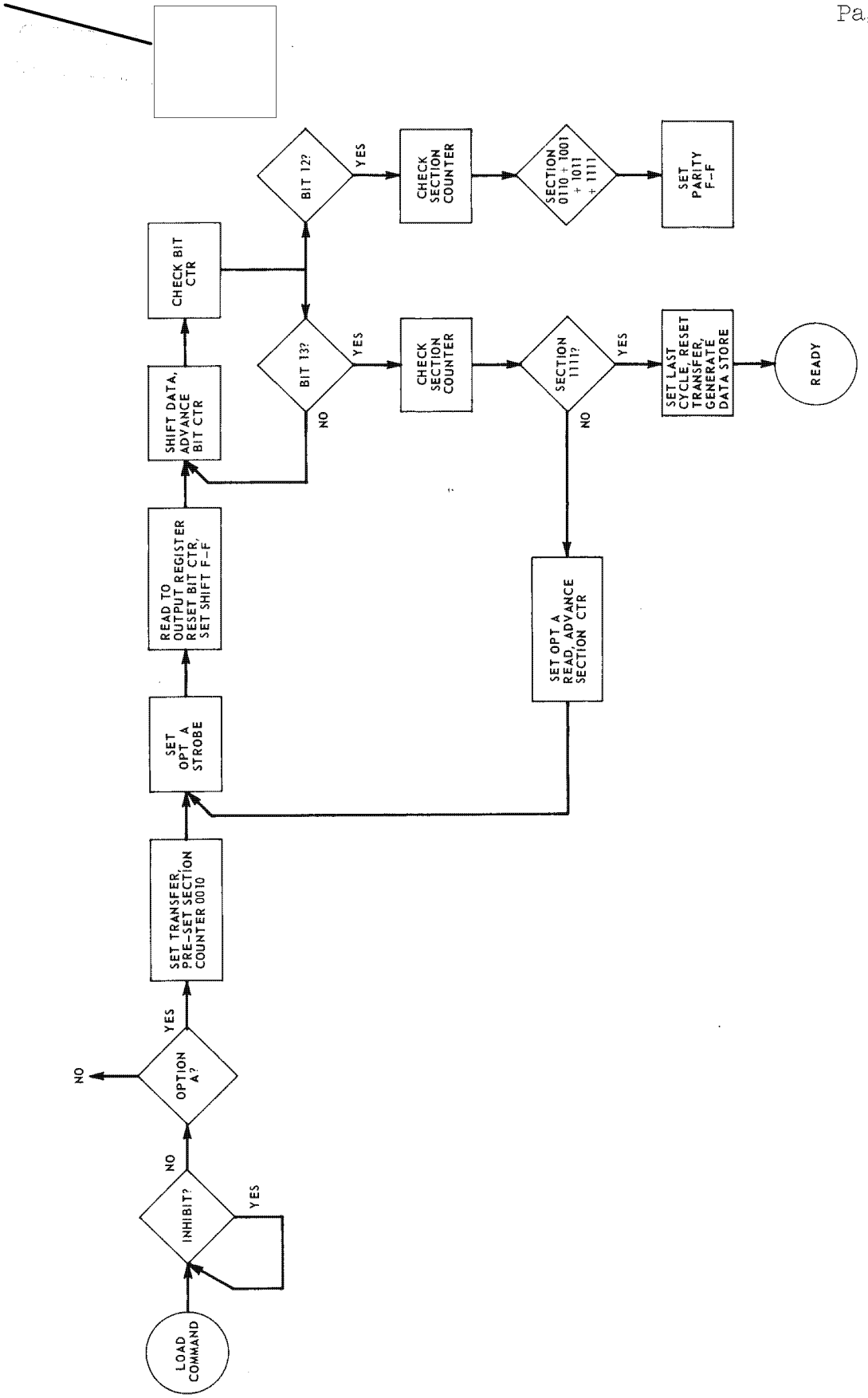

FIGURE 4.6-10. OPTION A FLOW CHART

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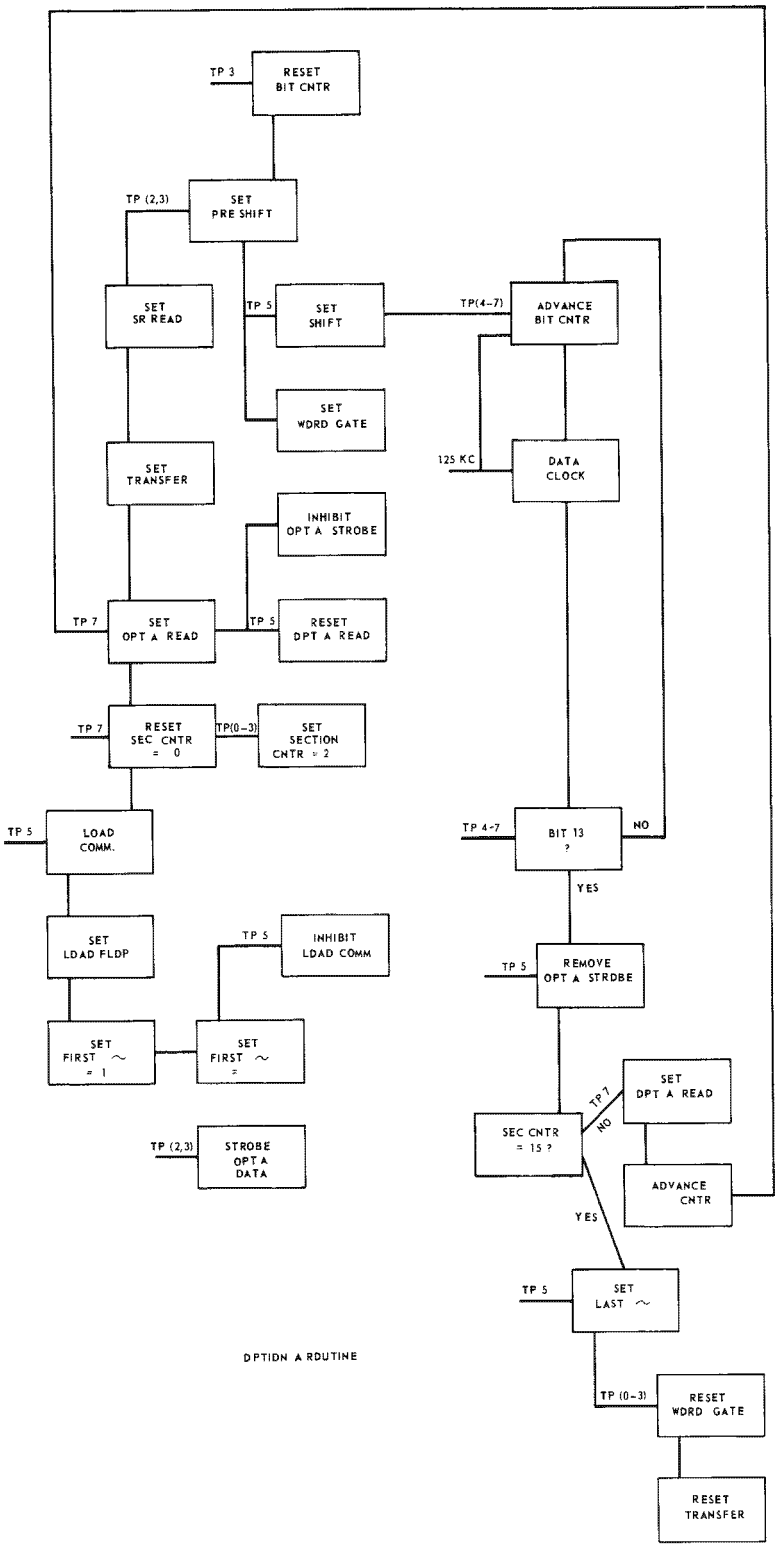
50X1



OPTION A ROUTINE

FIGURE 4.6-11. OPTION A ROUTINE TIMING

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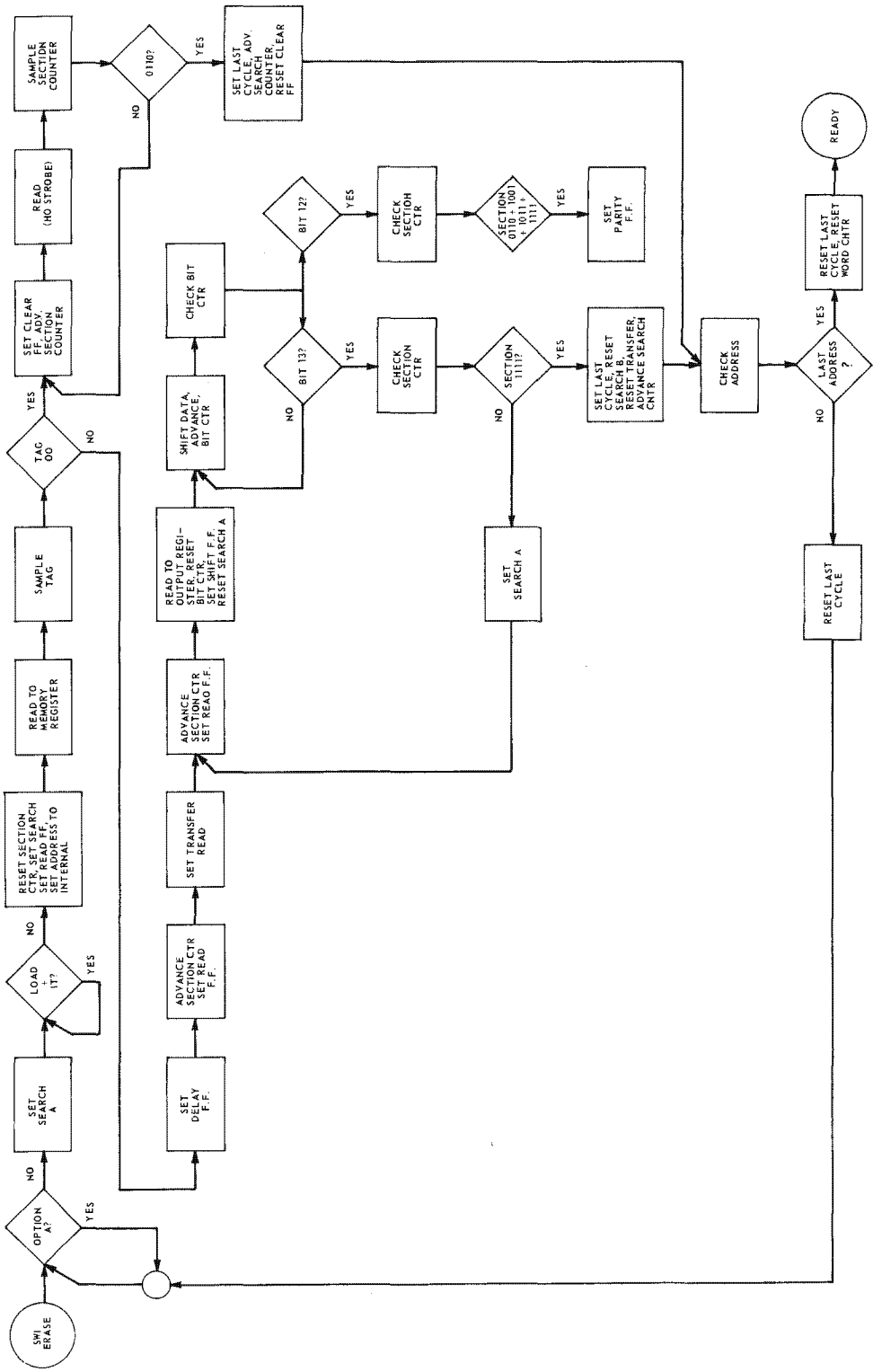

FIGURE 4.6-12. OUTPUT ROUTINE FLOW CHART

50X1

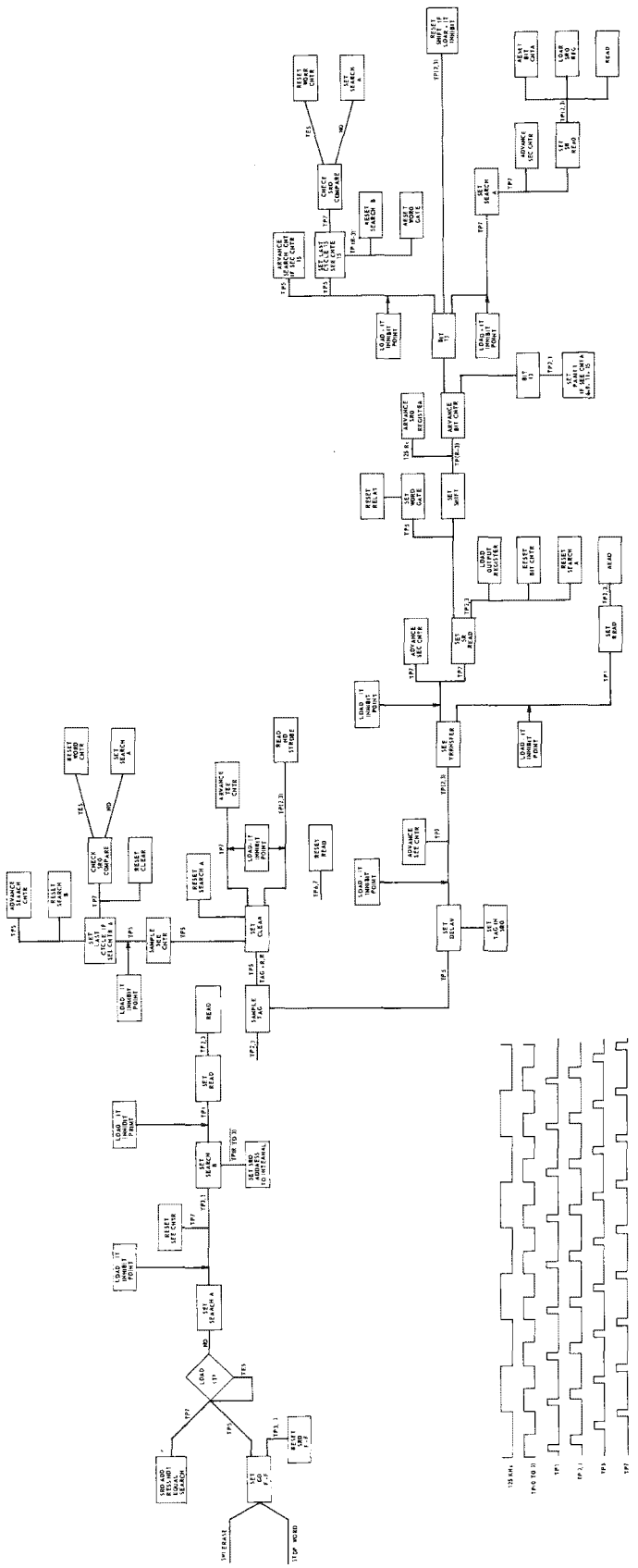

Figure 4.6-13. Output Routine Timing

50X1

The Search routine consists of sequentially reading the tag section of each word in the memory, and examining the tag bits and the CAL ID bit. If the tag bits are both ZERO, it indicates that data concerning only one pulse has been stored, for a given emitter. This is considered to be invalid data, and a Clear routine is initiated. The Clear routine reads each of the first five subwords of the selected address, but the memory strobe is inhibited so that the information is destroyed. If the tag is non-zero, the Output routine is enabled, reading the stored data into the Output Register. If a CAL ID bit is present, the first two bits of the Output Register are preset to ZERO.

At the completion of either a Clear or Output routine, the Search Counter is advanced to the next address and the interrogation process is repeated. This continues until the Search Counter reaches a state equal to the address stored in the SRO Address Register. When this occurs, the Comparison Logic terminates the Search routine, resetting the Word Counter.

The Word Counter, located on assembly A2A, is another six bit ripple counter. This counter is advanced every time a new Buffer Storage memory address is selected by the SWI logic, i.e., on storage of a TAW or first pulse data from an emitter. This generates the Buffer Storage Full indication, in the event that 64 words are stored before a Transfer is completed.

The six bits of address which control the memory switches are derived from the SWI logic during Load and Tag Interrogate, and from the Search Counter during Transfer, as discussed above. Gating is provided on the Search Counter assembly to select the appropriate source of address information. The outputs of these gates control the selection logic on assembly A3, which provides drive for the memory switches.

Assembly A1, the Memory Buffer, includes the memory inhibit driver logic, the memory reset logic, and a twelve bit buffer register used during Tag Interrogation. The inhibit driver logic is normally controlled by the Input Gates, for storage of incoming data. These drivers are also enabled during Memory Reset, to provide half of the necessary reset current to the cores. The remaining half is provided by the Reset Logic, which enables the Reset Drivers within the memory in four groups. These groups contain 4, 3, 3, and 3 drivers, respectively, and are enabled one group at a time in order to reduce peak current levels in the power supply. When the Reset driver group associated with a given set of bits is enabled, the corresponding set of inhibit drivers is enabled.

The twelve bit Memory Buffer receives the tag bits and the seventeen bits of FTOA data read from the memory. The tag bits and five least significant bits of FTOA data are read from the memory. These seven bits are sent to the SWI logic and the PRI encoder via isolating inverters, for tag and

PRI computation. Then the remaining twelve bits of FTOA data are read from the memory. These twelve bits are sent to the PRI encoder to allow the completion of the PRI computation. See Figures 4.6-14 and 4.6-15.

Timing for the output routine is provided by circuitry located on assembly A2B. The 250-kHz output of the System Clock is used to provide the Data Clock repetition rate of 125 kHz.

When an output routine is enabled, the Delay flip-flop, located on A14A, delays transferring data from the core memory to the Output Register while the Section Counter is advanced past the address containing the twelve most significant bits of FTOA data. When the Section Counter has advanced past the address containing the FTOA data, the Transfer logic is enabled and the system begins shifting data from the Output Register.

The data is placed in the Output Register from the core memory, in normal mode, or directly from the Input gates in Option A. After thirteen bits have been shifted, the Bit Counter (on assembly A14A) initiates another Read Cycle, thus placing the next thirteen bits of data in the Output Register. The Bit Counter is a four bit ripple counter with logic to detect state 12 and 13. It is advanced by the shift pulses, and reset each time a Read cycle is initiated.

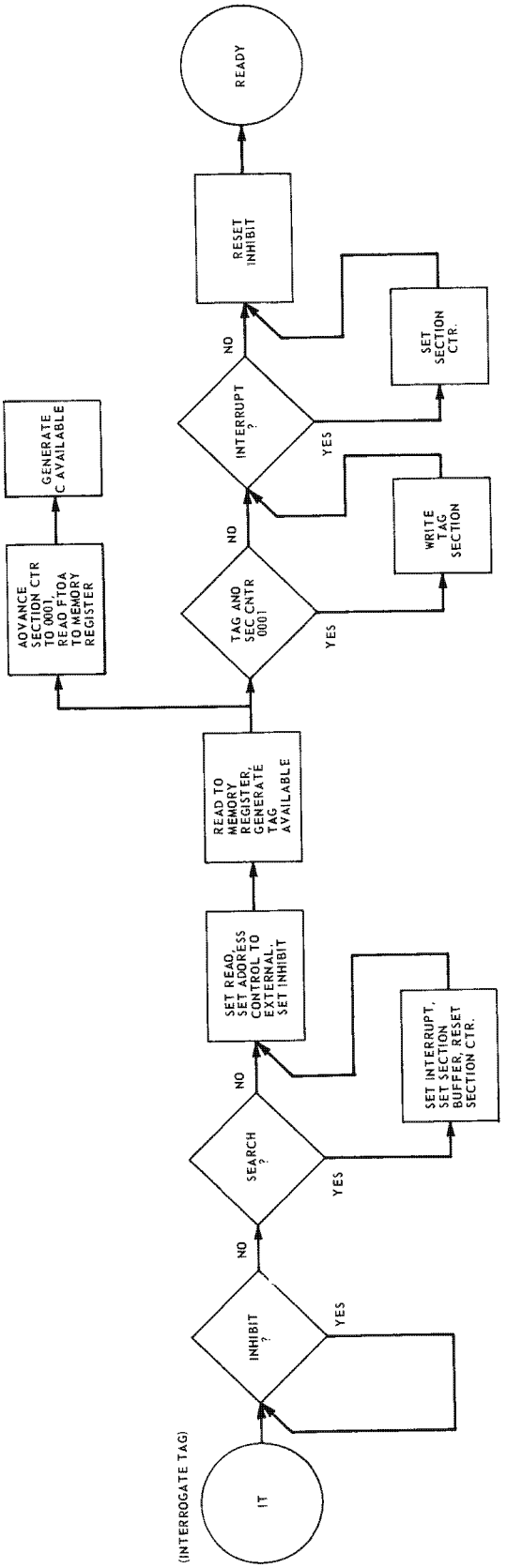

FIGURE 4.6-14. INTERROGATE TAG ROUTINE FLOW CHART

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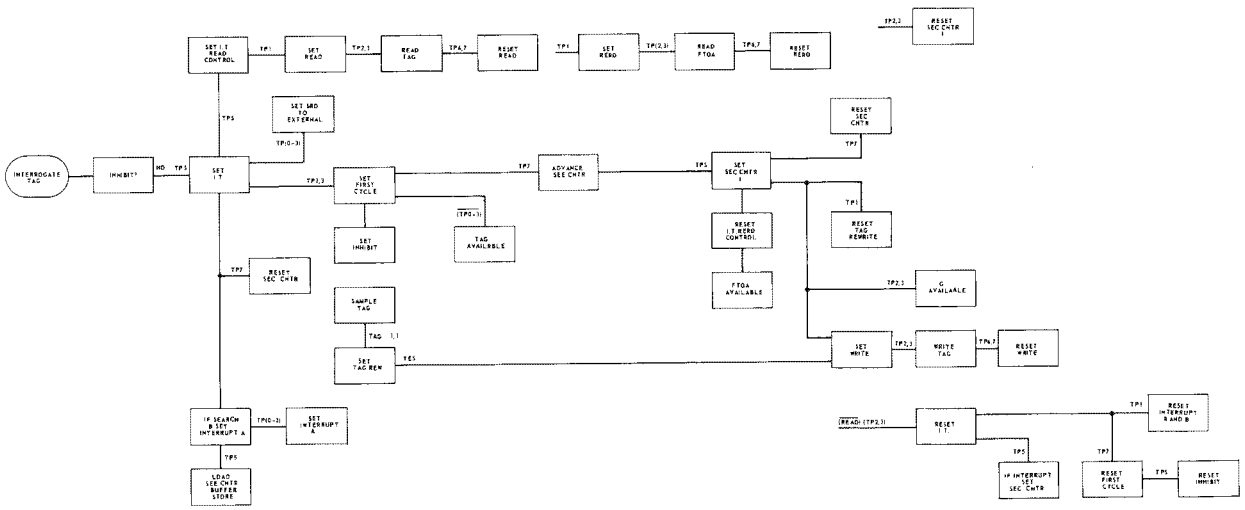


FIGURE 4.6-15. INTERROGATE TAG ROUTINE TIMING

50X1

50X1

[redacted]-R500
298

The Load routine and the TAG Interrogate routine have priority over the output routine and will inhibit generating the following commands in an output routine: Search A; Search B; Read; Transfer; Read to output register; and Last Cycle. The output routine's subword address in the Section Counter is temporarily stored during a Load or TAG Interrogate routine. The Load or TAG Interrogate routines do not prevent shifting data out of the output register, but these routines do prevent changing the output routine's subword address and reading data out of the memory.

The Command Logic assembly is designated A16, and the logic diagrams are [redacted].
The Timing Pulse Generator is located on A16B, and generates the Buffer Storage Logic timing pulses from the 1 MHz, 500 kHz, and 250 kHz outputs of the System Clock.

The Read and Write commands to the Z drivers are generated by flip-flops located on A16B.

The Memory Strobe command is generated on A16B and is inhibited during a clear routine. The Write Command strobes the inhibit logic on assembly A1. The Write X, Write Y, Read X, and Read Y commands strobe the X and Y drivers and switches on assembly A3. The Read command strobes the information from the memory's sense amplifiers into the temporary storage on assembly A1.

50X1

[redacted]

Idealized waveforms, showing the timing relationship of the System Clock, the Buffer Storage Logic timing pulses, the Read commands, the Write commands, and the memory strobe command, are shown in Figure 4.6-16.

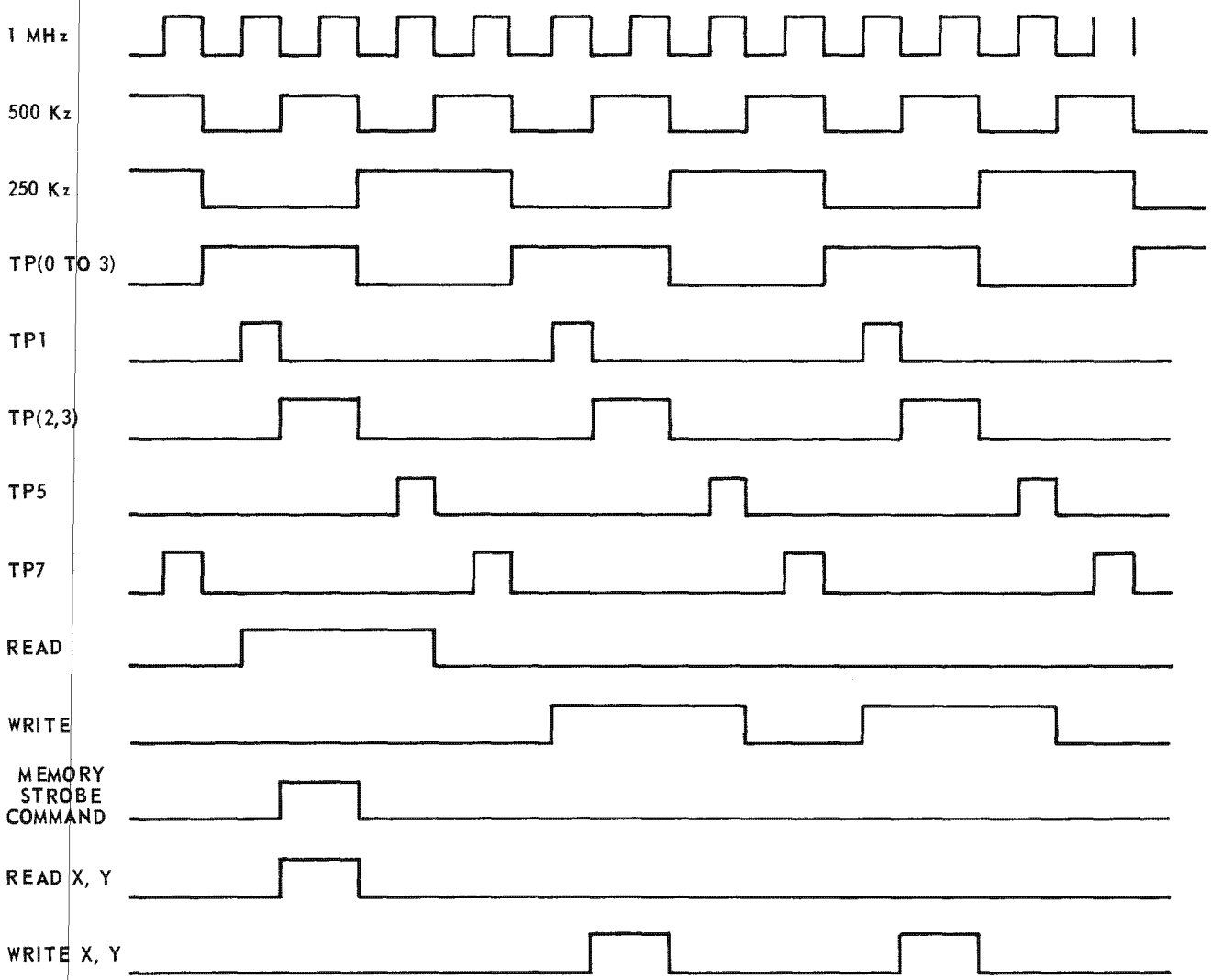
Assembly A16A is composed primarily of the following control flip-flops.

(1) The Interrogate TAG flip-flop places the system in the Interrogate TAG routine.

(2) The Load flip-flop places the system in the Load routine and causes the system to write data in the memory.

(3) The First Cycle flip-flop is set to binary ZERO after the first write cycle of a Load routine or read cycle of an Interrogate TAG routine. This command is used to preset the Section Counter to the correct state and to control the inhibit flip-flop on A16A.

(4) The Inhibit flip-flop, M14, disables the command gates, M14 and M15, after either the Load or Interrogate TAG flip-flops have been set. The Inhibit flip-flop is set when First Cycle is set and is cleared 3 us after First Cycle is cleared by the signal (First Cycle)•TP5 generated on A14A.



READ AND WRITE TIMING RELATIONSHIP

FIGURE 4.6-16 READ-WRITE TIMING DIAGRAM

50X1

(5) The Option A flip-flop causes the system to bypass the memory. During the Option A routine, the data is loaded in the output shift register rather than the memory.

(6) The Search B flip-flop indicates the system is in an output routine. During the output routine, the system may be either clearing the memory or transferring data from the memory to the output shift register. The Search B flip-flop is reset by the Last Cycle command generated on A2.

(7) The Search A flip-flop is set at the start of an Output routine and each time a subword is to be read from the memory during an output routine. This flip-flop is reset when a subword has been read from the memory to the output register on assembly A2, or at the start of a Clear routine. A Load or TAG Interrogate routine will inhibit setting the Search A flip-flop.

(8) The Anti-lock flip-flops, M17 and M18, will reset the Buffer Storage Logic if the system did not transfer data after a SWI Erase command.

In a Load routine the TAG data is written in the memory when the Section Counter is at subword zero. The FTOA data is written in the memory when the Section Counter is at subword 1. The data word is written in the memory when the Section Counter is at subwords 2 through 15. Thus in an output routine, the first two bits of a data word must be loaded into the output shift register when the Section Counter is at subword zero. The circuit composed of M5, M6, and M7 performs this function. A CAL word is indicated by the signal (Section 0)•(Read)•($\overline{\text{Plane 3}}$)•($\overline{\text{TPO to 3}}$) being ZERO. This causes the first two bits of an output word to be ZERO.

The least significant bit, LSB, of the ID word is decoded on A16A. This information is sent to the Interface Logic assembly, A15 . The flip-flop composed of M6 on A15A stores the decoded ID bit as I level, indicating an Intercept word is being written into memory, or T level indicating a TAW word. These levels allow the appropriate Input Gates to be strobed.

The output routine is initiated by logic on A15A. The SWI Erase command or Stop Word Level AND Data Stored generate SRO Clear, which clears the Stop Readout Address flip-flops on A14, and SRO Sample, which sets the Search A flip-flop. The Buffer Storage Empty signal inhibits the SRO Sample from setting the Search A flip-flop unless there has been at least one Load routine since the previous output routine. The Buffer Storage Empty Command is generated on A17B.

The Search A flip-flop is set by Gate M11 after thirteen bits of data have been shifted out of the SRO register on A2A. The search A flip-flop is also set if the SRO address is not equal to the Search Counter address. This signal is generated on A14B and is wire OR'ed with the other set Search A commands on Pin 45 of A15A. The Search A flip-flop is not set during a Load or TAG Interrogate routine.

The Option A Read command, generated on A15B, sets the transfer flip-flop on A2, advances the Section Counter on A13 and sets the shift flip-flop on A2 during the Option A mode of operation. The Option A Strobe, generated on A15B, strobes the data from the Input Gates, A10, A11, A12, and A13A, into the output shift-register on A2.

The signal (Section 0)•(TAG1,1)•(Read) generated on pin 28 of A15B is used on A14A to set the TAG Rewrite flip-flop. The signal (Section 0)•(TAG 0,0)•(Read) is used on A14A to enable either a Clear routine, if the TAG bits are both ZERO, or a transfer routine, if the TAG bits are not both ZERO.

The Section Counter and its associated logic are located on assembly A13A. The state of the Section Counter determines which of the data lines will be sampled, and defines the memory subword which will be selected during the Read-Write cycles.

The Section Counter is preset to 0100 when a TAW word is written into the memory. When an Intercept word is to

be written into the memory, the two most significant bits of the Intercept word ID preset the Section Counter as listed below:

ID	SECTION COUNTER
0 0	0 1 0 0
1 0	1 1 1 0
0 1	0 1 0 1
1 1	1 0 1 1

The presetting of the Section Counter is controlled by gates Z15, Z24, and Z24. The word counter is advanced each time the Section Counter is preset to 0100.

The Section Counter is advanced at the end of each Write Command until the Section Counter has advanced to 1110 OR 0101 OR 1011 AND Intercept word or 0000. Then the counter is preset to 1000 by the action of the set Section Counter to 1 flip-flop, Z4, and the twelve most significant bits of FTOA data are written into the memory. Data Store is generated by the action of the pre-data store flip-flop M25, the counter is cleared to 0000, the two bits of TAG, CAL ID, and the five least significant bits of FTOA are written into the memory, and the Load flip-flop on A16A is reset.

The function Section Counter Reset on Pin 67 of A13A resets the Section Counter after subword 1 has been read in an Interrogate TAG routine and when the set Section Counter to 1 flip-flop on A13A has been set during a Load routine.

This reset function is generated on Pin 15 of A14A.

In an output routine, the Section Counter is advanced by the function TP7•(Clear + Search A•($\overline{\text{Load + IT}}$) (Delay + Transfer)).

Enable SR Read is generated each time the Section Counter is advanced if the Transfer flip-flop has been set. The Enable SR Read is inhibited by (Load + IT)• $\overline{\text{Option A}}$ on A15A. The Enable SR Read signal is used on assembly A2 to set the SR Read flip-flop. The SR Read flip-flop prepares the logic to strobe data from the memory sense amplifiers into the output shift-register.

The flip-flops composed of M1 and M3 allow the Section Counter to be time shared between the Load routine, I.T. routine, and the Output routine. The Load and I.T. routines have priority over an output routine. The flip-flop composed of module M1 is set by Search B•(Load + IT). This transfers the state of the Section Counter into the Section Buffer flip-flops, M16, M17, M18, and M19. The information stored in the Section Buffer is preset into the Section Counter at the end of a Load or TAG Interrogate routine.

Assembly A13B contains the Input Gate logic for plane 13 of the memory, and the Input Gate Control. The Input Gate Control determines which of the data lines will be sampled by decoding the state of the Section Counter into twenty-one sample pulses. The relationship between the memory plane, the

sample pulse, and the data being sampled is shown in Table .

The Input Gates consist of thirteen parallel to serial convertors, and are on assemblies A10, A11, A12, and A13B. The Input Gates on assemblies A10, A11, and A12 convert data for memory planes one through twelve. Memory plane thirteen is converted by the Input Gate on A13B.

Assembly A14A contains the Bit counter, the Clear or Transfer logic, and logic associated with the Interrogate TAG routine.

The input to the Bit counter is the negation of the 125-kHz serial data clock. The Bit counter provides two signals; one signal indicates data bit 12 and the other signal indicates data bit 13. The signal (Bit 12)•TP5 is not used. The data bit 12 signal is used by the parity logic on assembly A2. The data bit 13 signal indicates the last data bit of a subword. This signal resets the shift flip-flop on assembly A2 and if subword 15 has not been read, initiates the next read cycle. If subword 15 has been read, the Last Cycle flip-flop on A2 is set. The Bit counter is reset when data is strobed from the memory into the output register on A2 or when an output routine ends.

The Sample TAG flip-flop, Z15, is set when the memory subword zero is addressed. The Sample Tag flip-flop can not be set during a Load or TAG Interrogate routine or when the Clear, Delay or Transfer flip-flops have been set.

This flip-flop samples the (TAG 0,0) signal generated on assembly A1A. The Clear flip-flop is set if (TAG 0,0) is present at pin 53. This permits the clearing of subwords 0 through 6, thus destroying the unconfirmed data located therein.

The Delay flip-flop, Z16, is set if (TAG 0,0) is not present. This signal delays transferring the data to the output shift register while subword 1 is read from the memory. Subword 1 contains the 12 MSB of FTOA data.

The Delay flip-flop is reset at the start of the Word Gate or every TP7 during the Option A mode of operation.

The signal (OPT A Read)$\cdot$TP (2,3) on pin 73 of A14A is used to preset the data into the output register on assembly A2 by strobing the input gates on assemblies A10, A11, A12, and A13B.

First cycle (TP5) on pin 67 of A14A is used to reset the inhibit flip-flop on assembly A16A.

The Search A Reset is generated on Assembly A14A by wire ORing (last Cycle)$\cdot$TP5 with SR Read$\cdot$(TP 2,3) + $\overline{\text{Clear}}$.

The Signal on pin 61 of A14A is not used.

Several Interrogate TAG routine commands are generated on A14A. The IT Read signal controls the Read flip-flop on A16B. IT Read is present from the start of the Interrogate TAG routine until after subword 1 has been read from the memory.

The TAG Rewrite Command is generated when both bits of TAG, which was read from subword 0, are ONE. After subword 1 has been read, the Section Counter is reset to subword 0. If the TAG bits are both ONE, TAG Rewrite sets the write flip-flop on A16B and subword 0 is written back into the memory.

The C available command is generated 4 us after subword 1 has been read from memory.

The remaining commands generated during an Interrogate TAG routine are located on A15A. The TAG Available command is generated after subword 0 has been read from memory and FTOA Available occurs after subword 1 has been read.

Module M4 on A15A inhibits setting the SR Read flip-flop on assembly A2 during a Load routine or an Interrogate TAG routine. The Option A mode disables the inhibit since the Load flip-flop on A16 is set during the Option A mode of operation.

Pin 27 on A15A is wire OR'ed with a Last Cycle command to generate (Bit 13)•(Option A)•(Last Cycle). This signal is used to reset the Data Store flip-flop on assembly A13 during the Option A mode.

The Stop Word Sample on Pin 49 of A15A causes Search A flip-flop on A16 to be set if the Stop Word Level is present on Pin 45 of A16A. This signal is inhibited during the Option A mode.

The Word Counter Reset on Pin 51 of A15A is wire OR'ed with pin 56 of A14B. The signal on pin 56 of A14B indicates the Search address equals the Stop Readout address. During the Option A mode, the Word Counter has no meaning so the counter is reset by Data Stored.

Assembly A2A contains the Word Counter, the Temporary X, Y storage, and logic associated with the output routine. The Word Counter, M4, M5, M6, M10, M11, and M12, is advanced each time the Section Counter is preset to 0100. It is reset when the Search Address equals the Stop Read-out Address during an output routine or by Data Stored during the Option A mode of operation.

Memory Full is generated when the Word Counter has counted 64 words before being reset.

The Temporary X, Y Storage flip-flops, M1, M8, M15, M16, M17, M18, M19, and M20, allows the X_c, X_f, Y_c, and Y_f data to time share much of the same logic.

The Transfer flip-flop, M13 and M21, indicates data will be transferred to the output shift register rather than be cleared. The Transfer flip-flop is set by [Delay]·[TP2S]·[$\overline{\text{LOAD}}$]·[$\overline{\text{I.T.}}$] · [Section Counter 1] or by the Load flip-flip during the Option A mode of operation. The Transfer flip-flop is reset when Last Cycle is generated.

The SR Read flip-flop, M13, indicates data is to be transferred within the next 2.5 us. The Enable SR Read signal is generated on A13A when the Section counter is advanced after the Transfer flip-flop has been set. Enable SR Read is inhibited by either a Load routine or an Interrogate TAG routine on card A15A. This allows either of these routines to have priority over the output routine.

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The SR Read command is AND'ed with TP2,3 on A2B. The signal SR Read • TP2,3 resets the Bit counter on A14, strobes the data from the memory into the Output Shift Register, M1 thru M10, M18, M19, and M20, sets the Preshift flip-flop, and resets the Search A flip-flop on A16. The Preshift flip-flop, M23, will set the Shift flip-flop, M22, M23, when the phase of the 125 kHz Data Clock is correct. The Shift flip-flop sets the Word Gate flip-flop, M21, removes the Inhibit on the Data clock which advances the data through the register and advances the Bit Counter.

The Shift flip-flop is reset after thirteen bits of data have been shifted out. Logic on A15 causes the Search A flip-flop to be set again. This advances the Section counter, generates Enable SR Read, and the next thirteen-bit subword is preset into the Output Register.

The Parity Generator consists of the Parity flip-flop M15 and the J-K flip-flop M27. Pin 6 of M27 will be a ZERO of an even number of data bits are ONE. The Parity flip-flop is set at the end of the twelfth bit of the sixth, ninth, twelfth, and fifteenth subwords of an output routine, and if the J-K flip-flop indicates an odd number of data bits in the subword were ONE. The Parity flip-flop presets the Output flip-flop M28 and forces a parity of ONE.

The Last cycle flip-flop, M7 and M14, on A2A is set on the last bit of the last subword of a transfer routine

or on subword 6 of a clear routine. The Last cycle command advances the Search counter, resets the Search B flip-flop, strobes the SRO comparator, and resets the Transfer flip-flop and the Word Gate flip-flop.

The timing relationships of the output routine are shown in Figure 4.6-17.

The Search Counter, assembly A14B, consists of four main subsystems: The Search Counter, the Storage for the SRO address, the SRO Comparator, and OR gates to apply either the Write address or the Search address to the X and Y switches.

The Stop Read-out address is applied to the Search counter assembly after the SRO Clear signal, from A15B has reset the SRO Address Storage flip-flops, M26, M27, and M28. These flip-flops provide one input to the SRO Comparator, M16, and M18. The other input is provided by the Search counter, M4, M5, M6, M7, M8, and M9. The Search counter provides the address information to the X and Y switches during an output routine. Initially the Search counter is reset to address 0 by the Memory Reset and continues to advance until the address in the Search counter equals the SRO address. At the next output routine, the Search counter starts at the old SRO address and advances until it equals the new SRO address. The Search counter is advanced by the Set Last Cycle command from assembly A2. The SRO Comparator is strobed after the

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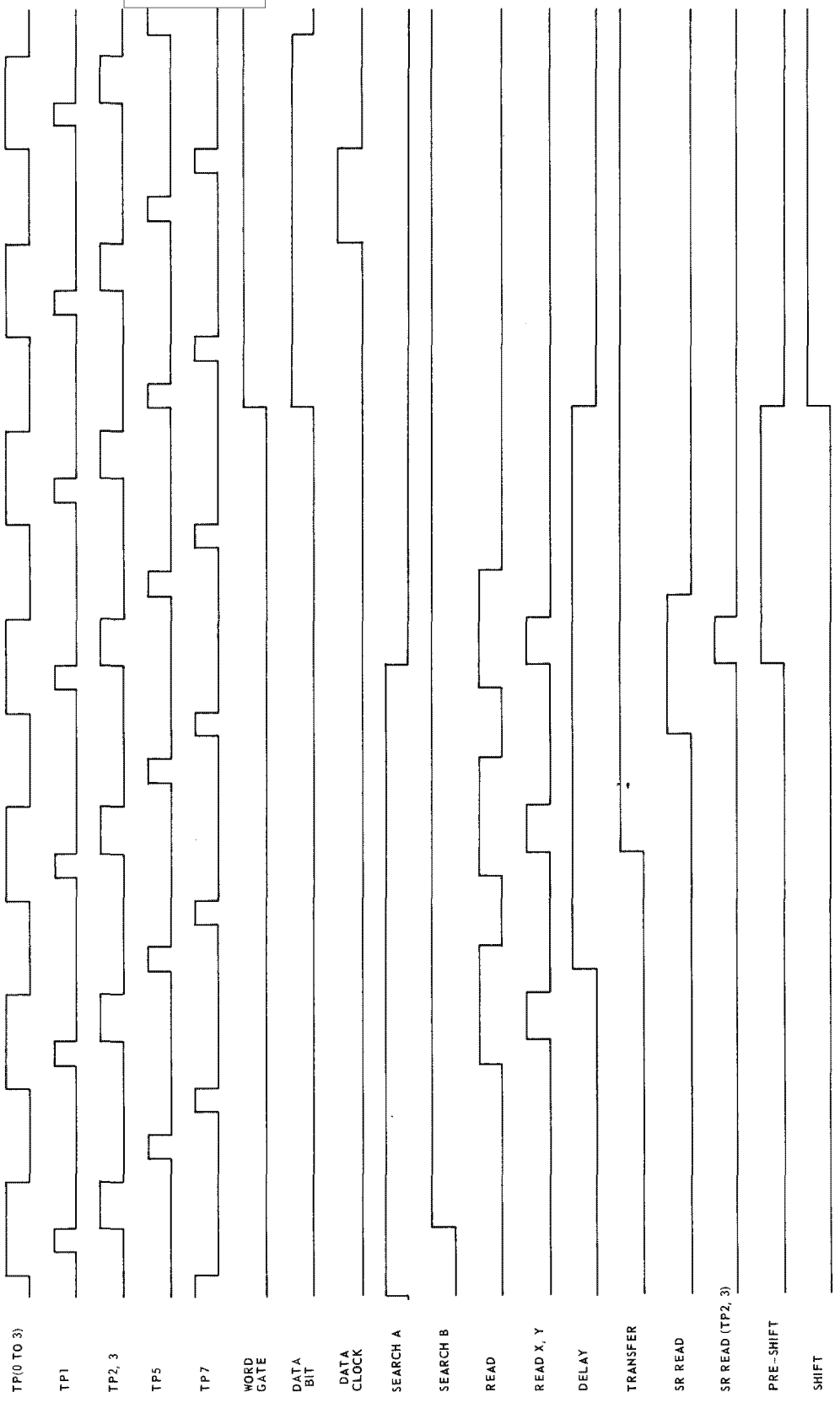

FIGURE 4.6-17. TIMING OF START OF OUTPUT ROUTINE

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counter has been advanced. If the Search counter does not equal the SRO address, the Search A flip-flop on A16 is set and a new output routine is begun. The output routine is stopped, by not setting the Search A flip-flop, and the Word counter is reset, when the Search address equals the SRO address.

Modules Z1, Z2, and Z3 form OR gates which apply either the Write address, for a load routine, or the Search address, for an output routine, to the X and Y switches. The flip-flop composed of Z21 controls this OR gate.

The address information is sent from the Search counter assembly to the X and Y Selection assembly A3. The three MSB of the address are decoded to provide the information for the eight X switches. The three LSB provide the information for the Y switches. The binary number from the Section counter, A13, is decoded to provide the information for the X and Y drivers. The two MSB provide the information for the X drivers and the two LSB provide the information for the Y drivers.

Assembly A1 consists of logic for controlling the memory Inhibit drivers, a buffer register for Tag Interrogation, and logic for implementing the initial clearing of the memory. Modules Z1, Z2, Z3, Z4 and Z5 of the B side form a ten-bit register for temporary storage of Fine Time of Arrival data from the memory. Z15 on the A side

provides two bits of storage register for the Tag bits. These registers are cleared initially by Memory Reset (pin 34), and also during each Read cycle by [TP2,3] [2 MHz] (pin 36) AND Read Level (pin 38).

When the tag section of the data word is read during an Interrogate Tag routine, the tag bits and the FTOA data are read into the register via inverters Z1, Z7, Z13B, Z13C, Z14B and Z14C of the A side of A23. The outputs of the register are routed, via isolating inverters Z6B, C and D, Z12, Z13, and Z14D of A23B, to the SWI logic and the PRI encoder. In addition, the tag bits are sampled by Z6A (B side) and Z14A (A side), producing ground true outputs at pins 73 or 74 if the tag bits are both ZERO or both ONE, respectively.

Modules Z7 through Z11 of A25B, and Z11A and Z12 of A25A, control the Inhibit drivers in the B.S. memory ANDing data inputs from the Input Gate cards with the "Write Level" (pin 66). The Inhibit drivers are thus activated during the Write cycle, if the data line for that particular bit is at ZERO.

Memory Reset, at pin 34, is a positive-true pulse, nominally four microseconds wide, which occurs twice per second during the periods when the Payload On command is not enabled. This pulse enables one of the outputs of Z4 or Z5, depending on the states of the two counter stages, Z2 and Z3. The enabled output activates one of the four groups of Memory

Reset drivers, and simultaneously activates the corresponding group of Inhibit drivers. This action resets all cores in the selected planes to zero. The end of the pulse advances the two stage counter, and the next Memory Reset pulse enables a different set of Reset and Inhibit drivers. The entire memory is thus cleared in four sections, one section for each reset pulse. This reduces the peak current drawn by the memory during the reset.

The signal start Delay Timer + S_{10} is generated on this assembly by Z8 for the SWI logic.

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4.6.9 Core Memories

Information storage for the Space Window correlation logic and for the Buffer Storage Logic is provided by two independent ferrite core memory systems. The internal operation of these memories is essentially identical for both units, the only major differences being in the array size and configuration.

4.6.9.1 Theory of Operation

The Ferrite core element which provides the storage capability is physically a small toroid, with a nominal outside diameter of 0.030 inches, nominal inside diameter of 0.020 inches, and a nominal thickness of 0.010 inches. The cores are constructed of a ferromagnetic material with very high retentivity and high hysteresis. The hystersis loop, or plot of flux density versus magnetomotive force, is shown in idealized form in Figure 4.6-18.

From the figure, it is readily apparent that, with no externally supplied magnetic field (H=0), the flux density in the core will be either that defined by point A or that at point D. The core is thus capable of storing binary information by some means of controlling and sensing the direction of magnetization of the core. Point A may be arbitrarily defined as the ONE state, and point D the ZERO state.

By threading a current-carrying conductor through the center of the core, it is possible to produce a controlled

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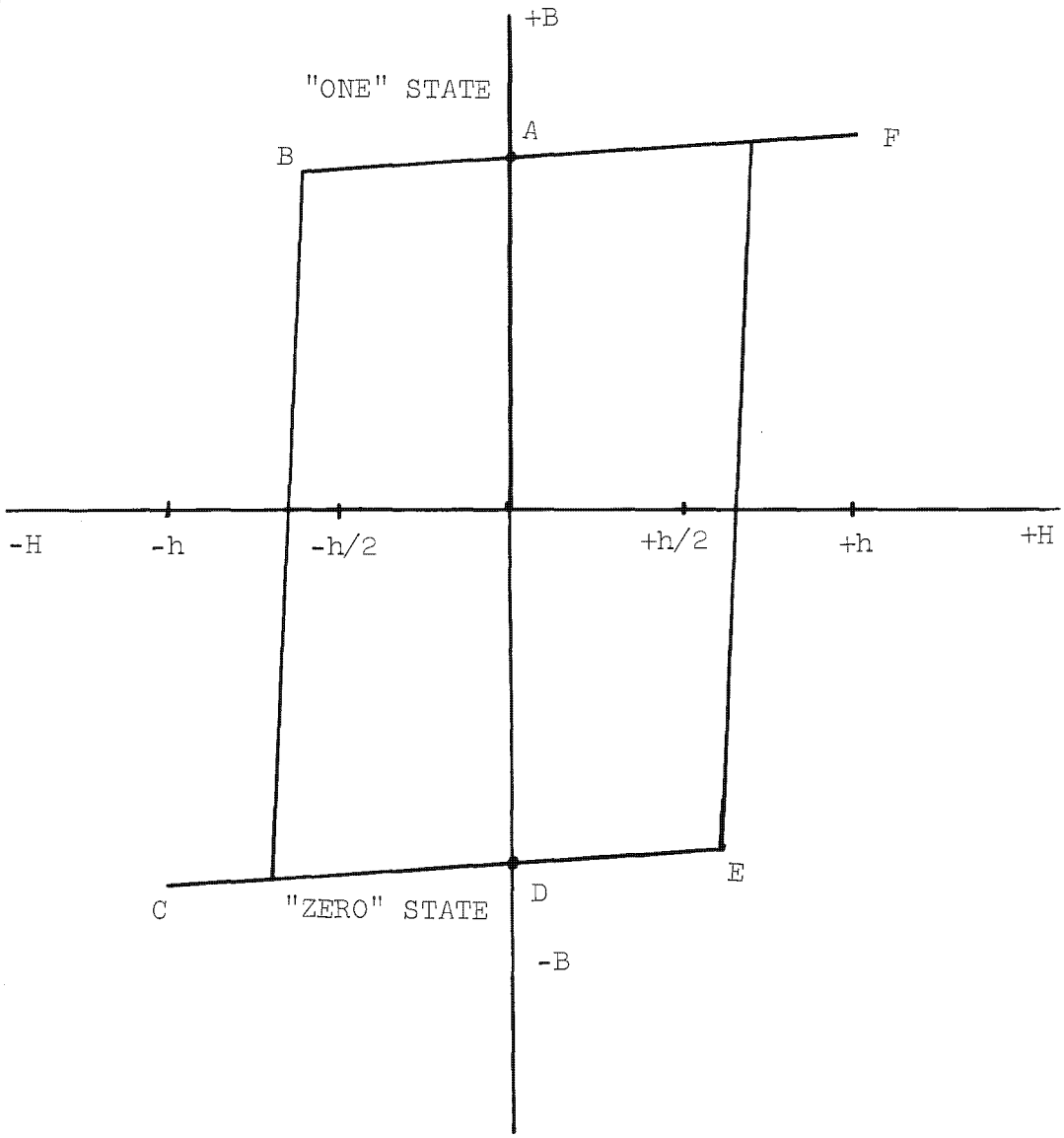

FIGURE 4.6-18 HYSTERSIS LOOP

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amount of magnetomotive force in the core, and thus modify the flux density. For example, assume that the operating point of the core is A, and current is passed through the wire such that the magnetomotive force is caused to increase in the negative direction. The operating point of the core will move along the curve toward point B, with very little change in the flux density. At point B, the core characteristics change, and further increase in the current will result in a relatively rapid change in flux density and a reversal in the direction of magnetization. Once the core has "switched," further increase in current, such as to point C, will cause little variation in the flux density. When the current is removed, the operating point moves to D, and the core is said to be in the ZERO state.

Current in the opposite directions will cause the core operating point to move from D to E, then out to F, returning to A after the current is removed. Thus, applying sufficient external magnetomotive force to change the core operating point to either C or F will cause the core to switch from one state to the other. If this level of magnetomotive force is defined as h, it will be noted that a core switching threshold may be defined. In the idealized case of Figure 4.6-18, the threshold is seen to be approximately 0.7 h. If an external magnetomotive force equal to, for example, 0.5 h is applied, it will be noted that no significant change in the core operating point will result after the excitation is removed.

Thus a current producing 1.0 h will cause the core to switch, while a current which produces 0.5 h will not change the state of the core. This characteristic is utilized in the memory to permit selective storage and recovery of binary information.

In the memory, numerous ferrite cores are arranged in planar array, with each core threaded by one conductor in each direction (X and Y axes). A small section of such an array is shown in Figure 4.6-19. If currents are passed through the wires, magnetomotive forces will be produced in each of the cores threaded by the wire. In particular, if a current sufficient to produce 0.5 h (typically, 300 to 400 milliamperes, depending on core type) is passed through wire X1, from top to bottom and if a similar current is passed through wire Y2, from left to right, the magnetomotive forces will add in core C, and it will receive a net excitation of 1.0 h. The other cores each receive only 0.5 h, and their states are thus not disturbed. This technique is known as coincident-current selection.

If it is assumed that core C had been in the ZERO state, and the directions of the currents are such that an opposing flux is produced, the core will be switched to the ONE state. This action is defined as writing the core. By producing currents in the opposite direction, it is possible to read the core by sensing the change in flux density as the core switches. This is accomplished by threading a third wire,

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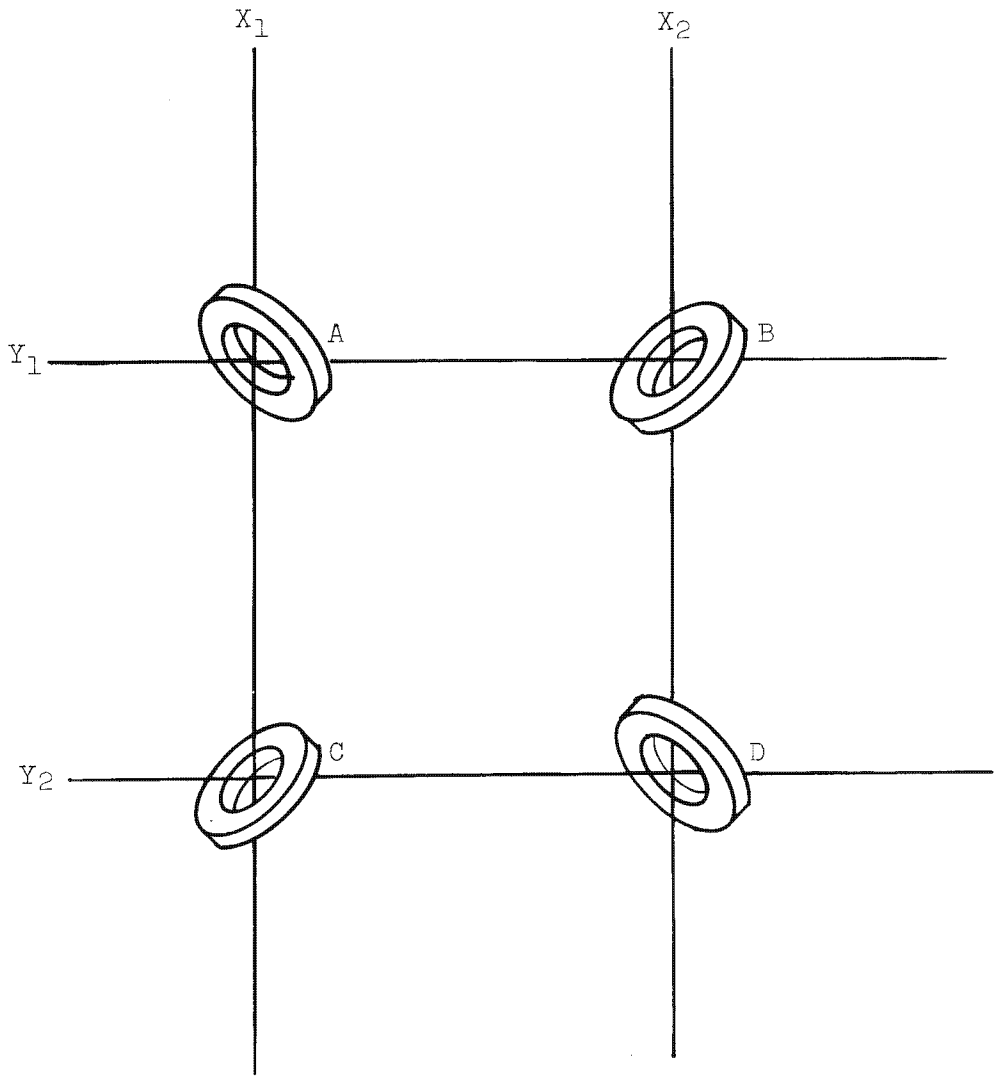

FIGURE 4.6-19 CORE ANNOY

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the sense wire, through all the cores in the plane. A current will be induced in this wire by the change in magnetic flux when a core switches. The sense wire is arranged so that the flux changes caused by the half-selected cores in the array tend to cancel, and the net current in the wire is primarily produced by the relatively large change in flux density in the selected core.

If the selected core is in the ZERO state, little flux change results, and a relatively small current is induced in the sense wire. An amplifier and threshold device is employed to discriminate between sensed ONE and a sensed ZERO. The read operation is inherently destructive, in that the selected core will unconditionally be in the ZERO state after reading. If it is necessary to retain the information, the core must be returned to its former state by a write operation.

A practical memory consists of several of the planar arrays described above, one plane for each bit in the data word. The X and Y axis wires are connected in series from plane to plane, such that current in a given set of drive lines will select one core in each plane. Each plane has an individual sense wire, with its associated sense amplifier and storage element. In order to write meaningful data in the memory, a fourth wire, designated the inhibit or Z-axis wire, is threaded through the cores. Each plane has a separate inhibit wire, which passes through the cores so as to be parallel with either the

X or Y axis wires.

By passing a current which produces 0.5 h through the inhibit wires, in a direction which will cancel the field produced by the X or Y wire, the writing of a core may be inhibited, as the net flux in the selected core will be 0.5 h + 0.5 h - 0.5 h = 0.5 h. The other cores on the selected X and Y wires receive a net flux of zero, and all other cores in the array receive -0.5 h. By this means, it is possible to individually write a ONE in any combination of the selected cores, while those planes receiving the inhibit current are not written, and remain in their original state.

Generation of the selection currents is accomplished by high current, saturating switches with series resistors which determine the current produced. In order to minimize the number of components required, selection of the X and Y axis is accomplished by a driver/sink technique. An example of this technique is shown in Figure 4.6-20, in which any one of six teen wires is selected by actuation of a unique combination of drivers and switches. For example, if Driver D2 and switch S2 are actuated, current will flow in the wire designated "6". The driver and switch circuits are bilateral, such that current may be produced in either direction in the wire. The magnitude of the current is determined by the voltage levels +V and -V, and by the current-determining series resistors.

The bilateral isolation diode matrix is used to

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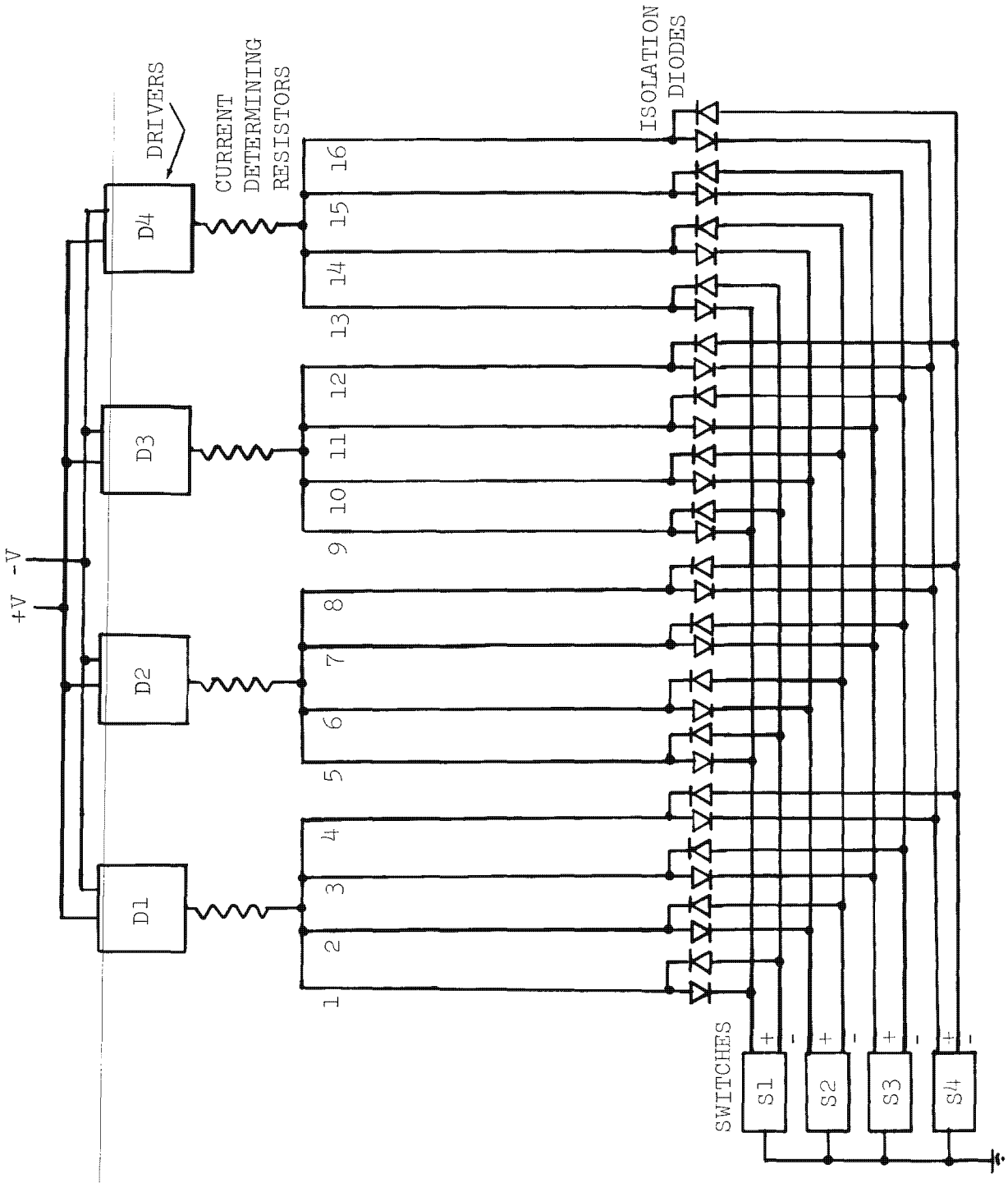

FIGURE 4.6-20 DRIVER/SINK TECHNIQUE

prevent parallel paths for current flow. Without the diodes, and with the same driver/switch combination as above, the following parallel paths would exist: (1) From D2, through wire 5, then back through wires 1, 9 and 13 to the other drivers, then to S2 via wires 2, 10 and 14. (2) A similar path through wire 7, then to S2 via wires 2, 10, and 14. (3) From D2 through wire 8, then through wires 4, 12 and 16, then to S2 via 2, 10, and 14. A similar set of parallel paths exists for each wire in the array, and since the ferrite core is a current operated device, it is necessary to closely control the current flow to the selected wire.

4.6.9.2 Memory Circuits

The circuits which generate the drive currents for the core memories are shown on the following drawings:

4124-62010 SWI Z Driver

4124-60010 B.S. Driver

4124-60016 X & Y Driver

4124-60018 X & Y Switch

4124-61012 Recognizer Z Driver

The SWI Z driver consists of a dual, unilateral saturating switch with series resistances in the output circuit. The output is connected directly to one end of the inhibit wire of a plane, the other end of the wire being returned to ground. A negative pulse (produced by the Data Handler SWI logic) at pin 6 causes Q1 to saturate, which in

turn saturates Q2. The collector of Q2 thus becomes essentially -10.5 volts, producing a current in the inhibit wire which is determined by the parallel combination of R9 through R12, in series with the resistance of the inhibit wire. The resistors R9 through R12 are selected in test to produce an inhibit current of approximately 365 milliamperes (ma.), a current which will produce the desired magnetomotives force of 0.5 h (see above).

The other part of the driver, consisting of Q3 and Q4, produces a reset current in response to a negative pulse at pin 2. Resistors R13 through R16 are chosen to produce a reset current of approximately 750 ma., which generates 1.0 h. This causes all cores in the plane to be reset, i.e., set to the ZERO state, and is performed at the beginning of each frequency dwell.

The Buffer Storage Z driver employs a similar dual, unilateral switching circuit, but re-arranged to operate from the +10.5 volt supply, thus tending to balance the load on the power supply. A negative pulse or pin 2 saturates Q1, saturating Q2, and thus causing the emitter of Q2 to become essentially +10.5 volts. Resistors R10 through R13 are chosen to produce a halfselect current of approximately 400 ma. (a different type of core is used in the Buffer Storage memory) in the inhibit wire.

The other half of this driver is identical to the Inhibit driver, and produces a half-select current of 400 ma

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during Initial Reset of the B.S. memory, in response to a negative pulse at pin 7. The Buffer Storage logic produces simultaneous pulses at both inputs to this circuit during reset, so that the net current in the inhibit wires is approximately 750 ma., sufficient to switch all cores to the ZERO state.

The Recognizer Z Driver is identical in circuit configuration to the Buffer Storage Z Driver. However, resistance values are modified to permit operation from +6V instead of +10.5V. This change was made to conserve power in the Recognizer Memory.

The X and Y driver circuit is a bipolar, saturating switching circuit, consisting essentially of one half of each of the Z driver circuits discussed above. The Read Driver, consisting of Q1 and Q2, is identical to one side of the B.S. Z driver, and generates current in the positive direction in response to a negative pulse at pin 1. The Write Driver, formed by Q3 and Q4, is similar to one side of the SWI Z driver, and generates current in the negative direction in response to a negative pulse at pin 7. The selected current determining resistors permit individual adjustment of Read and Write currents for each application. Each driver is connected to a group of selection lines, as was discussed above.

The X and Y Switch provides a bilateral sink for the currents produced by the X and Y drivers. This module also incorporates the selection matrix diodes for four wires. The circuits are essentially identical to the circuits in the driver, with the exception of the voltage levels involved. The Read Switch circuit is identical to the Write Driver, except that the emitter of the output transistor is returned to ground rather than -10.5 volts. A negative pulse at pin 2 saturates Q1 and Q2, providing a current sink for the output of a Read Driver.

The Write Switch is similar to the Read Driver, except that the collector of the output transistor is returned to ground, rather than +10.5 volts. A negative pulse at pin 1

saturates Q4 causing Q3 to conduct, and providing a sink for current produced by a Write Driver.

Sensing of the state of a core, during Read, is accomplished by an integrated circuit sense amplifier, the Texas Instruments SN5500. This amplifier is especially designed for memory applications, and incorporates a high gain differential amplifier, strobe logic, a threshold detector, and a one-shot multivibrator. One of these devices is used for each plane in the memory, and produces an output compatible with the integrated circuit logic in the data handler.

The voltage produced by the induced current in the sense wires is shown in the memory timing diagram, Figure 4.6-21. The induced noise, caused by the memory selection currents, will normally be well above the level of the sense voltage, necessitating a strobe pulse to avoid extraneous ONE's in the readout. The strobe enables the sense amplifier only at the time when a legitimate sense voltage may be present. Typical voltages on the sense line are 40 to 50 millivolts peak for a sensed ONE, and 6 to 8 millivolts peak for a sensed ZERO. The threshold detector makes a decision at strobe time, and if the sense voltage is in excess of the threshold level (e.g., 30 millivolts), the one-shot multivibrator is triggered, producing a ground-true output from the sense amplifier.

The relative timing of the selection currents is indicated in the figure. The inhibit current is present only

50X1

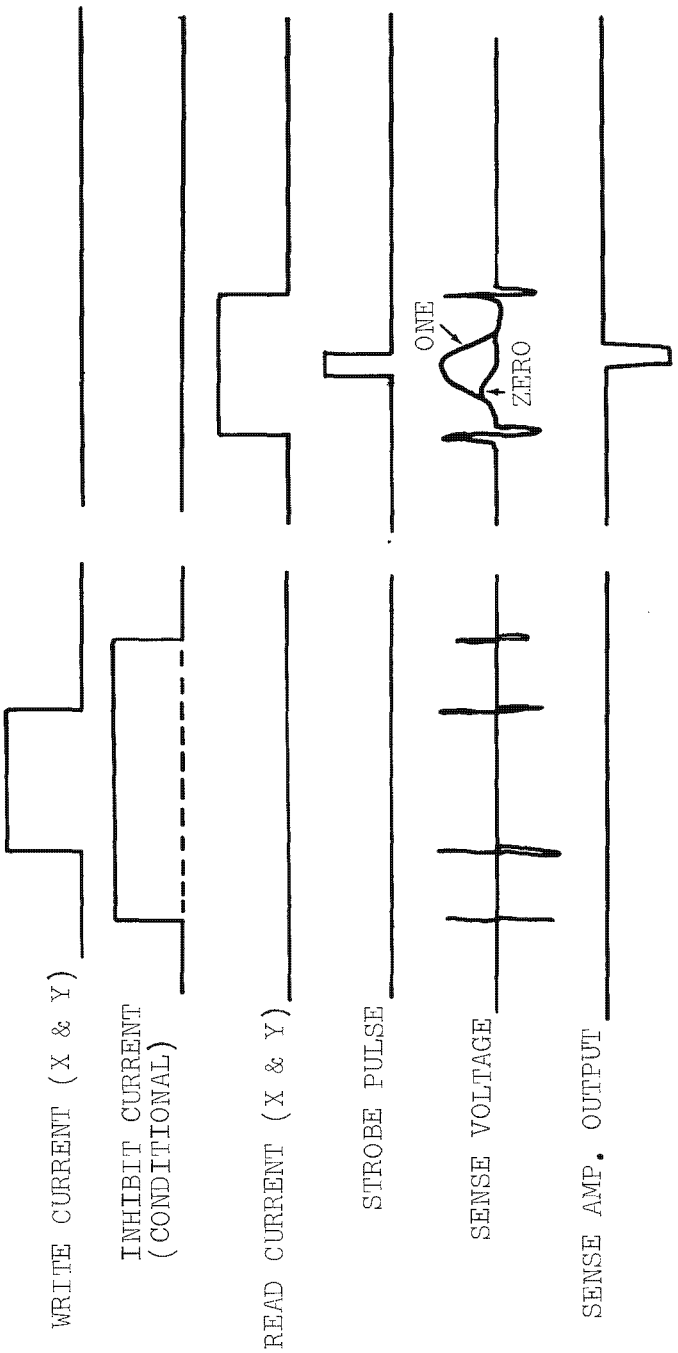

FIGURE 4.6-21 SELECTION CURRENT TIMING

50X1

when writing a zero, and is of longer duration than the X and Y axis current pulses to avoid improper core switching during the transient periods. Typical current pulse widths are one to two microseconds for X and Y axes, and three microseconds for the inhibit pulse.

The Read pulse generated in the memory logic is applied to the Strobe Driver (4124-60012), which in turn generates a narrow (approximately 200 ns) positive strobe pulse which is applied to the strobe input terminal of all sense amplifiers in the memory. This pulse is delayed approximately 350 ns behind the leading edge of the Read pulse. Both the width and delay of the output pulse are adjustable to provide optimum timing for each memory. The sense amplifiers are mounted on circuit boards adjacent to the core stack. Also, the Buffer Storage sense amplifier boards incorporate inverters to produce positive true pulse from the memory.

4.6.9.3 Memory Organization, SWI

The Space Window memory is shown in simplified block diagram form in Figure 4.6-22. This memory consists of seven planar arrays of cores, each array being 16 (Y) by 40(X) cores. These cores are selected by four drivers and four switches in the X axis. Seven each of the SWI Z drivers and sense amplifiers (one for each plane) provide the remaining interface between the memory and the SWI logic. The Z axis drivers have an individual Inhibit input from the logic, while

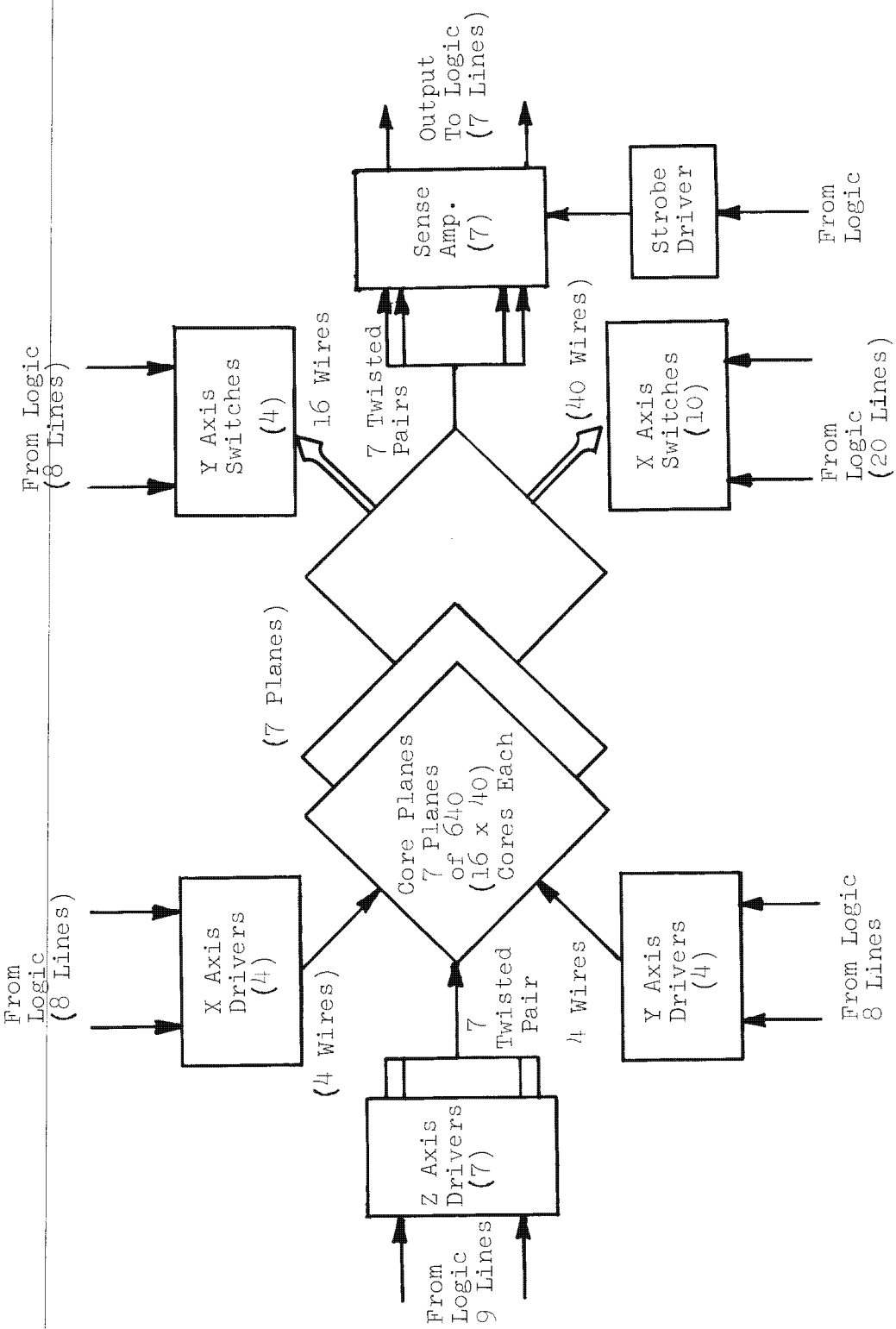

FIGURE 4.5-22 SWI BLOCK DIAGRAM

the reset inputs are connected in two groups, one of four and one of three drivers. Each of the X and Y drivers and switches has two inputs from the logic, one for Read and one for Write.

Addressing of the SWI memory is controlled by the outputs of the Coder-Combiner via the SWI Selection Logic. The array represents the System Field of View, with each core in the array subtending an area equal to two quantizing elements on a side. A particular combination of phase codes, i.e., arrival of a pulse from a given direction, will enable a unique combination of drivers and switches, thus addressing a particular set of coordinates in the array and a particular group of seven cores. Arrival of another pulse from the same direction will interrogate the same cores, resulting in the capability of space-oriented correlation of pulses from multiple emitters. The operation of the SWI memory and logic is discussed in detail in paragraph

4.6.9.4 Memory Organization, Buffer Storage

The Buffer Storage memory is shown in simplified block diagram form as Figure 4.6-23 . The core stack consists of thirteen planes, each containing 1024 cores arranged in a 32 x 32 array. The X and Y axis wires are divided into four groups of eight wires each in each axis, and are selected by four drivers and eight switches in each axis. Thirteen sense amplifiers, one for each plane, provide the readout data to the Buffer Storage logic. The thirteen Z axis drivers are connected

50X1

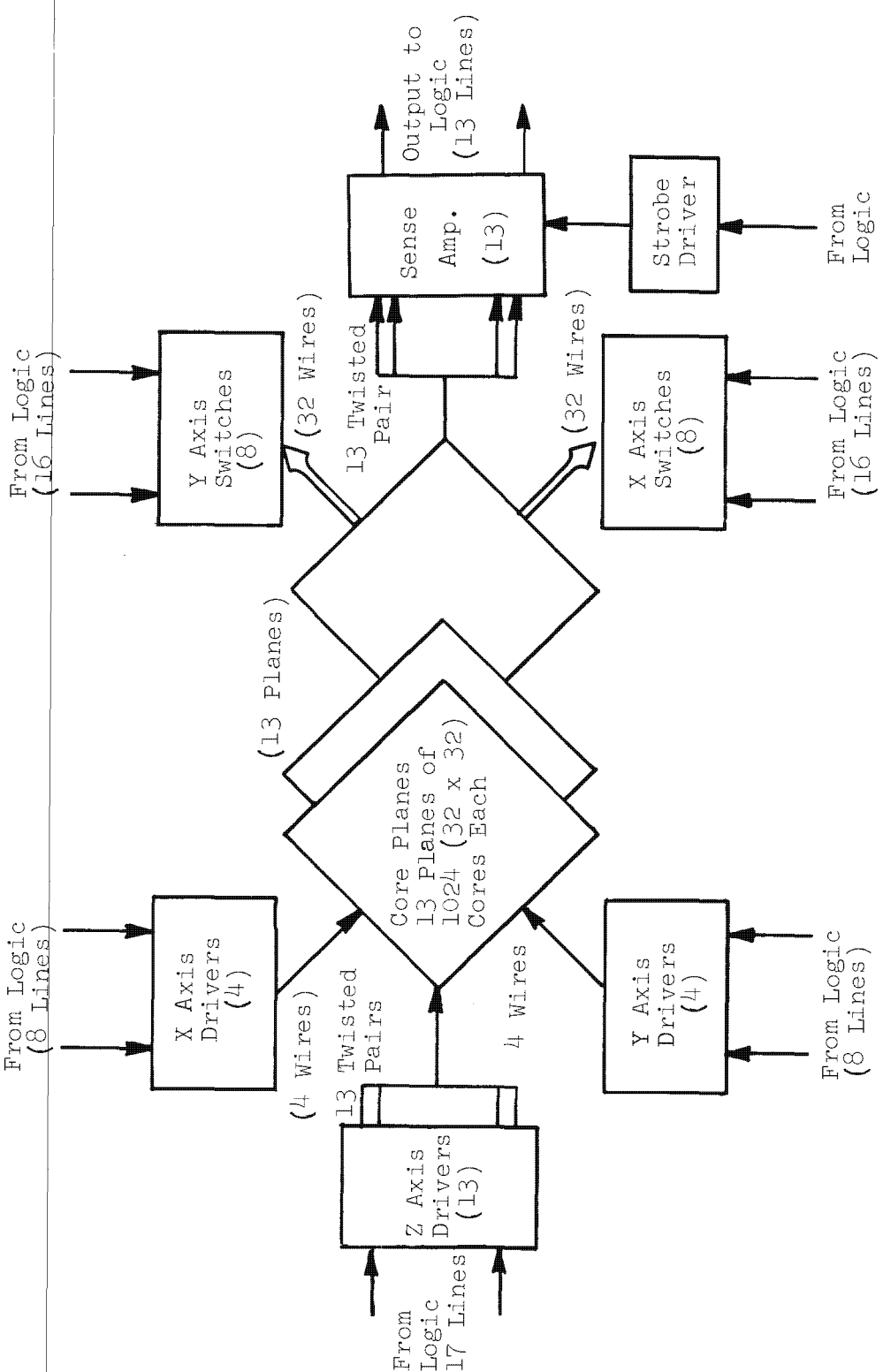

FIGURE 4.6-23 BUFFER STORAGE MEMORY

50X1

with the Inhibit functions individually available to the logic, and the reset inputs combined in three groups of three drivers each, and one group of four drivers. This grouping is done to avoid overloading the logic outputs and to reduce peak current demands from the power supply. During reset, only one of these groups is enabled. The next reset pulse enables another group, etc., so that after four reset pulses, the entire memory is cleared. Each of the X and Y axis drivers and switches has two inputs from the B.S. logic, one each for Read and Write.

The Buffer Storage memory is addressed by the state of the Section Counter (See paragraph 4.6.8) and by either the Search Counter or the SWI logic. The X and Y drivers are controlled, via the Selection Logic, by the Section Counter. The six bits from either the Search Counter or the SWI Logic, via the Selection Logic, control the X and Y axis switches.

Data is written into, and read from, the cores in subwords of thirteen bits each, i.e., one bit in each pulse at the selected address. Sixteen sets of thirteen bits, or 208 cores, are reserved for storage of each word. Of these, 182 appear in the actual data word, 13 are used for the tag section for pulse counting and PRI computation and 13 are not used.

Figure 4.6-24 shows the data word formats, as read out and as stored in the cores. The section designators shown refer to the state of the Section Counter which results in the

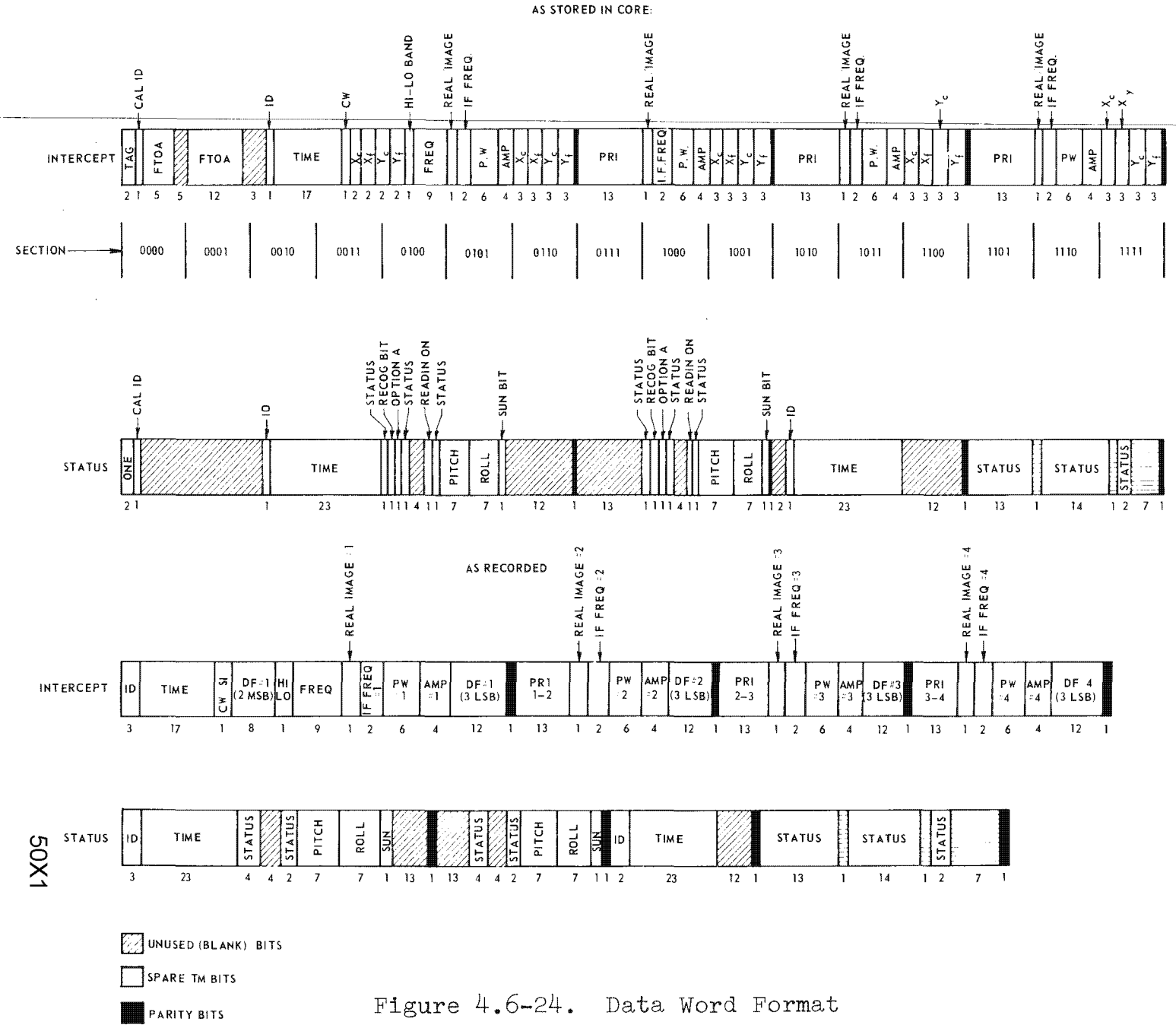

Figure 4.6-24. Data Word Format

selection of the particular group of thirteen cores. A total of 64 such data words can be stored in the complete memory.

4.6.9.5 Memory Organization, Recognizer

The Recognizer Memory is shown in simplified block diagram form in Figure 4.6-25. The core stack consists of 14 planes, each containing 32 cores, arranged in a 4 x 8 array to provide a storage capacity of 448 bits. The X axis wires are divided into two groups of four wires each and are selected by two drivers and four switches. The Y axis wires are divided into two groups of two wires each and are selected by two drivers and two switches. The fourteen Z axis drivers are connected with the inhibit functions individually available to the logic and the reset inputs combined into two groups of five drivers and one group of four drivers. Fourteen sense amplifiers, one for each plane, provide the data readout to the storage buffer in the Recognizer logic. During the memory Readin mode the memory is sequentially addressed by the thirty-two decoded states of a five stage ripple counter. In the Search mode this counter is modified logically to provide the sixteen addresses for readout of the eight sets of frequency limits. The addressing of the memory during the portion of the frequency dwell when SI signals are being received is controlled by the set identification codes of those sets which previously indicated a favorable comparison. This information addresses the sixteen memory locations where pulse width and PRI limits for the eight parameter sets are stored.

50X1

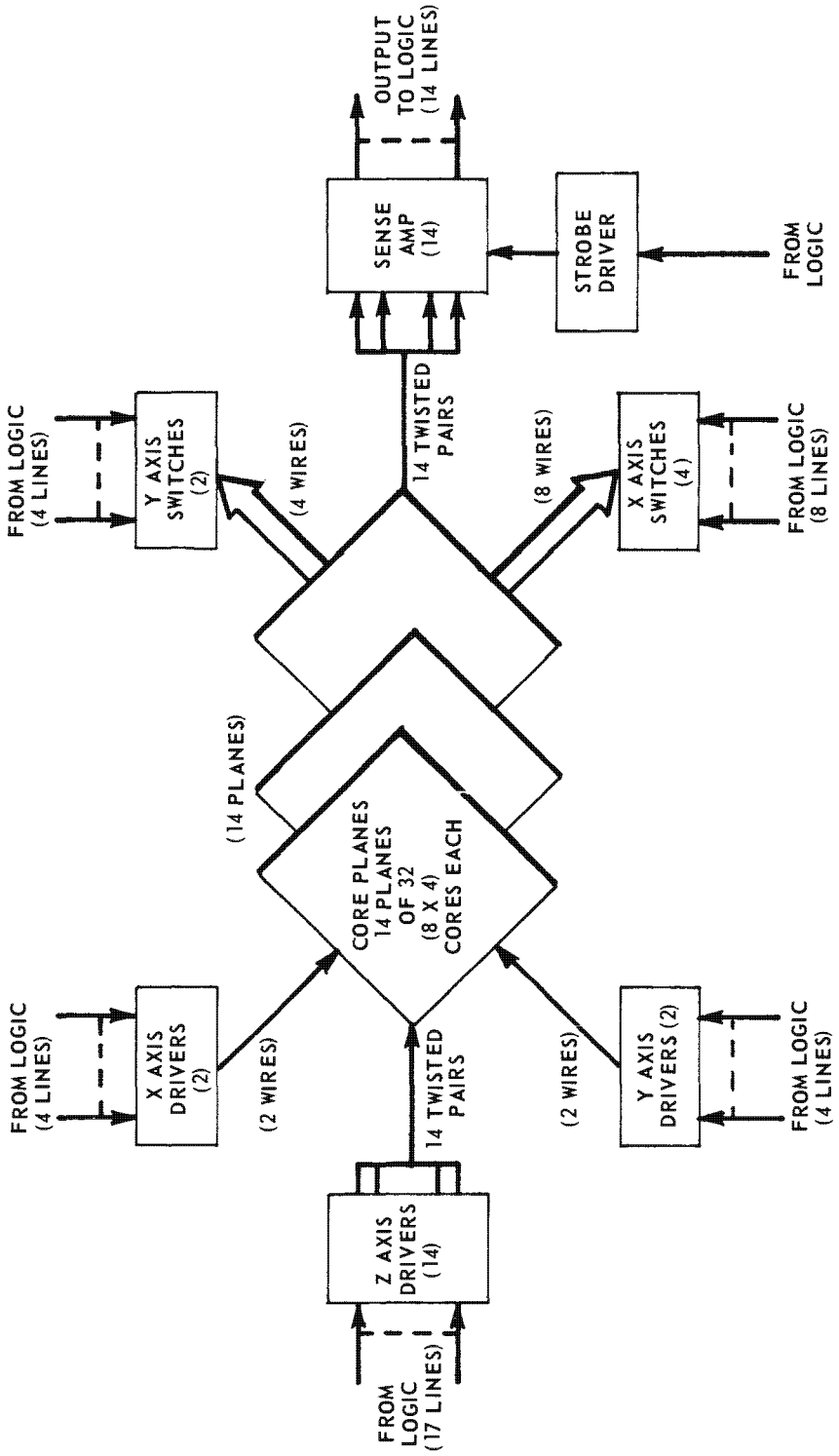

FIGURE 4.6-25 RECOGNIZER MEMORY

50X1

4.6.10 System Clock

4.6.10.1 Oscillator Circuit

The System Clock Oscillator (4124-64214) is basically a crystal controlled oscillator whose output is counted down by flip-flops to the desired frequency. In order to meet the data handler speed requirements, the clock frequency had to be 8 megahertz.

The oscillator developed on the Setter I program is 8.388608 megahertz. In order to take advantage of the existing oscillator design and stabilization circuits it was decided to utilize this design with slight changes to achieve a frequency of 8.0 megahertz. Figure 4.6-26 is a block diagram of the system clock.

The basic oscillator circuit chosen for use was the Colpitt's due to its simplicity. A buffer amplifier circuit was used to isolate the oscillator proper from the remaining stages. A zener diode was used to maintain a constant supply voltage for the oscillator stage. The output of the buffer amplifier drives the wave shaping circuit which consists of saturating amplifiers.

The various timing signals needed for System operation are obtained from the appropriate stage of the counter driven by the 8 MHz output. The Colpitt's oscillator provides the necessary frequency stability through temperature. All components are standard items and the only adjustment necessary

50X1

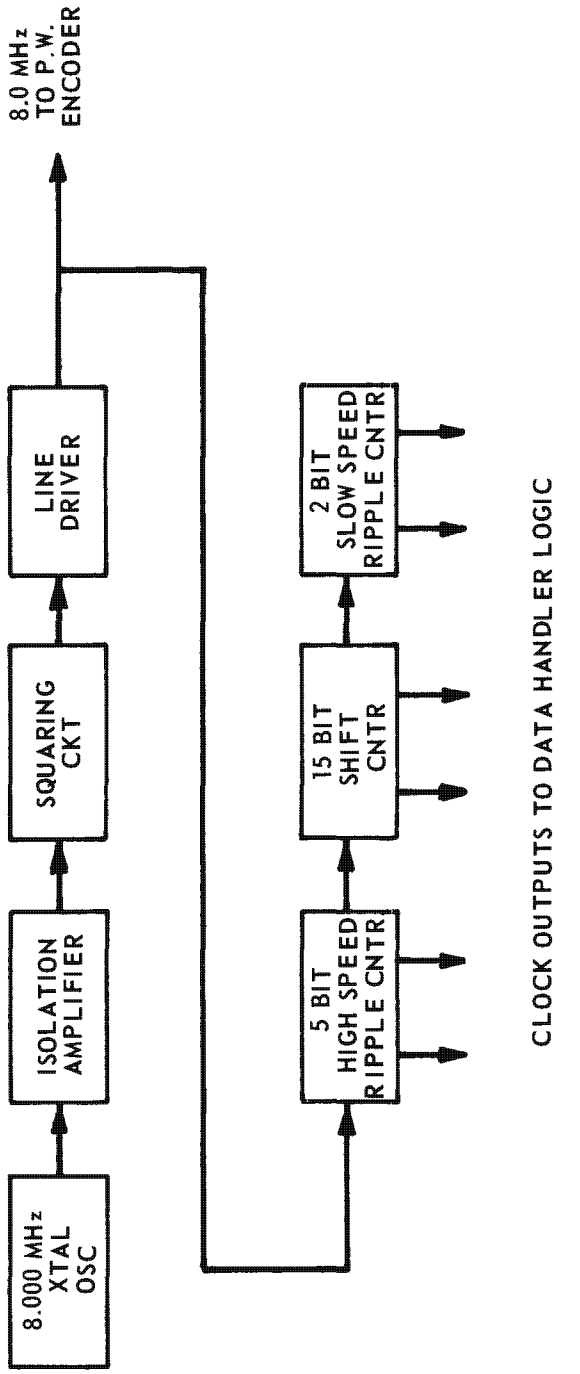

FIGURE 4.6-26 SYSTEM CLOCK

50X1

in the initial set-up of the oscillator was that for fine frequency adjust. This adjustment varies the crystal load capacitance slightly which sets the crystal to an exact frequency of 8.000 MHz. Variation of frequency with temperature is so slight as to have negligible effect on system performance, and need not be calibrated since this source is no longer used to drive the Time Encoder.

4.6.10.2 System Clock Divider Chain

The first link in this divider chain is a 5 bit high speed ripple counter located on card A8A (4124-64208). Five Fairchild 950 flip-flops are used to give good waveshape and high reliability at the speeds required for these stages.

The remaining stages on this card form a 15 bit single propagate shift counter. The single propagate feature requires some extra gating, but is necessary to provide outputs for the PRI encodes which will remain stable during the sample time and which will give a one microsecond resolution on the sample. This is discussed in more detail in the section describing the PRI Encoder. The flip-flops used in the 15 bit shift counter are Fairchild 948 J-K type.

The two stage slow speed counter was added to provide clock pulses which occur at a slower rate than the 8 pps Time Encoder Clock. The time encoder outputs were to be used originally but due to asynchronism between the time update and the system clock it was necessary to extend the system clock

chain. These two stages are located on card A6B (4124-64261), and consist of two Fairchild 9040 flip-flops.

50X1

4.6.11 Pulse Width (PW) Encoder

4.6.11.1 Introduction

The pulse width encoder has three basic functions: (1) to provide an IF actuate (IFA) signal to the IF deck; (2) to encode the pulse width (PW) of the signal indicate (SI) output of the IF deck; and (3) to provide the IF deck with a command change to CW inhibit operation. IFA is provided whenever the data handler is ready to accept pulse data. The PW of the SI is encoded, linearly, with a resolution of 0.25 microseconds or better from 0 to 8 microseconds. CW inhibit is commanded when four signals of 24.0 microseconds or greater duration occur in one frequency step.

The Pw encoder as shown in the block diagram of Figure 4.6-27 consists of an IFA generator, an 8 MHz discrete component gating circuit, a PW counter, and a CW event counter. The discrete component gating circuit is located on the System Clock Oscillator Card, A5(4124-64214). Remainder of the logic is on card A7A (4124-64207).

4.6.11.2 IF Actuate (IFA) Generator

The IFA generator consists of an R-S flip-flop (Z18C and Z26D) and gates Z268, Z26C, and Z27. The IFA output (pin 13) is normally high. It goes to ground while the data handler is in the local oscillator delay time, is processing a time attitude word, or at the end of SI if processing is incomplete. The IFA also goes to ground if SI remains up

50X1

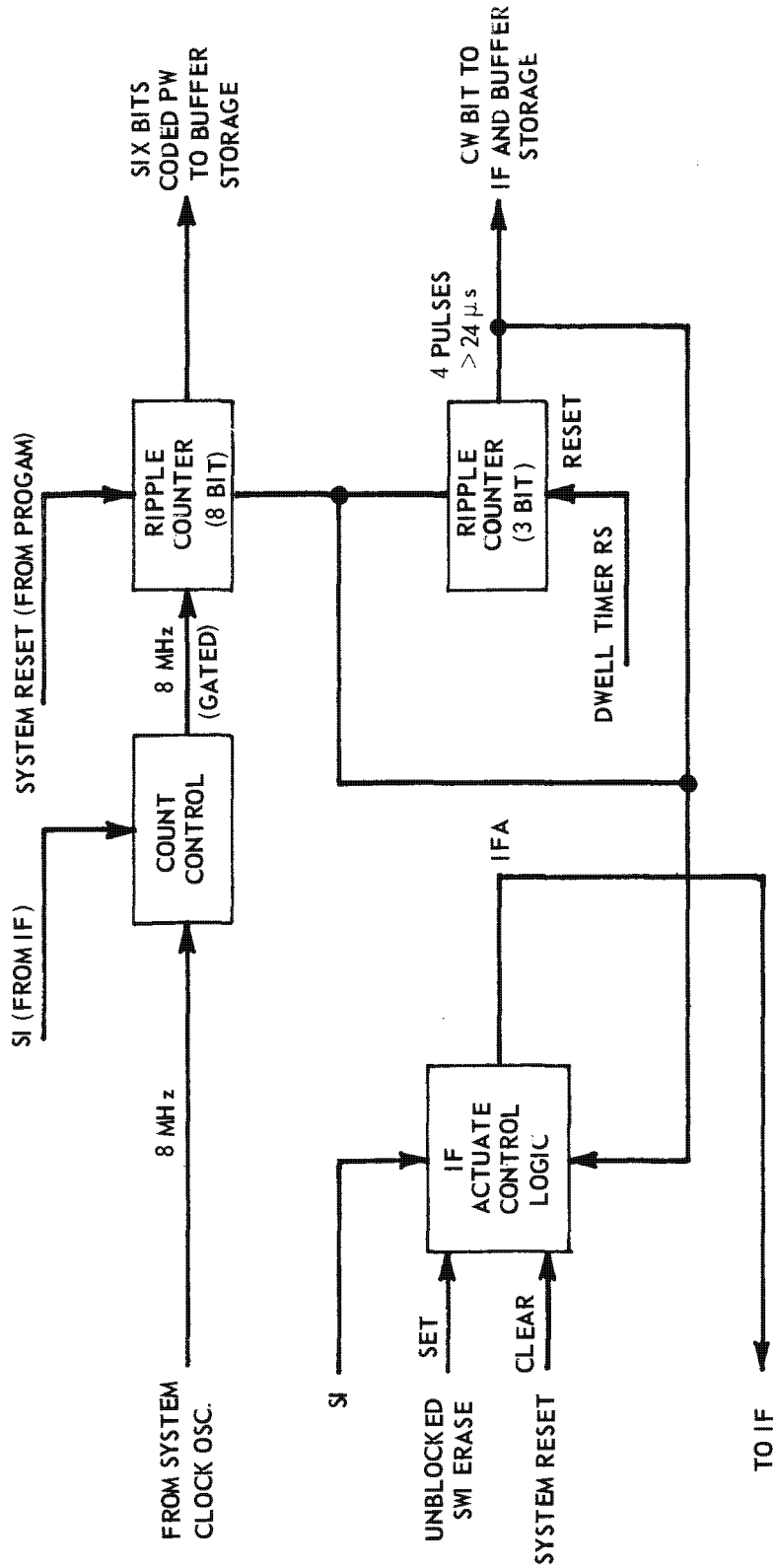

FIGURE 4.6-27

PULSE WIDTH ENCODER

50X1

for more than 24.0 microseconds. When IFA goes to ground, it disables the outputs of the IF deck.

The flip-flop is set by a ground-true SWI ERASE signal from the programmer (pin 7) or by SI (pin 5). The flip-flop is cleared by a ground true SYSTEM RESET signal from the programmer (pin 27). With the flip-flops set and $\overline{SI}$ high, the output of gate Z26C goes to ground, driving Z27B high and Z27A (IFA) low. Gate Z26B receives a positive-true (system reset +A+B) signal (pin 17) and inverts it for a wired OR with Z26C. This holds IFA low during SYSTEM RESET and during Programmer Control Counter State 1-6. Gate drives the other input to gate Z27B if counter flip-flops Z18B and are both in the ONE state, indicating that the SI has been up for 24.0 usec.

4.6.11.3 Pulse Width (PW) Counter

The PW counter is an eight-bit binary ripple counter. The input is the gated 8.0 MHz output of the discrete component gating. For reliable counting, ac coupled DTul 950 flip-flops are used for the first three bits (Z1-Z3). The remainder (Z4 through Z8) are dc coupled DTul 948 flip-flops. The outputs of the counter are gated to produce a direct reading of counter contents for pulse widths less than 24 microseconds. Output is all ONES for pulse widths greater than 24 microseconds.

4.6.11.4 CW Event Counter

The CW event counter generates the CW indicate signal to the IF deck. It consists of a three bit binary ripple counter (Z15-Z17). The input to the counter is the 24.0 microsecond. PW signal (Z18B) inverted to positive-going by Z25A. When four such input pulses have been received, Z17 clocks to the ONE state. When the ZERO output of Z17 goes to ground, the asynchronous SET input to Z15 sets, and holds Z15 in the ONE state, blocki g any further input pulses. At the same time, the output of Z9B goes high (pin 3) sending the CW mode command to both the IF deck and the buffer storage. The counter is cleared by a Dwell Timer Reset (pin 21) from the programmer, inverted by Z18B.

4.6.12 Time Encoder

The Time Encoder (4124-64213) consists of a 20 stage eighths-of-seconds counter and a 3 stage days counter. In normal operation, the counters are operated in tandem, forming a 23 bit counter which gives elapsed time in eighths-of-seconds up to maximum of 8 days. In addition to providing elapsed time data for use by the Buffer Storage, the Time Encoder provides a 16 second clock to the TAW logic and a 256 seconds clock to the calibrator logic.

The Time Reset Function is generated on card assembly 4124-64246 (pin 63) every 86,400 seconds (one day), providing a 24 hour time base for the eighths-of-seconds counter. When this reset occurs, the last stage of the eighths-of-seconds counter is cleared from a one to a zero, advancing the 3 bit days counter one count.

The 8 Hz clock to the Time Encoder is received from the vehicle on card assembly A35 (4124-64248) pin 31. An integrator circuit on this card rejects noise spikes of less than a specified pulse duration. Output of this integrator is gated by the Buffer Storage Load Command (while the system is processing) by the time update logic on card assembly A9 (4124-64246). This gating prevents an update of the Time Encoder during the period when data is being sotred in the Buffer Storage memory. If an update were allowed to occur during data storage, errors in the Time data could

occur. Output of the gating logic (A9-75) is also used to synchronize the Time Reset logic so that the Reset occurs precisely at the time when the counter would normally advance. This prevents gaining or losing a clock pulse when the eighths-of-seconds counter is reset.

An initial clear signal received from the vehicle can be used to clear both the eighths-of-seconds counter and the days counter.

All Time encoder logic is on auxiliary power and is unaffected by turn-on or turn-off of the system main power.

50X1

4.6.13 Attitude Encoder

The vehicle pitch and roll information is generated in analog form, but the processing of data is accomplished in a digital system. For this reason it is necessary to convert the pitch and roll information to digital form. This function is performed in the attitude encoder which consists of two identical analog to digital (A/D) converters. One of the A/D converters is used to convert the pitch information while the other converts the roll information. Since both encoding channels are identical, the following discussion shall be limited to one of the A/D converters.

The A/D converter is of the voltage amplitude to pulse width type. That is, a given analog voltage amplitude corresponds to a certain pulse width which, in turn, is used as a control variable to determine the number of clock pulses

counted by a standard binary counter. Varying the amplitude of the analog voltage will cause the control gate width to vary which in turn varies the number of clock pulses gated to the binary counter.

Figure 4.6-28 is a simplified block diagram of the Attitude Encoder. The principle of operation is as follows: A "start encode" signal is applied to the delay one-shot and the binary counter simultaneously. This action causes the counter to be reset to count 0000000. The delay one-shot changes states causing the NAND gate to be inhibited. At the same time, the flip-flop is set causing the ramp generator to start its cycle. As soon as the delay one-shot relaxes back to its stable state the NAND gate is enabled allowing the clock pulses to be gated through to the counter. The clock pulses will be forwarded to the counter until such time as the ramp voltage has increased to the point where it is equal in amplitude to the value of the analog voltage signal. A pulse is generated by the voltage comparator when the two inputs are equal, or as they do in practice, differ by a small fixed amount. This coincidence pulse triggers the flip-flop to its original "off" state. The flip-flop, in turn, resets the ramp generator and inhibts the NAND gate so that the clock pulses are no longer gated through to the binary counter. The counter has recorded in binary form the number of clock pulses forwarded to it by the NAND gate. This binary number, then,

50X1

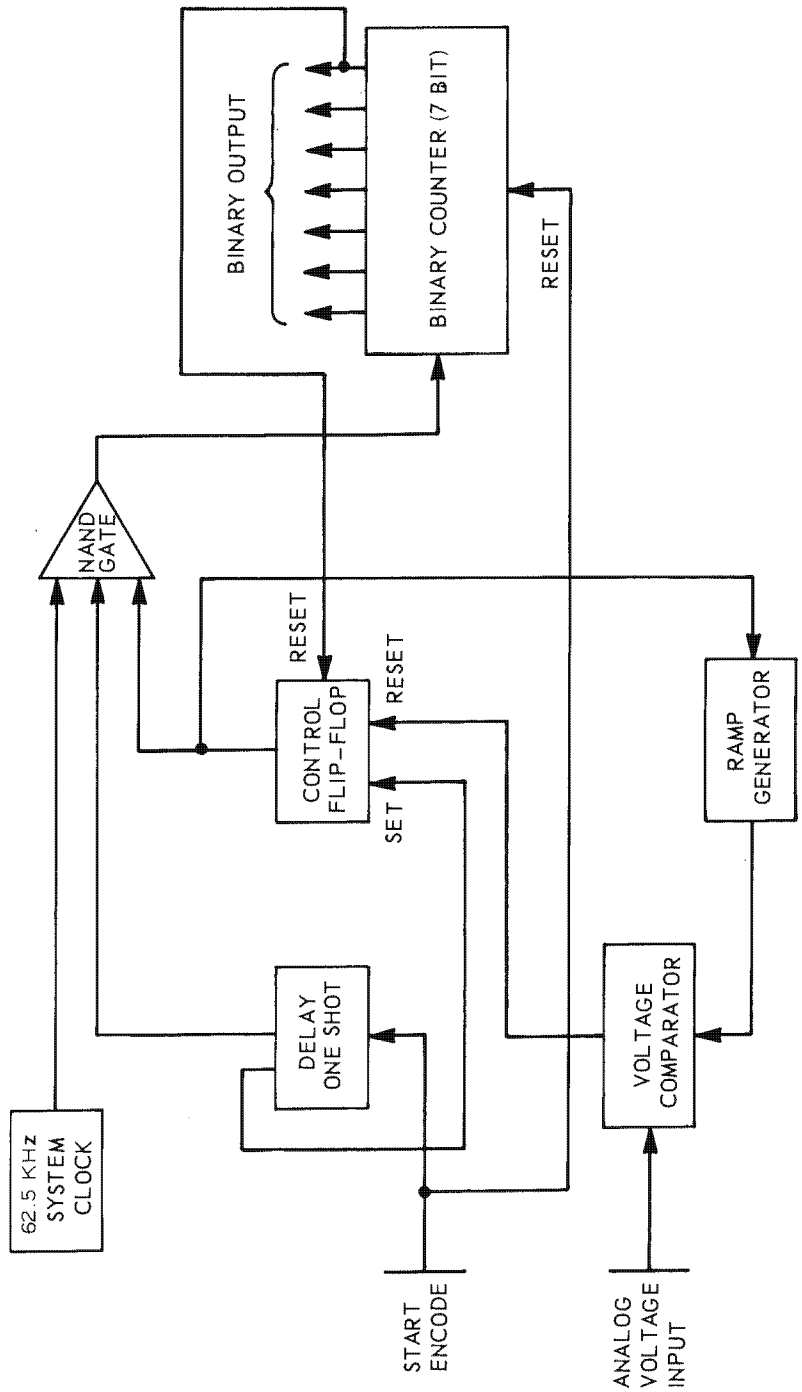

FIGURE 4.6-28 ATTITUDE ENCODER

50X1

is a direct representation of the amplitude of the analog voltage signal. The encoding cycle is now complete and the converter is ready for the next start encode command.

Figure 4.6-29 is a simplified schematic of the linear ramp generator which is a bootstrap integrator circuit. During standby, Q1 and Q2 are saturated and the generator output is at a small positive potential. During a portion of this period the small charge of C2 which was lost during the previous encoding cycle is replaced. A start encode signal causes Q2 to become cut off and the ramp voltage starts to increase. Since C2 is connected through the base-emitter junction of Q1 to the ramp potential, a bootstrap action occurs. This action results in a constant potential being held across R. This causes a constant current to flow to C with resulting in a linear voltage built up across C with respect to time.

Figure 4.6-30 is a simplified schematic of the voltage comparator. This circuit is derived from a Schmitt trigger circuit except that as a result of the requirement for high input resistance, the feedback loop is coupled through the capacitor C_1. During standby both junctions of Q_1 are reverse biased. When an encoding cycle is started the ramp signal increases the emitter voltage of Q_1 until its emitter becomes forward biased and transistor action occurs. Regeneration results producing a negative going pulse with a fast rise time at the output.

50X1

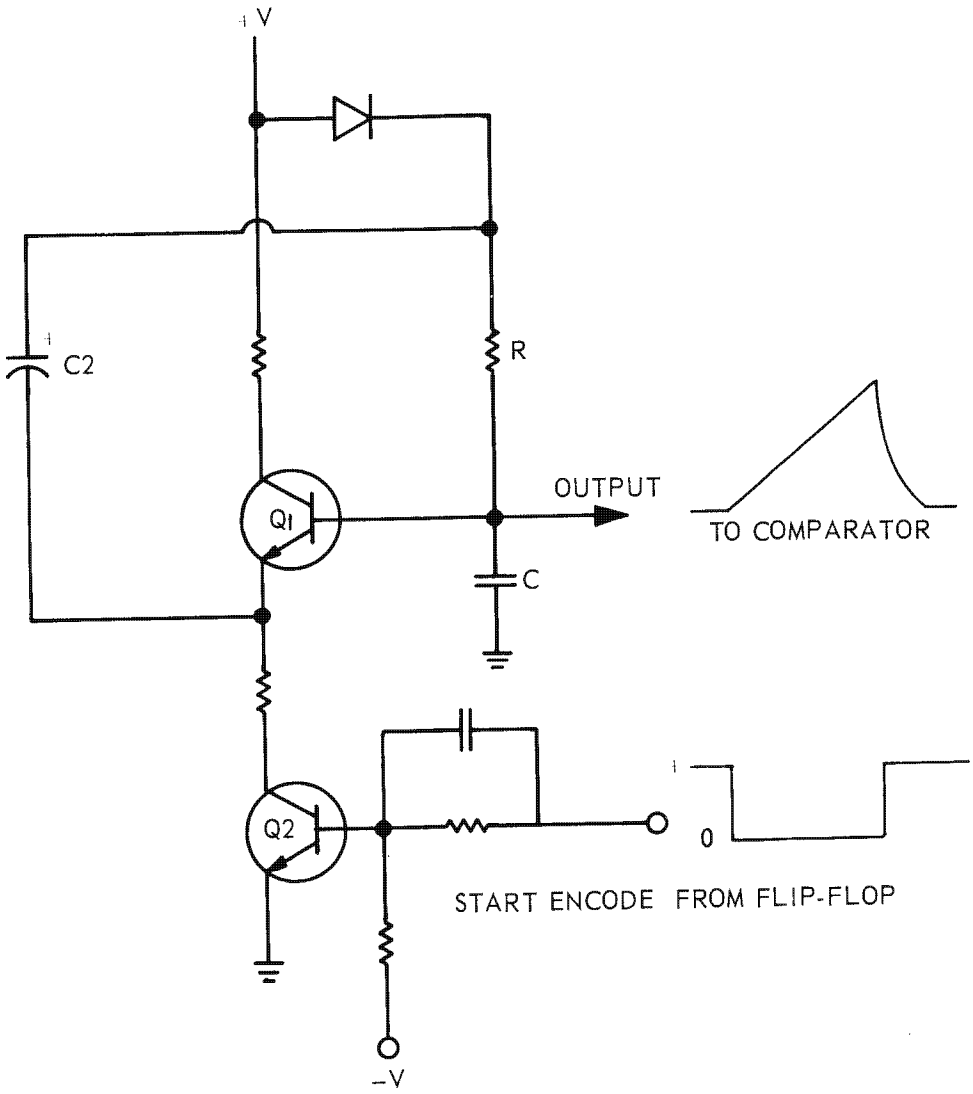

FIGURE 4.6-29 RAMP GENERATOR

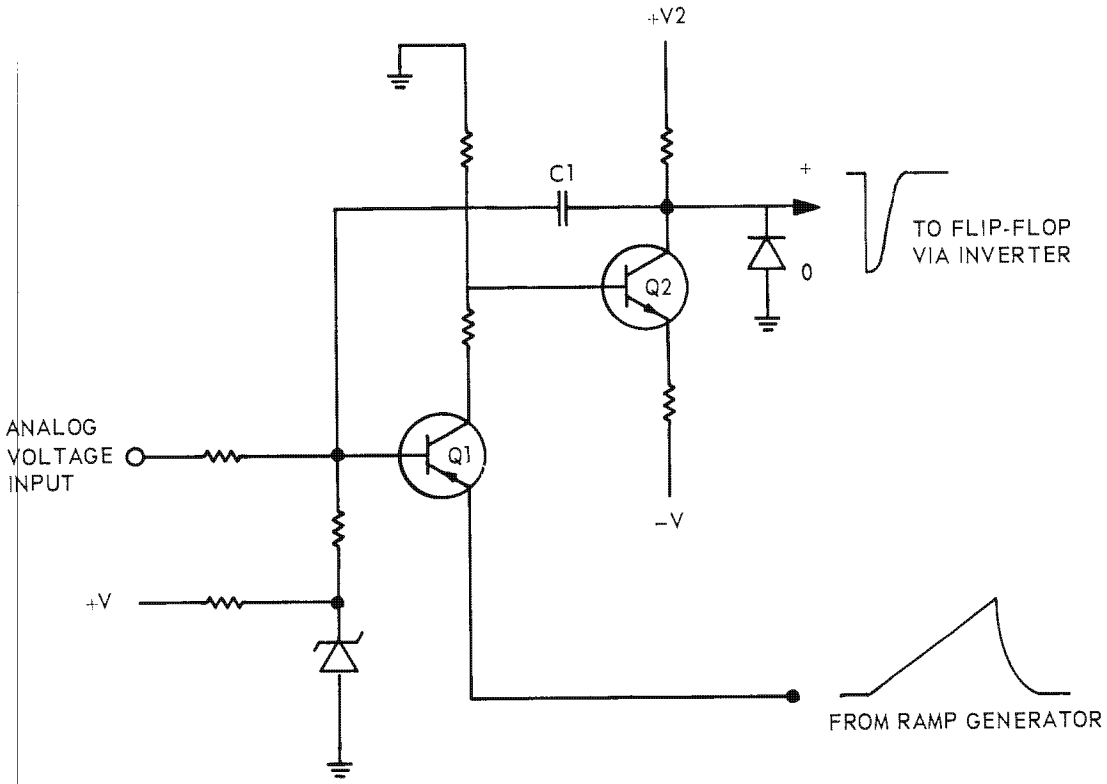

FIGURE 4.6-30 VOLTAGE COMPARATOR

50X1

While the analog signal voltage limits are ± 10 VDC for the encoder, the input voltage is capable of taking on the extreme values of ± 14 VDC. The values less than -10 VDC and greater than + 10 VDC must be discriminated against in order that they cause no overrun of the counter. In order that voltage inputs in excess of + 10 VDC can have no effect on the output information, +10 VDC was made to correspond to the binary count 1111111. When the input voltage exceeds + 10 VDC the next clock pulse counted causes the counter to read 0000000. At the same time a pulse is generated which sets the control flip-flop to its "off" state causing the clock pulses to be blocked from the counter. The result is that the count 0000000 means that a voltage limit, either upper or lower, has been exceeded and no more clock pulses shall be counted.

If the input voltage decreases beyond -10 VDC the base-emitter junction of Q_1, Figure 4.6-30 becomes forward biased. The result is that the comparator oscillates. In order that the counter does not record an erroneous count, the period of the delay one-shot was made greater than the period of oscillation of the comparator. In effect, this means that all voltages less than -9.842 VDC are blocked from the counter.

4.6.14 Test Generator Logic

The function of the calibrator is to generate an RF signal of known characteristics, i.e., pulse width, amplitude, repetition interval, phase, etc., which can be processed by the system in the same manner as any other signal. This allows the System performance to be checked during intervals when other data is being received.

The calibrate signal generator shown in the block diagram of Figure 4.6-31 generates a pulse train which is used to modulate the cal oscillator. Output of this oscillator is fed into a mixer board in the RF section and processed like any other signal. The phase, amplitude, etc., of this signal is essentially the same for each pulse generated, and readouts for these parameters in the data words can be used to check operation of the circuits which measure them.

Very little power is consumed by the calibrate oscillator as its supply voltage is switched on only during the interval in which cal pulses are being generated. This is only 4 milliseconds during each dwell period for a duration of 8 seconds. These 8-second bursts occur once each 256 seconds. (See Waveforms in Figure 4.6-32). The conditions which initiate generation of cal pulses are:

1. Cal time buffer set (every 256 seconds).
2. 16 second clock HIGH.
3. Cal sample pulse received from Programmer.

50X1

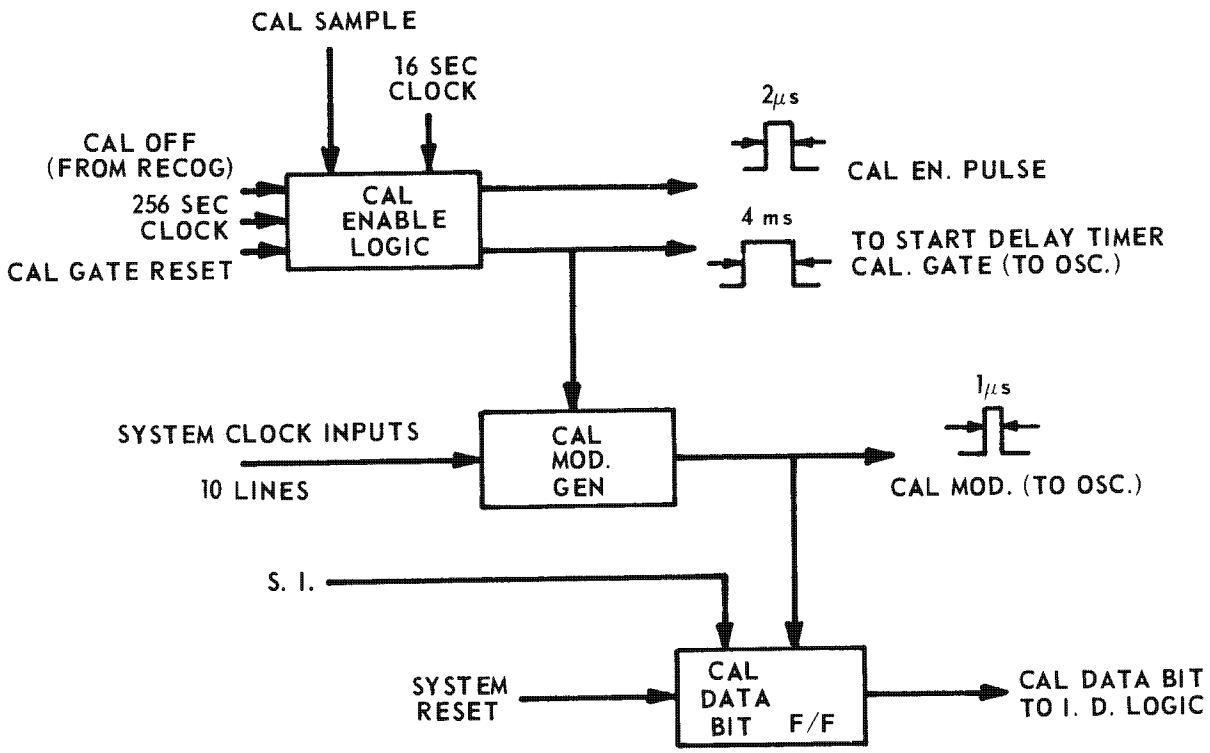

FIGURE 4.6-31

CALIBRATE SIGNAL GENERATOR, BLOCK DIAGRAM

50X1

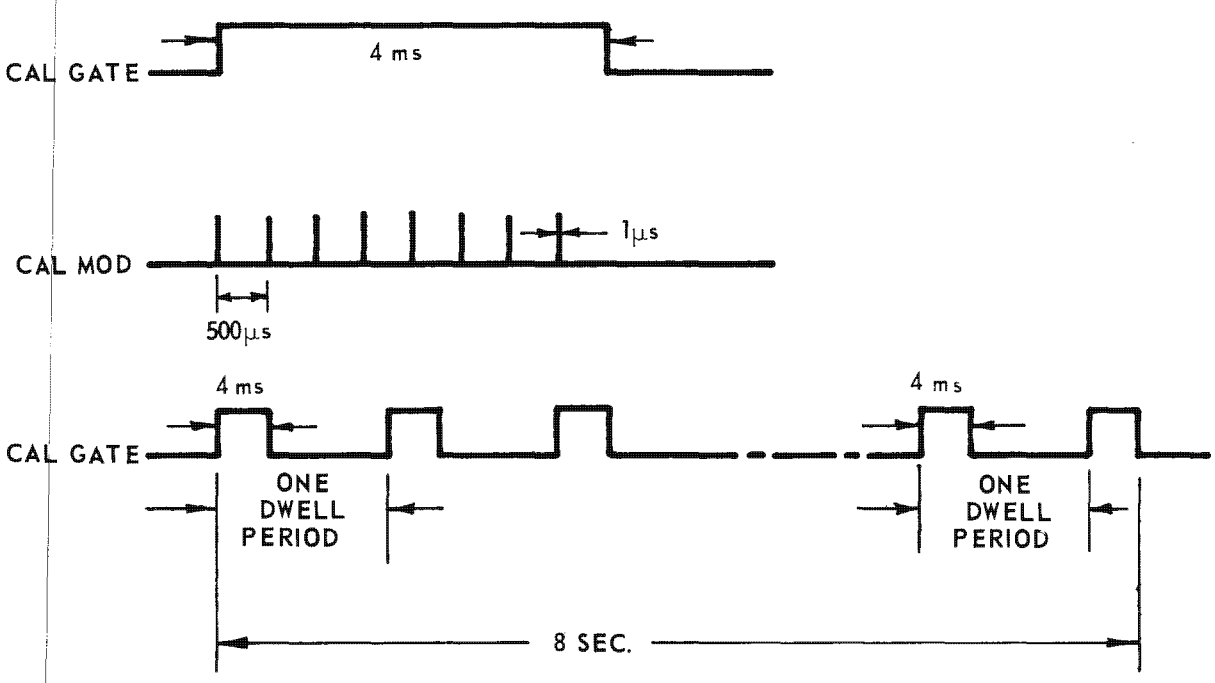

FIGURE 4.6-32

CALIBRATE SIGNAL GENERATOR, TIMING DIAGRAM

50X1

50X1

4. Cal is enabled (No Recognizer Match).

It can be seen from this list that initiation of enable and modulation pulses to the calibrator oscillator are independent of frequency. The reason for this is that the burst of enable pulses is of sufficient duration (8 seconds) to cover at least one complete scan of both frequency bands of the local oscillator. Since the output of the oscillator is spectral lines occurring each 120 frequency steps, the system processes calibrate pulses on only these stops, even though the oscillator is being enabled and modulated on every frequency stop in both bands.

The enable level (Cal Gate) has a 4-millisecond duration during which a burst of 8 cal pulses are generated. Nine outputs of the System clock are used by the output gating to generate the proper pulse width and repetition interval for the cal pulse train. These parameters have been chosen to be 1.0 and 500 microseconds, respectively. The burst of eight cal pulses occurs during the first four milliseconds of each dwell period.

Distinction between data words and normal intercept words is provided by a 000 I.D. in the data word format. Whenever a cal pulse is generated, the Cal Data Bit F/F is set. When the system finishes processing the pulse, the buffer is cleared by a system reset. Thus the 000 I.D. appears only in those data words which contain the parameters of the calibrate

signal. Other pulses interleaved with cal pulses will also be processed, but will not contain the cal I.D.

The calibrator logic is implemented on card A9A - Assembly No. 4124-64246.

50X1

4.6.15 Data Handler Interface Logic

The interface circuitry is necessary to make the Data Handler compatable with equipment external to the Reaper system. These circuits consist of discreet components and are all contained on a printed circuit board placed in location A35 of Assembly A43. Refer to Drawing No. 4124-64 . The interfaces consist of the following circuits:

(a) Command Computer Interface

The information that is loaded into the Recognizer memory or the partial scan memory is transmitted to the Data Handler via a "1" line and a "0" line. For example, when it is desired to write a "1" in the memory a pulse is generated on the "1" line. By the same token , a pulse on the "0" line represents a "0". The Interface to the Data Handler is identical for both the "1" and the "0" lines and consists of an inverter which converts the input pulse levels to value compatable with the Reaper logic.

(b) Three Level RZ Converter

The 3LRZ Converter is used to convert the bilevel binary information signals at its inputs to a binary signal having three distinct voltage levels for transmission to

the DSU. The three output levels of the 3LRZ converter are nominally +6.0 volts, 0 volts, and -6.0 volts. A 50 usec +6.0 volt pulse represents a logical one while a 50 usec, -6.0 volt pulse represents a logical zero. After each logical one or zero, the output returns to a level of 0 volts. This system is therefore self-clocking, i.e., it requires no clock signal to differentiate between a logical one and a logical zero. This circuit will develop a 6.0 volt pulse across an external resistive impedance of 3.75K ohms minimum. A truth table relating the inputs of the 3LRZ converter to its output is shown in the following table:

TABLE 3 LRZ CONVERTER

4124-64248

INPUTS		OUTPUT
PIN 75	PIN 73	PIN 77
0	0	0 volts
0	1	-6.0 volts
1	0	+6.0 volts
1	1	0 volts

50X1

(c) Time Input Interface

This circuit provides a load impedance of 22 $\pm$ 4.4 KΩ and converts the 6 volt input pulse to levels compatable with the Reaper time encoder. It further insures that input pulses of 6 volts amplitude having pulse widths of 10 microseconds or less shall not cause the time encoder to count.

In operation with no input Q5 and Q2 are saturated while Q1 and Q6 are cut off. A pulse at the input causes Q6 of drawing 4124-64 to saturate causing Q5 to cutoff. When Q5 cuts off Q2 also cuts off due to a lack of base drive current thereby releasing the collector of Q1. The collector of Q1 can go "high", however, only if Q1 is also cutoff. The base circuit of Q1 consist of a R-C differentiator thus when Q5 cuts off a positive "spike" is applied to the base of Q1 causing Q1 to saturate and hold its collector voltage at a "low" state. Q1 remains saturated until the charge

on C4 is reduced sufficiently to allow Q1 to cut off. The period during which Q1 is saturated is determined by the R-C time constant of the differentiator and is chosen such that a 10 microsecond pulse at the input of the circuit will not cause Q1 to become cut off. Input pulses of greater than approximately 14 microseconds will allow Q1 to cut off thereby allowing the circuit output to attain a "high" state and the time encoder to record an input.

(d) Relay Driver

The Relay Driver is not an interface circuit but is used to sink the drive current necessary to switch a relay. In operation, the input is held at a low level which keeps Q7 cut off. When the ecognizer receives a "turn off" command it generates a signal to the Data Handler. This action causes the input to the relay driver to "open" thereby causing the current which flows through R15 to be applied to the base of Q7 which then saturates. The collector

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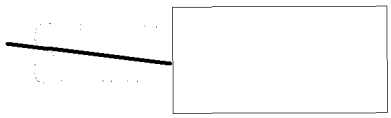

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of Q7 is connected through a relay coil to +28 V D.C. When Q7 is saturated the relay coil is energized causing the logic power to the Recognizer to be disconnected, disabling the Recognizer.

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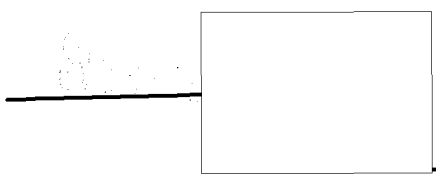

4.6.16 Marker Word Generator

Marker words are 48 bit data words generated by the system for recording on the DSU and for direct readout through the wide band data link. The marker word is identified by a zero in bit 48. Table 4.6-1 shows the format of this data word and figure 4.6-33 shows the functional block diagram. Referring to this figure, note that the marker generator is composed of four block functions: the Control section, the Data Register, the 10 KHz Generator and the 3-level return-to-zero circuit. The marker function is essentially that of loading, in parallel, 48 bits of data into the marker register and then serially shifting this data out and into the 3 LRz converter. This process is initiated when "Recognizer Enable and Recognizer Override" and "DSU Request" are enabled or when "DSU Activate" is enabled. Under these input conditions to the control section (see block diagram) the leading edge of the 8 pps clock triggers a pulse which loads the 48 bit data register. At the same time the 10 KHz shift clock generator is started and the serial shifting of data into the 3 LRZ circuit begins. At this time, a parity bit is injected into the data at bit 47 to provide even parity as required. After bit 48 is read into the 3 LRZ circuit, a "clear" pulse is generated which resets the control function, the register and the 10 KHz shift clock

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TABLE 4.6-1 MARKER WORD FORMAT

BIT NO.	CONTENT		BIT NO.	CONTENT
1	Spare		25	
2	DSU		26	
3	Status		27	
4			28	
5		(MSB)	29	
6	Amplitude		30	
7	Threshold	(LSB)	31	
8	DSU		32	
9	Status		33	
10	Stop Scan		34	Time
11		(LSB)	35	
12	Set ID		36	
13		(MSB)	37	
14	High-Low Band		38	
15		(MSB)	39	
16			40	
17			41	
18	Frequency		42	
19			43	
20			44	
21			45	
22			46	(MSB)
23		(LSB)	47	Parity
24	Time	(LSB)	48	Reaper "0"

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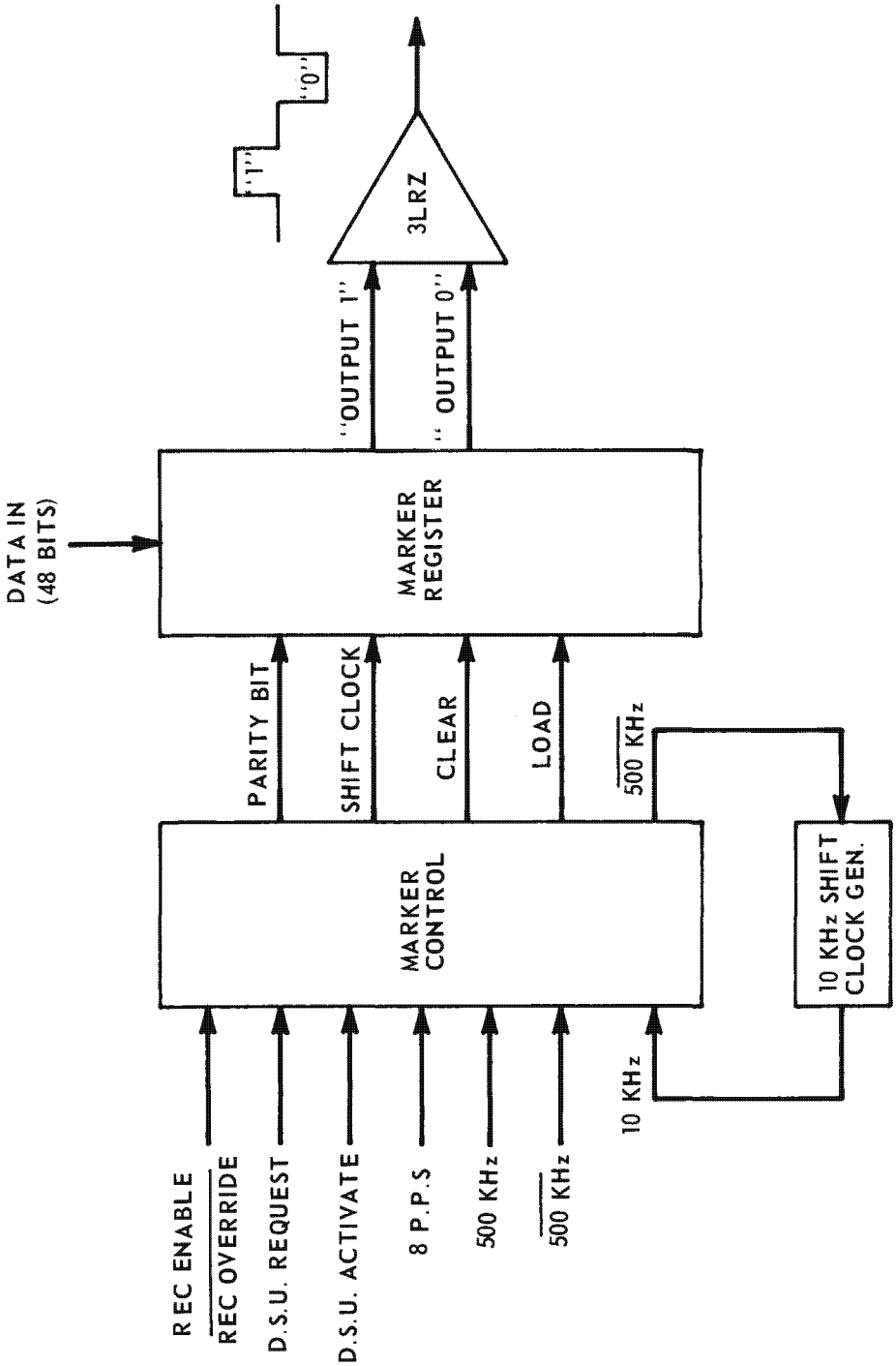

Figure 4.6-33. Marker Word Generator

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generator. All functions then remain inactive until the leading edge of the next 8 pps clock.

A more detailed description of the marker generator function is contained in the following paragraphs. Reference is frequently made to schematics 4124-64 4124-64 4124-64 and 4124-64 .

Marker generator logic A & B card, 4124-64318 contains 47 flip-flops connected as a shift register. These flip-flops are loaded with data in parallel and shifted serially. The most significant bit, the last to be shifted out, is bit 47. This bit is always a zero because of the ground on pin 13 of module Z9 on side 4124-64241.

A parity bit is generated by flip-flop module Z12 on marker generator logic O (card 4124-64243) to provide even parity for the serial output of this register. This bit is inserted into the flip-flop at module Z21 on 4124-64242 immediately following the serial shift of bit 46 into Z21. Bit 46 is always a zero at this point and becomes a "one" only if needed to satisfy even parity.

The purpose of marker generator logic C & D (card 4124-64319) is to generate the controls for marker generator logic A & B shift register 4124-64318. These controls consist of a clear pulse which "resets" all flip-flops (sets pin 9 high); a "Load" pulse which loads a 47 bit data word into the shift register; a shift clock consisting of 47

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square wave pulses supplied at a 10 KHz rate, and a parity bit which is developed by module Z12 on card 4124-64243.

The following is a description of the function of flip-flops located on marker generator logic C card 4124-64243. These flip-flops are identified according to their module number on the board.

F/F Z15 this flip-flop initiates a load/shift operation on the leading edge of each 8 pps clock provided "Recognizer Enable" is high and "DSU Request" is high or provided "DSU Activate" is high. When this flip-flop "sets" (pin 6 goes high) it enables the gate at Z22. This gate will then clock the flip-flops which generate the parallel load pulse (Z17 and Z18 on 4124-64243) on the leading edge of the next 500 KHz clock.

F/F Z17 and Z18 - These flip-flops make up the "parallel load pulse" generator, the function of which is to develope a 2 microsecond negative pulse. Initially F/F Z18 is cleared to "set" (pin 6 is high) and F/F Z17 is cleared to "reset" (pin 9 is high). Upon receiving an enable signal at Z22 (from Z15), the F/F at Z18 "resets" on the leading edge of the next 500 KHz pulse. Upon receiving the leading edge of the next

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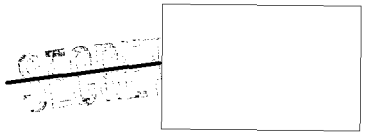

500 KHz clock at Z22, the flip-flop at Z18 sets and simultaneously sets the flip- flop at Z17. This action blocks the gate at Z22, preventing the generation of more than one load pulse.

F/F Z16 - After the F/F at Z17 "sets", this flip-flop "sets" on the trailing edge of the next 500 KHz clock. This action starts the shift clock generator located on marker generator logic D(card 4124-64244).

Shift Clock Generator - This generator consists of seven flip-flops connected as a divide-by-fifty counter. Dividing the 500 KHz input clock by fifty results in a signal at pin 64 (on 4124-64243) which is initially low for 50 micro-seconds after counting begins. This signal then developes 47 positive 50 microsecond pulses at a 10 KHz rate.

Shift Counter - A six bit serial shift counter (modules Z1, Z3, Z4, Z6, Z7 and Z9 on 4124-64243) counts the 50 microsecond shift pulses and detects the 46th pulse (module Z10-6) and the 47th pulse (module Z10-8). The signal at Z10-6 loads the parity bit (if required) and the signal at Z10-8 limits the number of shift pulses to 47 and initiates the generation of a clear pulse (Z14).

F/F M12 - This is the parity flip-flop. It is initially cleared to "Reset" (pin 9 is high) since it is clocked by the "ones" output line from the marker register (Z19-8), it is in the "set" position after an odd number of "ones" is shifted out of the register. After 46 shift pulses, the parity bit will be in the least significant flip flop of the shift register. See 4124-64242 pin 22). It will always be shifted in as a zero. If flip-flop Z12 is "set" at this time, flip-flop Z21 on 4124-64242 will "set". This system always guarantees an even number of ones coming out of the shift register. (Even Parity)

F/F Z13 and Z14 - After the 47th shift pulse is executed F/F Z14 is conditioned for set by Z10-8 and will set on the leading edge of the next 10 KHz clock. When flip-flop Z14 "sets" all flip-flops on marker generator logic card C, 4124-64243, are cleared to "reset". The flip-flops of the shift clock generator are also cleared to reset. On the trailing edge of the $\overline{500\ KHz}$ clock F/F Z13 "sets", resetting F/F Z14. On the next 500 KHz F/F Z13 "resets". The load/shift cycle of the marker generator is

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now complete. One 48 bit data word has been loaded in parallel into the marker generator register and has then been shifted out with a parity bit injected as required. The cycle is now ready to begin again with the next 8 pps clock.

4.6.17 Description of the Operation of the Scan Control Function

The purpose of the Scan Control Function is to control the counting range of the LO counter during the partial scan mode of operation. A choice of two counting ranges is available. Each range may be selected singularly or both ranges may be selected symultaneously. When both ranges are selected, the LO counter will count each range alternately.

The Logic functions required to control the LO counter in the scan mode are contained on "Scan Control Logic A and B" card 4124-64328 (the Scan Control Data Register) and the "Scan Control C and LO counter" card 4124-64316 (The control logic for the scan operation). The block diagram in Figure 4.6-34 shows the relationships between the Scan Control functions. New Scan Limits are loaded into the Scan Register on the "data in 1" and "data in 0" lines. When a Scan enable line ("enable A", "enable B" or both) are raised, the control section selects the appropriate register sections using control lines "enable serial gates" and "isolate registers". This action applies the proper upper limit to the comparator and the proper lower limit to the parallel input bus (9 bits) to the LO counter. The raising of the scan enable line also causes the control section to clear the LO counter and to load into this counter the lower scan limit. The counter then counts C.F.C. pulses until the comparator senses that it has exceeded the upper limit by one count. When this occurs the comparator

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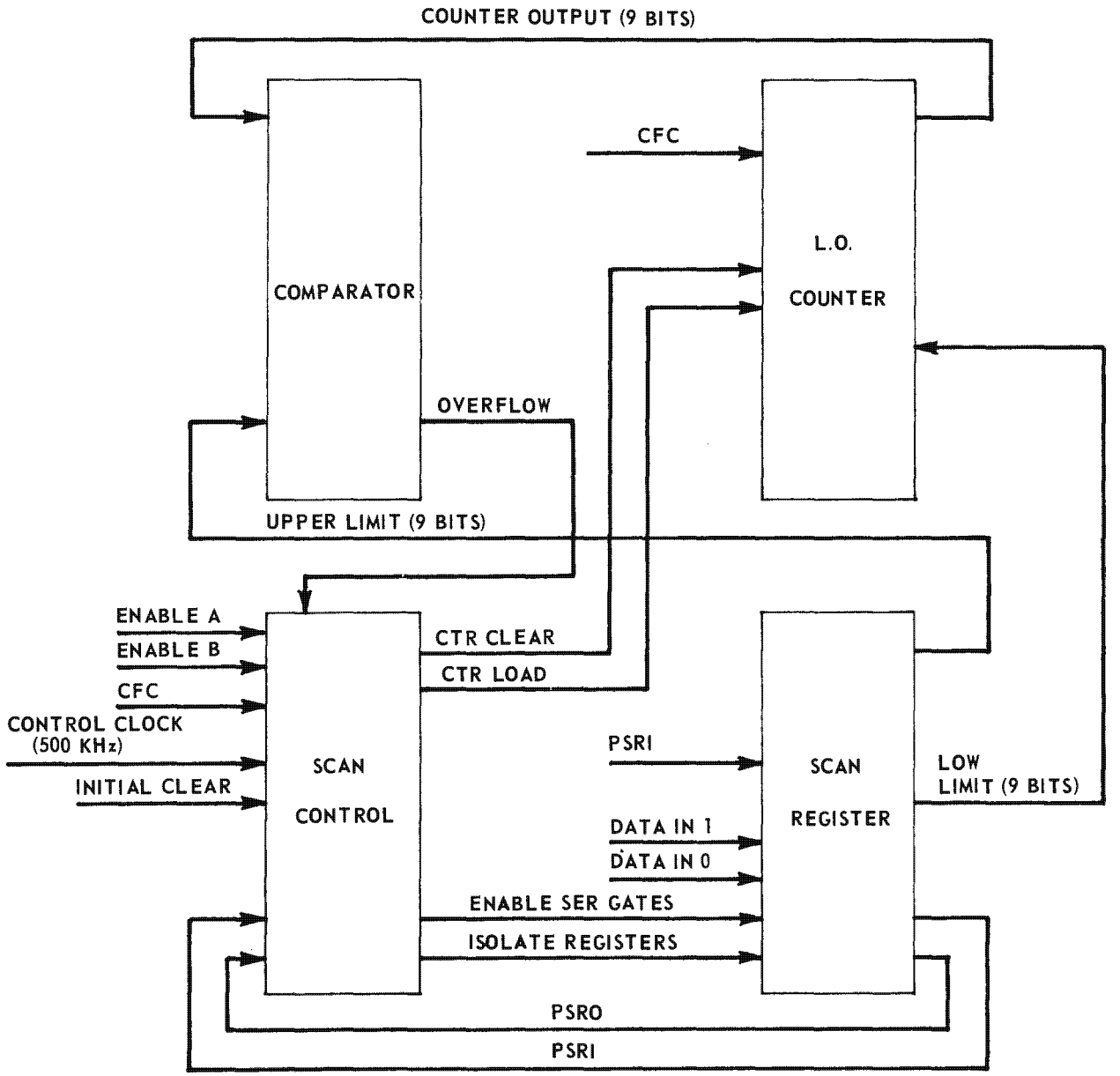

FIGURE 4.6-34 SCAN CONTROL BLOCK DIAGRAM

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puts out an "overflow" pulse. This pulse causes the control section to generate another LO counter clear pulse and another LO counter load pulse. The lower Scan limit is again in the LO counter and the counting cycle repeats.

The following paragraphs describe the scan operation in greater detail. References are made to schematics 4124-6 4124-6 , 4124-6 , and 4124-6 .

Scan Control Logic A and B, 4124-64316, is a Logic Card containing a 36 bit shift register and associated logic. The purpose of the shift register is to contain the data which specifies the counting range of the LO counter when either the Scan A or Scan B operating mode is selected. The 36 bit register is divided into four, 9-bit sections. The first 9-bit section Z1, Z2, Z3, Z4, Z5, Z7, Z8, Z9, and Z10 on 4124-64238 contains the upper counting limit for the Scan B mode. The three remaining 9-bit sections contain "A upper limit", "B lower limit", and "A lower limit" respectively.

The following is a description of the operating modes for which this register is designed.

The partial scan read-in operation consists of loading 36 bits of data serially into the register. This action is initiated when PSRI (Pin 7 on 4124-64238) goes low. $\overline{\text{PSRI}}$ (Pin 66 on 4124-64239) disables the data restore loop of the register preventing interference during the read in operation. Also "enable serial gates" (pins 59 & 78) is held

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high and "isolate registers" (pins 52 & 77) is held low by the PSRI signal to prevent interference during this operation.

The readout command is not initiated on this board. However, when this command is initiated, the "enable serial gates" signal goes high and the "isolate register" signal goes low. Since the $\overline{\text{PSRI}}$ signal is now high (no "read-in" command is present) the data restore loop is enabled. When the 36 readout shift pulses are applied to the registers, the data is simultaneously shifted through the register and restored at the input.

When the Scan A mode is initiated the "isolate register" signal goes high and the "enable serial gates" signal goes low. This places the "A upper limit" and the "A lower limit" on the parallel output bus of the register.

When the Scan B mode is initiated the "isolate register" signal goes low and the "enable serial gates" signal goes high. This places the B upper limit and the B lower limit on the parallel output bus of the register.

The Scan Control Circuit Card 4124-64316 contains a bit comparator, a 9 bit counter, and logic for the control of the Scan Control A & B Card (4124-64328). The overall function of this logic is to control the counting range of the 9 bit LO counter. Four operating modes are possible:

normal operation, Scan A, Scan B and Scan A & B

Normal operation occurs when the LO counter operates within its own pre-set limits and is unaffected by the Scan Control Circuit. These limits cause the counter to count from 0 to 255 or 0 to 360 or alternate between these counts in accordance with, whether low, high or both frequency bands are selected. (Pins 31 & 33 on 4124-64217). During normal operation the counter always resets to zero at the completion of each counting sequence.

The Scan A mode is selected when the "enable A" signal (Pin 62 on 4124-64240) goes high. At this time the F/F at M18 on the Scan Control Logic C Assembly (4124-64240) is set. This action conditions the register located on the Scan Control A & B Assembly 4124-64328, placing the "A upper limit" and a lower limit on the output bus of the register. The 9 bits of the "A upper limit" are dumped into the comparator located on Scan Control C (4124-64240). The 9 bits of "A lower limit" are simultaneously placed on the 9-bit parallel input load bus of the LO Counter awaiting a "load enable" command.

The mode command "Enable A", besides connecting the upper and lower counting limits to the proper circuits, also causes the circuits of the Scan Control C Assembly (4124-64240) to generate a counter "clear" and a counter "load" signal. (See timing diagram, Figure 4.6-35).The clear signal is generated by flip-flops at position Z6 and Z7. The

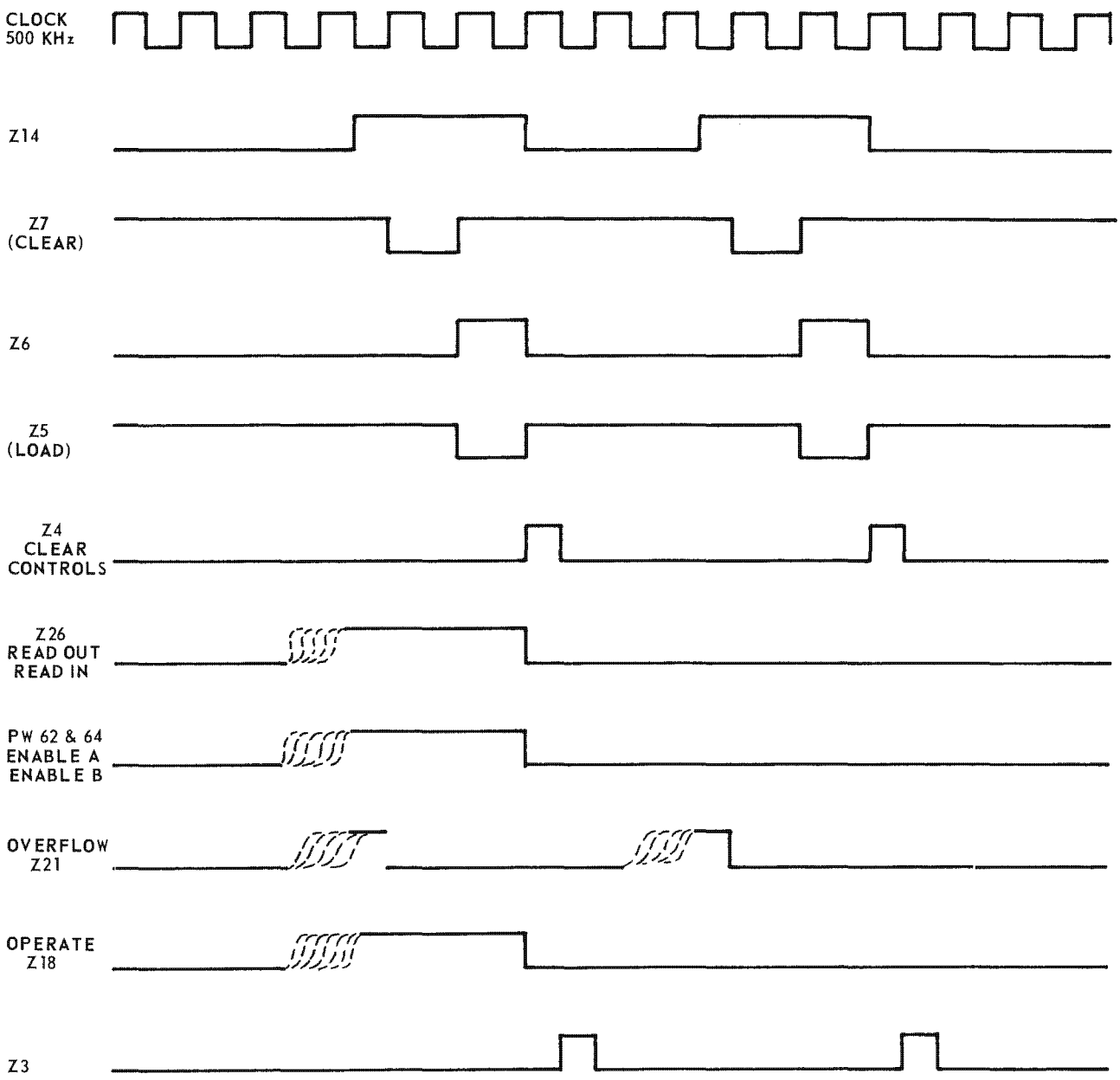

FIGURE 4.6-35 SCAN CONTROL TIMING DIAGRAM

load signal is generated by flip-flops at position Z3, Z4, and Z5.

After the counter is cleared and then loaded with the "A lower limit", it proceeds to count CFC pulses until it has completed one complete dwell time at the upper limit. At this time a positive overflow pulse from the comparator (Z21 on 4124-64240) again sets the flip-flop at Z14 and triggers a new clear/load cycle. The LO counter continues to count between the "A lower limit" and the "A upper limit" as long as "enable A" is high and providing no read commands are executed.

The function of the Scan B mode is similar to the function of the Scan A mode with the exception that the register located on the Scan Control A & B Assembly is conditioned to output the "B upper limit" and the "B lower limit" rather than "A upper limit" and "A lower limit". The LO counter will now count CFC pulses repeatedly between these limits as long as "Enable B" is up.

The Scan A & B mode is generated by raising both "enable A" and "enable B". When this occurs, the flip-flop at position Z18 on 4124-64240 toggles with each overflow signal from the comparator. In the "set" state this flip-flop commands the "Scan A" mode and in the "reset" state it commands the "Scan B" mode. The LO counter now counts alternately between the "A" and "B" limits.

A circuit is included which will detect an over-range condition in the LO counter. This is done by detecting

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that the two most significant bits of the LO counter are true while counting in the high band range. Under these conditions the module at Z12 on card 4124-64240 will clear the counter to zero, preventing an over-range condition which might damage the local oscillator.

Interrupts - The scan modes may be interrupted by any of the following events:

a. Partial Scan read in is executed

b. Partial Scan read out is executed

c. The Scan mode selected is removed

Should event a or b occur during a Scan mode, the overflow pulse from the comparator is blocked from initiating a clear/load cycle. At the completion of the read operation, the LO counter will be cleared and loaded with the lower limit of the mode selected and will count only within this mode range. If both scan modes are enabled at the completion of the read operation, the scan mode in which the LO counter will operate first is that scan mode which was initially interrupted.

Should the Scan mode change (event c) the counting range of the LO counter is conditional as follows:

1. If, while operating in the alternate scan mode (A & B), the lower counting range is disabled while the LO counter is counting in the lower range, the counter will reset to

[redacted]

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the lower limit of the lower range and will continue to count until the upper limit of the upper range is reached. The counter then resets to the lower limit of the upper range and then proceeds to repeat only the upper counting range.

2. If, while operating in the alternate scan mode (A & B) the upper counting range is disabled while the LO counter is counting in the upper range, the LO counter will be immediately cleared and preset to the lower limit of the lower range. The LO counter will then continue to repeat only the lower counting range.

3. If, while operating in the alternate scan mode, a counting range is disabled other than the range in which the LO counter is counting, the LO counter will count undisturbed within the remaining selected range.

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4.6.18 Description of The Relay Assembly (4124-66000)

The Relay Logic provides a means for interfacing commands to the Reaper system from the command programmer. Further, it isolates the Reaper system from the command programmer.

Commands are of two types. Type I commands have a low current capability and meet the following requirements:

True Level:	+22.0 to 29.3 VDC
False Level:	0 to +1.0 VDC
Pulse Duration:	125 $\pm$ 25 milliseconds measured between the 50% amplitude points
Rise Time:	0.5 to 20 milliseconds measured between 10% and 90% amplitude points.
Fall Time:	0.5 to 20 milliseconds measured between 10% and 90% amplitude points
Maximum Current:	150 milliamperes at 29.3 VDC
Maximum Load Inductance:	300 milliheneries at 20 kHz
Minimum Load Resistance:	200 ohms

Type II commands have a high current capability and meet the following requirements.

True Level:	+22.0 to 29.3 VDC
False Level:	0 to +1.0 VDC (OPEN)

Pulse Duration: 135 ± 35 milliseconds measured at the 90% amplitude points

Relay Contact Bounce: 2 milliseconds

The relay box houses 35 latching relays, 2 momentary relays and 4 power switching latching relays. Also included are filter networks for relays located in the command programmer and recognizer unit. The 41 relays are mounted on a metal frame and are serviced by 4 sixty-six pin connectors. Each relay has a filter across the contacts to surpress contact bounce. Also, each relay coil has a diode across it to drain away reverse current generated when it is de-energized. All discrete components are mounted on seven printed wiring boards housed within the frame.

As an example of the way relay commands are generated, refer to relay assembly schematic, Figure 4.6-36 and Table 4.6-2. This command will "reset" k36 (energize the left-hand coil). This places +6 volts on pins 42, 45 and 46 of connector J4. Pin 42 is a TM point. Pin 45 goes to the data handler and pin 46 goes to the IF section. The commands arrive at the relay coils in the form of 125 milliseconds pulses with amplitudes of from +22 to +28 volts. K1 and K2 are momentary relays and will remain closed only for the duration of the command pulse. The remaining 39 relays are latching relays which remain in either of two states depending upon which of

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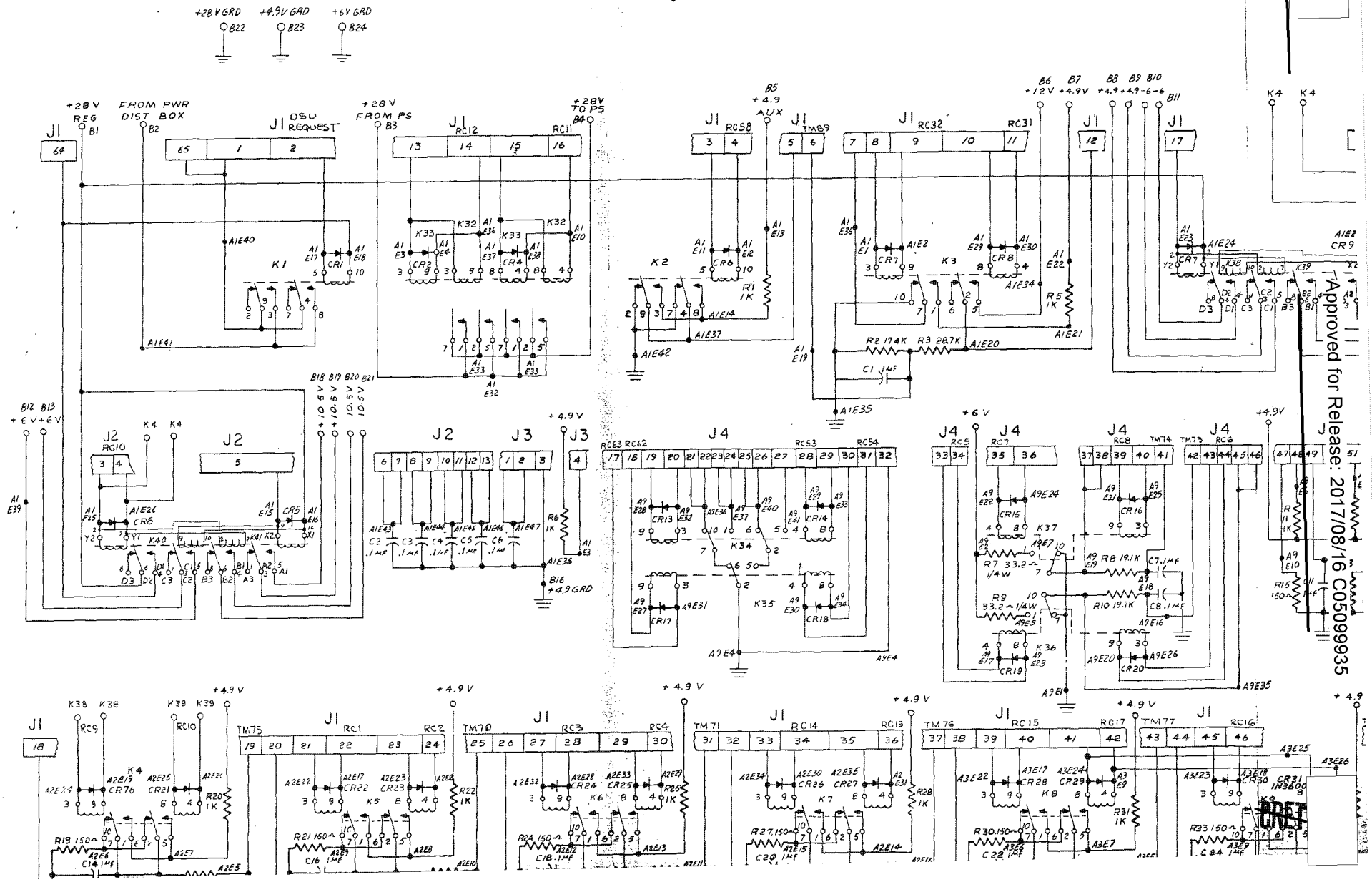

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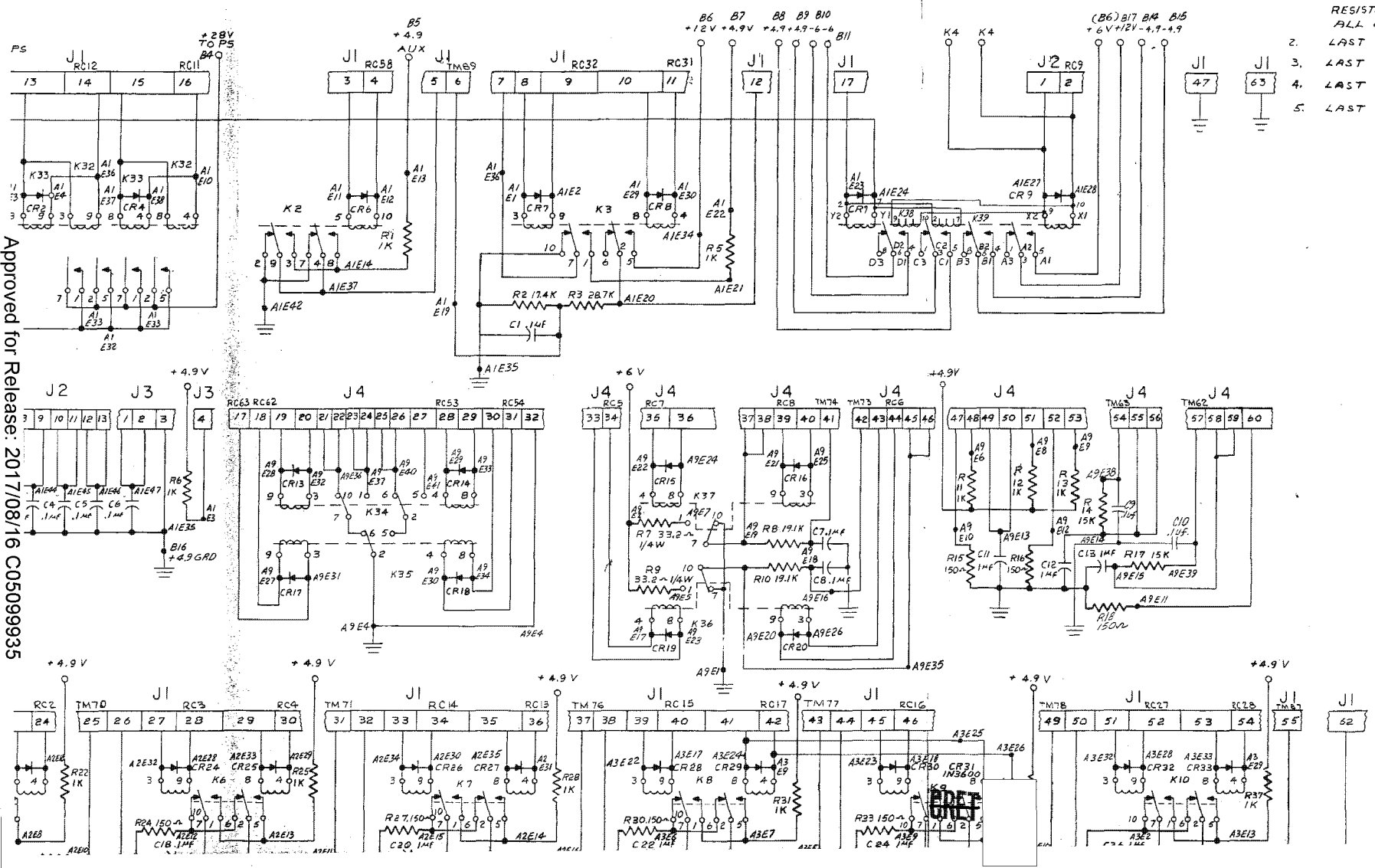
NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL COMPONENTS ARE AS FOLLOWS:
   DIODES ARE IN916A
   RESISTORS ARE 1/8 W, ± 1%.
   ALL CAP 35DCYW
2. LAST CAPACITOR C49
3. LAST RESISTOR R101
4. LAST DIODE CR75
5. LAST RELAY K31



HANDLE VIA BYEMAN CONTROL SYSTEM ONLY

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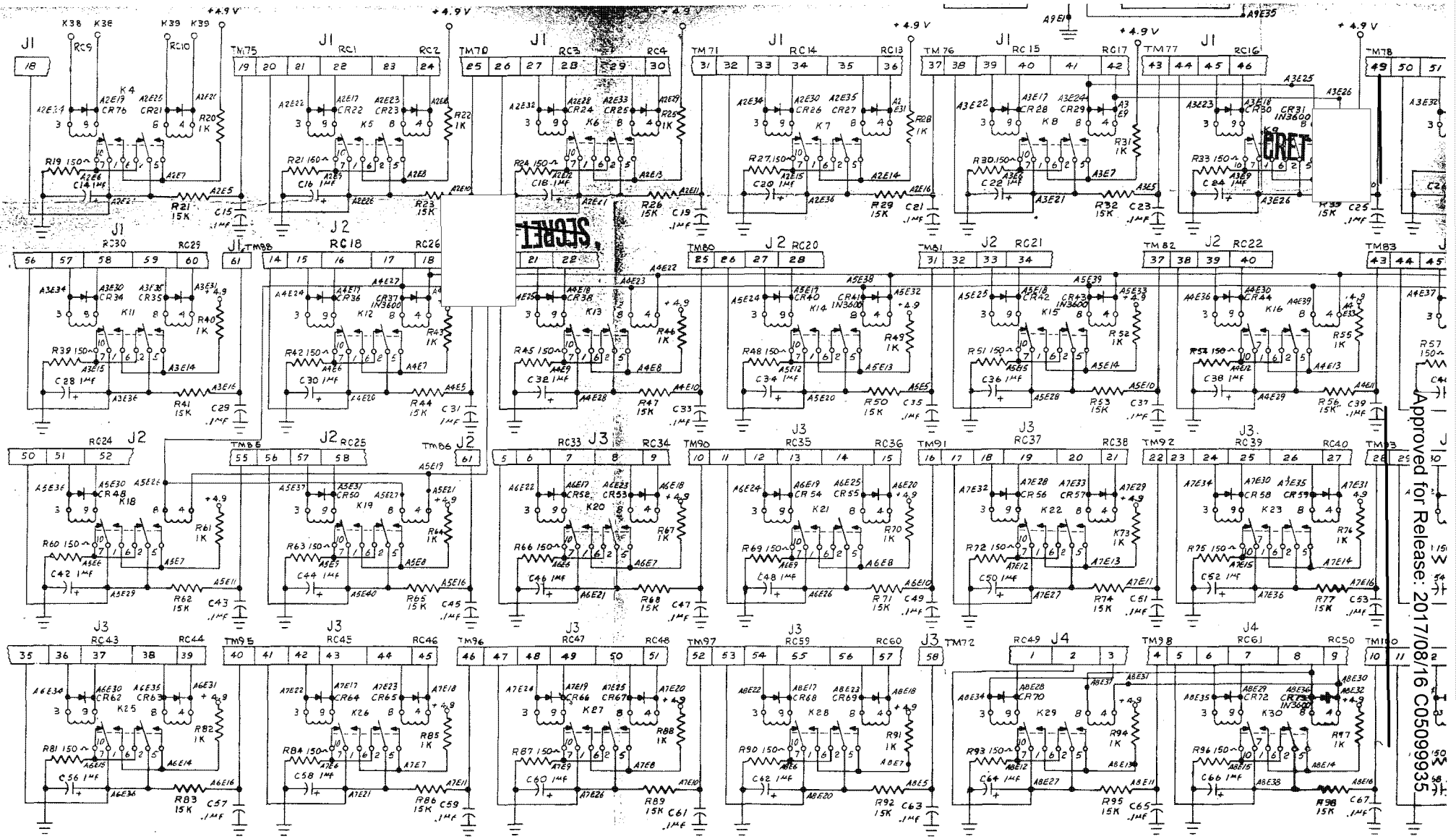

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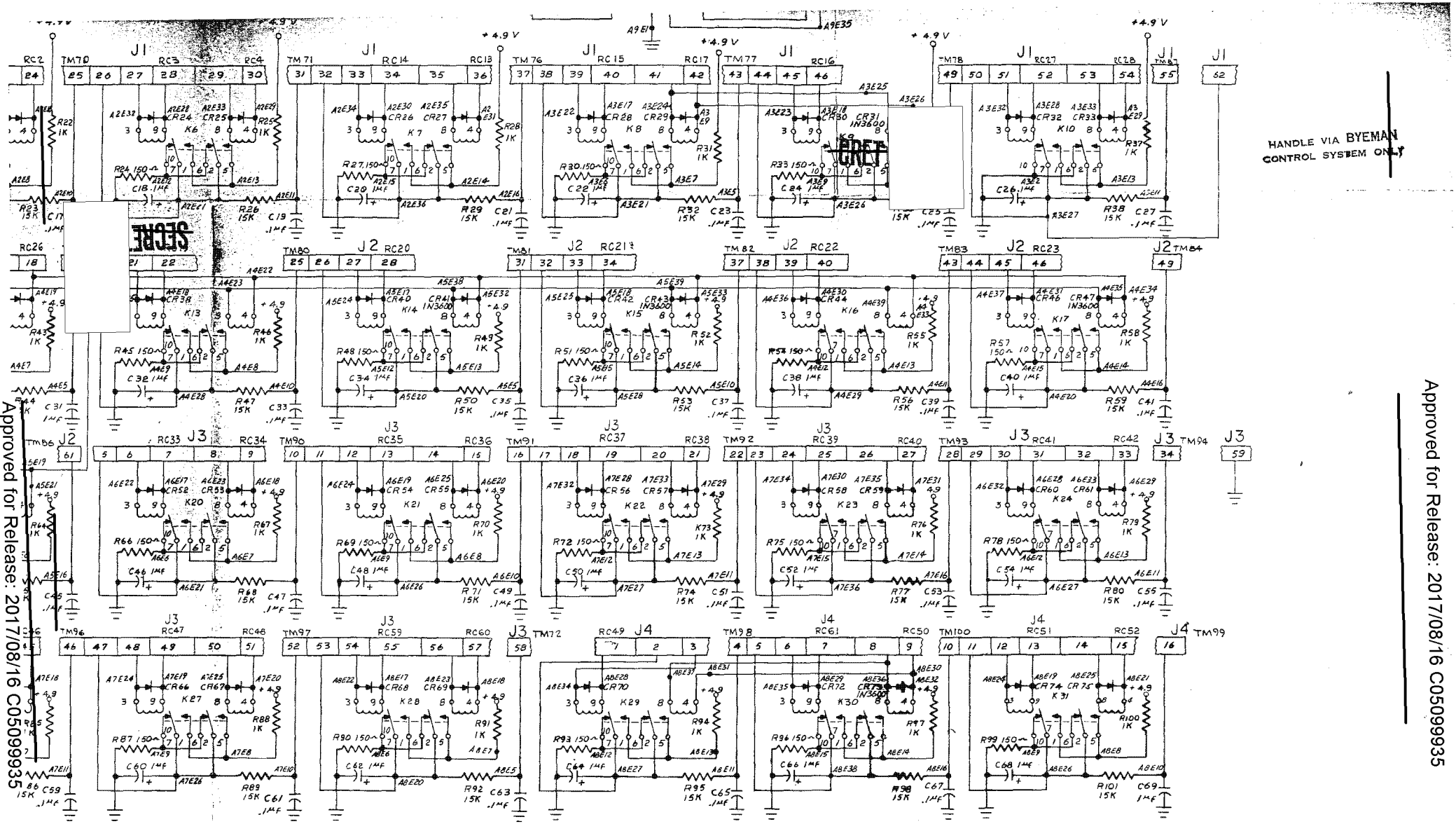

FIGURE 4.6-36. RELAY ASSEMBLY SCHEMATIC DIAGRAM

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~~SPECIAL HANDLING~~

HANDLE VIA BYEMAN CONTROL SYSTEM ONLY

TABLE 4.6-2. SYSTEM COMMANDS

COMMAND NO.	RELAY NO.	COMMAND NAME
RC1	K5-R*	Increase Dwell Time
RC2	K5-S	Decrease Dwell Time
RC3	K6-R	Partial Frequency Scan A On
RC4	K6-S	Partial Frequency Scan A Off
RC5	K36-R	Threshold Control A
RC6	K36-S	Threshold Control $\overline{A}$
RC7	K37-R	Threshold Control B
RC8	K37-S	Threshold Control $\overline{B}$
RC9	K38-S	Recognizer Enable
RC10	K39-R	Recognizer Disable
RC11	K32 & K33-S	Payload On
RC12	K32 & K33-R	Payload Off
RC13	K7-S	Readin On
RC14	K7-R	Readin Off
RC15	K8-R	Disable Upper Frequency Band
RC16	K9-R	Disable Lower Frequency Band
RC17	K8 & K9-S	Enable Upper & Lower Freq. Band
RC18	K12-R	Disable Memories
RC19	K13-R	Disable FOV Inhibit
RC20	K14-R	Disable Tmin Confirm
RC21	K15-R	Disable Tmax Inhibit
RC22	K16-R	Disable A/R Inhibit
RC23	K17-R	Disable Real/Image Confirm
RC24	K18-R	Disable PW Confirm
RC25	K19-R	Disable Frequency Confirm
RC26	K12 - K19-S	Reset R18 through R25
RC27	K10-R	Disable CW - SI
RC28	K10-S	Enable CW - SI
RC29	K11-S	Disable Recognizer Buffer
RC30	K11-R	Enable Recognizer Buffer
RC31	K3-S	Enable RF Calibrator
RC32	K3-R	Disable RF Calibrator
RC33	K20-R	Enable Set A
RC34	K20-S	Disable Set A
RC35	K21-R	Enable Set B
RC36	K21-S	Disable Set B
RC37	K22-R	Enable Set C
RC38	K22-S	Disable Set C
RC39	K23-R	Enable Set D
RC40	K23-S	Disable Set D

* R = Reset Coil (Left coil on schematic 4124-66001)
S = Set Coil (Right coil on schematic 4124-66001)

TABLE 4.6-2. SYSTEM COMMANDS

COMMAND NO.	RELAY NO.	COMMAND NAME
RC41	K24-R	Enable Set E
RC42	K24-S	Disable Set E
RC43	K25-R	Enable Set F
RC44	K25-S	Disable Set F
RC45	K26-R	Enable Set G
RC46	K26-S	Disable Set G
RC47	K27-R	Enable Set H
RC48	K27-S	Disable Set H
RC49	K29-R	Enable Recognizer Input Mode
RC50	K29 & K30-S	Disable Recognizer/Partial Scan Input Mode
RC51	K31-R	Enable Recognizer/Partial Scan Readout
RC52	K31-S	Disable Recognizer/Partial Scan Readout
RC53	K34-S	Recognizer Threshold Bit A
RC54	K35-S	Recognizer Threshold Bit B
RC55		Spare
RC56		Spare
RC57		Spare
RC58	K2-S	Time Reset
RC59	K28-R	Partial Scan B On
RC60	K28-S	Partial Scan B Off
RC61	K30-R	Enable Partial Scan Input Mode
RC62	K34-R	Recognizer Threshold Bit $\overline{A}$
RC63	K35-R	Recognizer Threshold Bit $\overline{B}$

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the two coils was last energized. These relays will operate reliably over a temperature range of -30°C to +85°C with a pulse amplitude of +22 volts minimum and a pulse width of 125 milliseconds minimum.

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4.6.19 Telemetry (T/M) Assembly

The TM Assembly receives 122 input signals and conditions these signals for conversion to telemetry data. All T.M. circuits are listed and described in Table 4.6-3. This table gives the name of the TM point, the location from which the T.M. signal originated, whether the signal is discrete or analog, whether the signal is resolved through use of a 4-bit or 8-bit encoder, the signal category and the type of circuit used to condition the signal.

The "conditioning" process consists of transforming these signals to a voltage level between zero and +5.12 volts. Those signals which are analog* are designed to operate into 2 megohms minimum and 200 picofarads maximum load. Those signals which are discrete** must operate into a load of 500 k ohms minimum and 2000 picofarads maximum.

The 122 input signals are divided into the following classifications:

Category No.	Type	Qty
1	Negative Voltages	8
2	Positive Voltages Equal to or greater than +5.12 Volts	19
3	Positive Voltages less than +5.12 volts.	5

*Analog - Signals which are continuously variable over a given range

**Discrete - Signals which may attain only two voltage levels. These levels for T.M. circuits are -0.4 to +0.9 V.D.C. and +3.1 to +5.9 V.D.C.

TABLE 4.6-3. TELEMETRY POINTS

T.M. POINT NO.	DESCRIPTION	LOCATION	DISCRETE ANALOG	RESOLUTION	CATEGORY	TYPE OF CIRCUIT
1	Main Power Voltage	P/S	A	4	3	F.E.T.
2	Main Current	T.M.	A	4	3	F.E.T.
3	Aux. Voltage	P/S	A	4	3	F.E.T.
4	Aux Current	T.M.	A	4	3	F.E.T.
5	P/L On	T.M.	D	4	2	F.E.T.
6	L.O. Power Monitor (Low Band)	T.M.	A	4	3	Op. Amp.
7	L.O. Power Monitor (High Band)	T.M.	A	4	3	Op. Amp.
8	Osc Control Current (Low Band)	T.M.	A	4	1	Op. Amp.
9	Osc Control Current (High Band)	T.M.	A	4	1	Op. Amp.
10	D/A Output (Low Band)	D/A	A	4	3	-
11	D/A Output (High Band)	D/A	A	4	3	-
12	System Osc	T.M.	D	-	3	Op. Amp.
13	System Clock	D.H.	D	-	↑	Fil.
14	Time Encoder Bit 1	↑	D	-	↑	↑
15	2	↑	D	-	↑	↑
16	3	↑	D	-	↑	↑
17	4	↑	D	-	↑	↑
18	5	↑	D	-	↑	↑
19	6	↑	D	-	↑	↑
20	7	↑	D	-	↑	↑
21	8	↑	D	-	↑	↑
22	9	↑	D	-	↑	↑
23	10	↑	D	-	↑	↑
24	11	↑	D	-	↑	↑
25	12	↑	D	-	↑	↑
26	13	↑	D	-	↑	↑
27	14	↑	D	-	↑	↑
28	15	↑	D	-	↑	↑
29	16	↑	D	-	↑	↑
30	17	↑	D	-	↑	↑
31	18	↑	D	-	↑	↑
32	19	↑	D	-	↑	↑
33	20	↑	D	-	↑	↑
34	21	↑	D	-	↑	↑
35	22	↓	D	-	↑	Fil.
36	23	D.H.	D	-	↓	-
37	Low Band Supply Voltage A	T.M.	D	-	2	DIV
38	High Band Preamp Supply Voltage B	T.M.	D	-	2	DIV
39	Recognizer Inputs	T.M.	D	-	6	Fil.

TABLE 4.6-3. TELEMETRY POINTS (CONT'D)

T.M. POINT NO.	DESCRIPTION	LOCATION	DISCRETE ANALOG	RESOLUTION	CATEGORY	TYPE OF CIRCUIT
40	Sample A/D	T.M.	D	-	6	Fil.
41	IF Disable	↑	D	-	6	↑
42	CW Logic		D	-	6	
43	Preamp SW Low Band		D	-	6	
44	Preamp SW High Band		D	-	6	
45	Frequency Outputs		D	-	6	
46	Frequency Outputs		D	-	6	
47	Frequency Outputs		D	-	6	
48	Frequency Outputs		D	-	6	
49	Frequency Outputs		D	-	6	
50	Frequency Outputs		D	-	6	
51	Frequency Outputs		D	-	6	
52	Frequency Outputs		D	-	6	
53	Frequency Outputs		D	-	6	
54	Frequency Outputs		D	-	6	
55	SI Gated		D	-	6	
56	SI Ungated		D	-	6	
57	Marker Word Output		D	-	5	
58	Data Outputs		D	-	5	
59	Enable Output		D	-	3	
60	Clock Output	↓	D	-	5	Fil.
61	DSU Requested	T.M.	D	-	2	F.E.T.
62	DSU Available	Rel.	D	-	3	-
63	DSU Actuate	Rel.	D	-	3	-
64	Recognizer Readout	T.M.	D	-	6	Fil.
65	SGLS Clock	T.M.	D	-	6	Fil.
66	SGLS Enable	T.M.	D	-	6	Fil.
67	CFC	T.M.	D	-	6	Fil.
68	RF Calibrator #1	T.M.	D	-	6	Fil.
69	RF Calibrator #2	T.M.	D	-	6	Fil.
70	Dwell Time	Rel.	D	-	3	-
71	Requency Scan A	Rel.	D	-	3	-
72	Frequency Scan B	Rel.	D	-	3	-
73	Threshold Control #1	↑	D	-	↑	-
74	Threshold Control #2		D	-		-
75	Recognizer Enabled		D	-		-
76	Read-in On		D	-		-
77	Upper Band Enabled		D	-		-
78	Lower Band Enabled		D	-		-
79	Memories Enabled		D	-		-
80	F.O.V. Inhibit		D	-		-
81	Tmin Confirm Enable		D	-		-
82	Tmax Inhibit Enable		D	-		-
83	A/R Inhibit Enable	↓	D	-	↓	-
84	Real/Image Confirm Enable	Rel.	D	-	3	-

TABLE 4.6-3. TELEMETRY POINTS (CONT'D)

T.M. POINT NO.	DESCRIPTION	LOCATION	DISCRETE ANALOG	RESOLUTION	CATEGORY	TYPE OF CIRCUIT
85	PW Confirm Enable	Rel.	D	-	3	-
86	Freq. Confirm Enable		D	-		-
87	CW SI Circuits Enabled		D	-		-
88	Pre D. Circuits Enabled		D	-		-
89	RF Calibrator Enabled		D	-		-
90	Set A Disable		D	-		-
91	Set B Disable		D	-		-
92	Set C Disable		D	-		-
93	Set D Disable		D	-		-
94	Set E Disable		D	-		-
95	Set F Disable		D	-		-
96	Set G Disable		D	-		-
97	Set H Disable		D	-		-
98	Recognizer Input Mode		D	-		-
99	Rec/Part Scan Readout Mode		D	-		-
100	Partial Scan Input Mode		D	-		-
101	Recognizer Threshold Bit A		D	-		-
102	Recognizer Threshold Bit B	Rel.	D	-	3	-
103	L.O. Regulator	T.M.	A	4	2	DIV.
104	Main Power Supply +28 V		A	4	2	Zener
105	Main Power Supply +8 V		A	4	2	DIV.
106	Main Power Supply +6 V		A	4	2	DIV.
107	Main Power Supply +4.9 (DH)		A	4	3	DIV.
108	Main Power +15 V		A	4	2	Zener
109	Main Power +12 V		A	4	2	Zener
110	Main Power +10.5 V		A	4	2	Zener
111	Main Power +15 V F		A	4	3	F.E.T.
112	Main Power -8 V		A	4	1	Op. Amp.
113	Main Power -6 V		A	4	1	Op. Amp.
114	Main Power -4.9 V		A	4	1	Op. Amp.
115	Main Power -10.5 V		A	4	1	Op. Amp.
116	Main Power +4.9 V (Rec)		A	4	3	DIV.
117	Recognizer Power +10 V		D	-	2	DIV.
118	Recognizer Power -10 V		D	-	1	Op. Amp.
119	Recognizer Power +4.9 V		D	-	2	DIV.
120	Recognizer Power -4.9 V		D	-	1	Op. Amp.
121	Recognizer Power +6 V		D	-	2	DIV.
122	SPARE		D			
123	Recognizer Power +12 V		D	-	2	DIV.
124	Recognizer Power +28 V		D	-	2	DIV.
125	Aux. Power +4.9 V		A	4	3	DIV.
126	Temp. Phase Channel #1	T.M.	A	8	3	DIV.

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TABLE 4.6-3. TELEMETRY POINTS (CONT'D)

T.M. POINT NO.	DESCRIPTION	LOCATION	DISCRETE ANALOG	RESOLUTION	CATEGORY	TYPE OF CIRCUIT
127	Temp. Phase Channel #2	T.M.	A	8	3	DIV.
128	Temp. Phase Channel #3			8		
129	Temp. Phase Channel #4			8		
130	Temp. Freq. Confirm			4		
131	Temp. Log IF #1			8		
132	Temp. Log IF #2			4		
133	Temp. A/D Converter			8		
134	Temp. SI			4		
135	Temp. A/R			4		
136	Temp. Real/Image			4		
137	Temp. Recognizer Threshold			4		
138	Temp. Pre-D			4		
139	Temp. Main P/S #1			8		
140	Temp. Main P/S #2			4		
141	Temp. Aux. P/S			4		
142	Temp. Recog. Memory #1			8		
143	Temp. Recog. Memory #2		A	8		
144	Temp. SWI Memory		A	4		
145	Temp. BS Memory		A	8		
146	Temp. Rec. Rack		A	4		
147	Temp. DH Rack #1		A	4		
148	Temp. DH Rack #2		A	4		
149	Temp. D/A Assy.		A	4		
150	Temp. Loc. Osc.		A	8		
151	Temp. Current Driver		A	8		
152	Temp. Oven		A	8		
153	Temp. Stripline Low Band		A	4		
154	Temp. Stripline High Band		A	4		
155	Temp. Support Channel		A	4		
156	Temp. Honeycomb 1		A	4		
157	Temp. Honeycomb 2		A	4		
158	Temp. Honeycomb 3		A	4		
159	Temp. Honeycomb 4		A	4	3	DIV
160	Rec. Input "0" Line	T.M.	D	4	6	Fil.

KEY: F. E. T. - Field Effect Transistor Circuit
Op. Amp. - Operational Amplifier Circuit
Fil. - Decoupling Network
P/S - System Power Supply
T.M. - T. M. Assembly
D/H - Data Handler
D/A - Digital to Analog Converter
DIV - Voltage Divider
Rel. - Relay Assembly
Zener - Zener/Divider Circuit

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SPECIAL HANDLING

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(Continued)

Category No.	Type	Qty.
4	Thermistor Inputs	34
5	Digital Inputs	3
6	Decoupling Circuits	53
	Total	122

The T/M circuits which condition these signals are described in the following paragraphs.

Circuits for conditioning Category #1 signals - negative voltages, regardless of value are reduced to -200 millivolts or less using a voltage divider and then amplified by a Fairchild Operational Amplifier Moded #702A. The amplifier is designed to operate in the inverting configuration so that the output will vary between zero and +5.12 volts for the expected variations in the negative input voltage. See Figures 4.6-37 and 4.6-38. T/M circuits falling into this category are TM 112, TM 113, TM 114, TM 115, TM 118, TM 120, TM 8 and TM 9.

Circuits for Conditioning Category #2 Signals

These signals are subdivided into two categories: Analog signals and Discrete signals. The analog outputs are adjusted for a nominal output of +2.5 volts. This adjustment is normally made by a voltage divider. Examples are Tm 103 TM 105 and TM107. When the input signal is large, a Zener diode is used to increase the output sensitivity. This is

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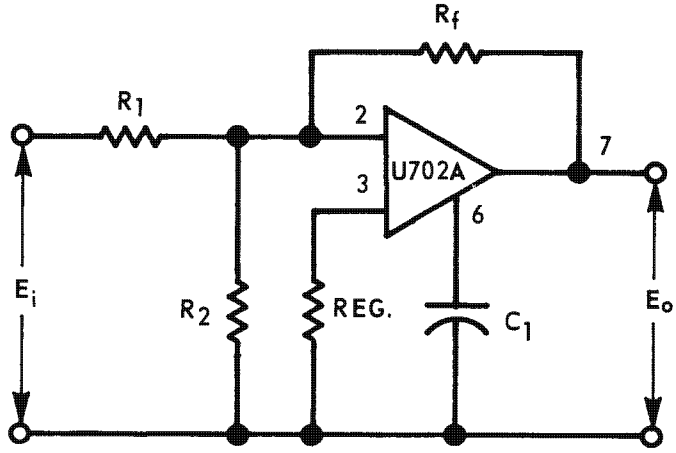

$$\text{GAIN} = \frac{R_f}{R_s} \qquad R_s = \frac{R_1 R_2}{R_1 + R_2}$$

$$\text{REG} = \frac{R_f R_s}{R_f R_s}$$

NOTE: THE VOLTAGE AT TERMINAL 2 MUST NOT EXCEED 200 MILLIVOLTS. OTHERWISE THE AMPLIFIER WILL SATURATE.

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FIGURE 4.6-37 INVERTING OPERATIONAL AMPLIFIER

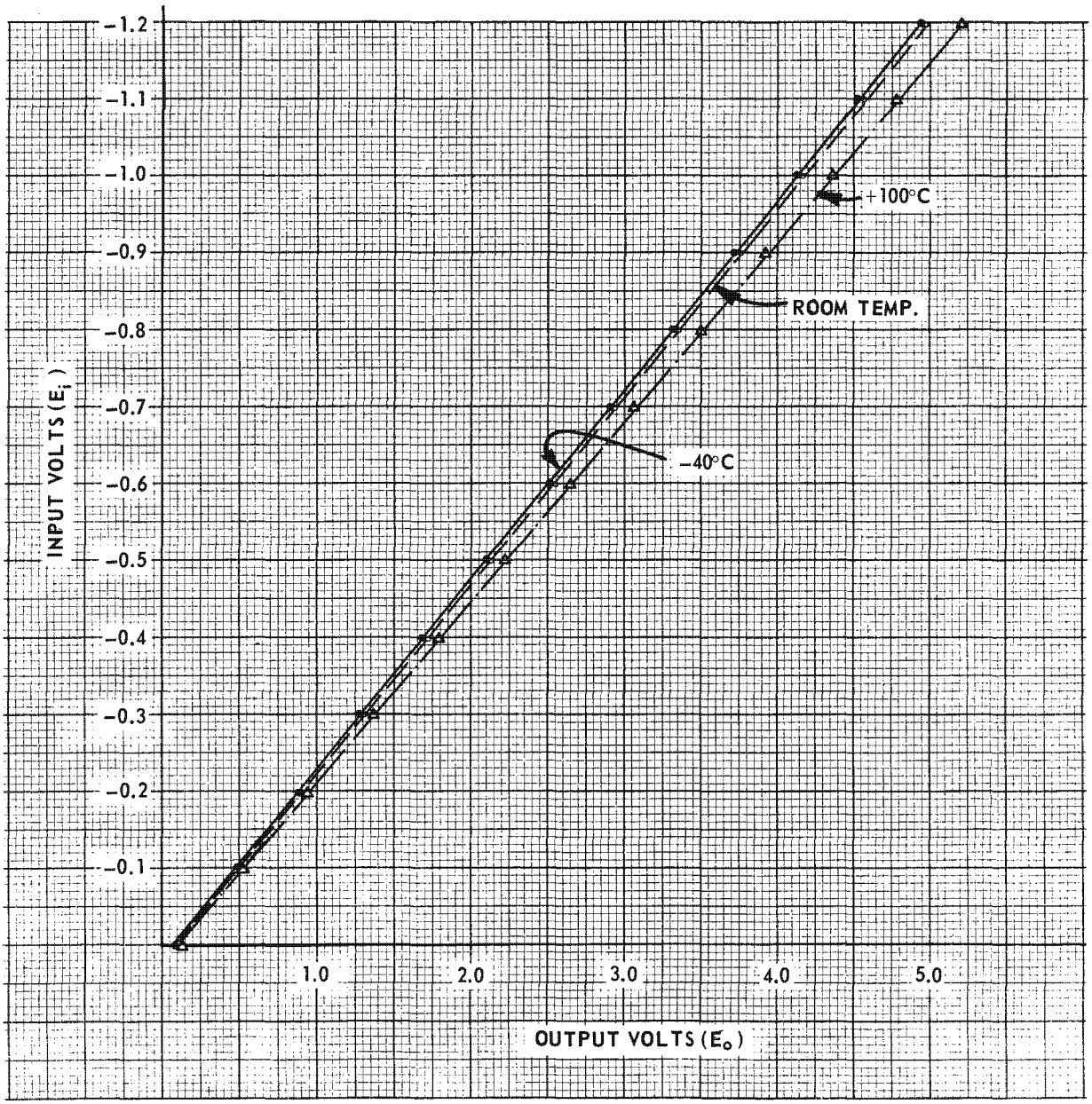

FIGURE 4.6-38 OPERATIONAL AMPLIFIER RESPONSE

done in TM 104, TM 108, TM 109 and TM 110.

Discrete Signals equal to or greater than +5.12 volts are also converted to a voltage range between +4.0 and +5.12 volts by voltage dividers. Included in this category are TM 37, TM 38, TM 117, TM 119, TM 121, TM 123, and TM 124. Where a large amount of isolation is required, a F.E.T. 2N2609 circuit is used. When connected as in Figure 4.6-39, the input impedance is greater than 10 megohms. Figure 4.6-40 shows typical response curves for temperatures of -30°C, +25°C and +85°C. TM 5 and TM 61 utilize this type of circuit.

Positive signals less than +5.12 volts category #3 signals are amplified through the use of Fairchild #702A operational amplifiers. The amplifier is connected in the non-inverting configuration as shown in Figure 4.6-41. The response curves for this circuit for temperatures of -30°C, +25°C and +85°C are shown in Figure 4.6-42. The T.M. points included in this category are TM 6, TM 7 and TM 12. TM 116 and TM 125 also fall in this category.

Some analog Signals require isolation from the input signal. This is accomplished through use of a field effect transistor (Figure 4.6-39). Examples are TM2, TM4,and TM 111.

There are thirty-four temperature monitoring T/M circuits (TM126-TM159) similar to the circuit shown in Figure 4.6-43.

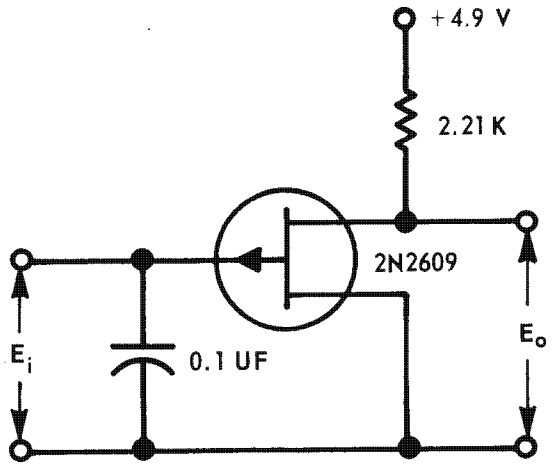

FIGURE 4.6-39 TYPICAL F.E.T. CIRCUIT

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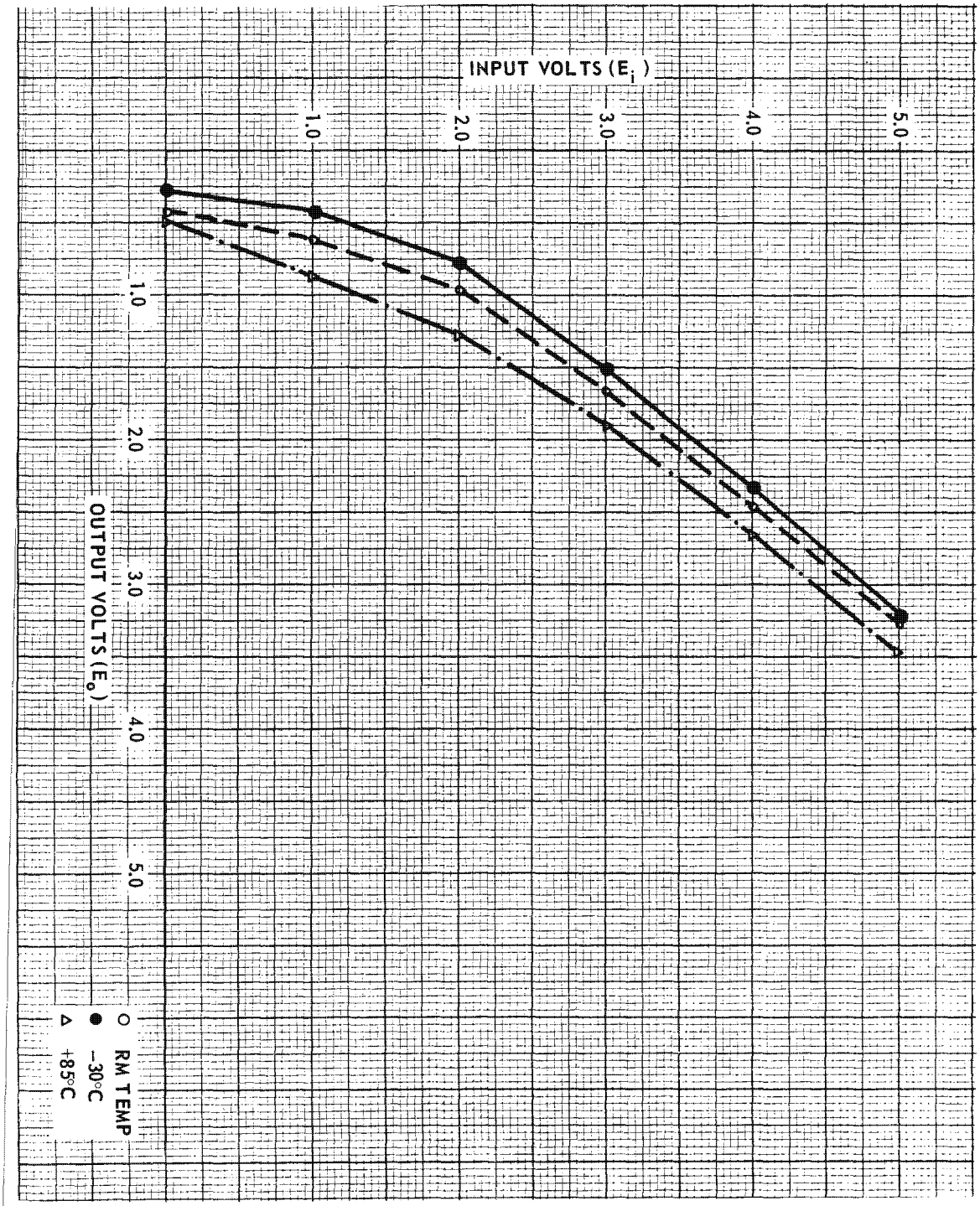

FIGURE 4.6-40 F.E.T. RESPONSE

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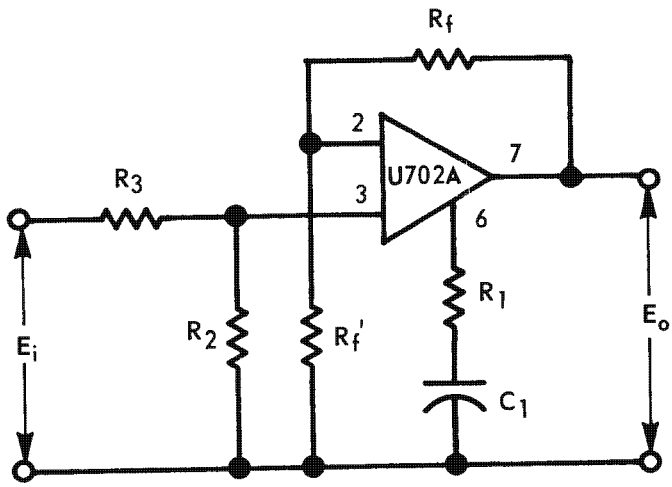

GAIN = $\frac{R_f' + R_f}{R_f'}$

FOR MINIMUM ZERO OFFSET: $RS = \frac{R_f R_f'}{R_f + R_f}$

$RS = \frac{R_2 R_3}{R_2 R_3}$

NOTE: IF THE VOLTAGE AT TERMINAL 3 EXCEEDS 200 MILLIVOLTS, THE AMPLIFIER WILL SATURATE.

FIGURE 4.6-41 NON-INVERTING OPERATIONAL AMPLIFIER

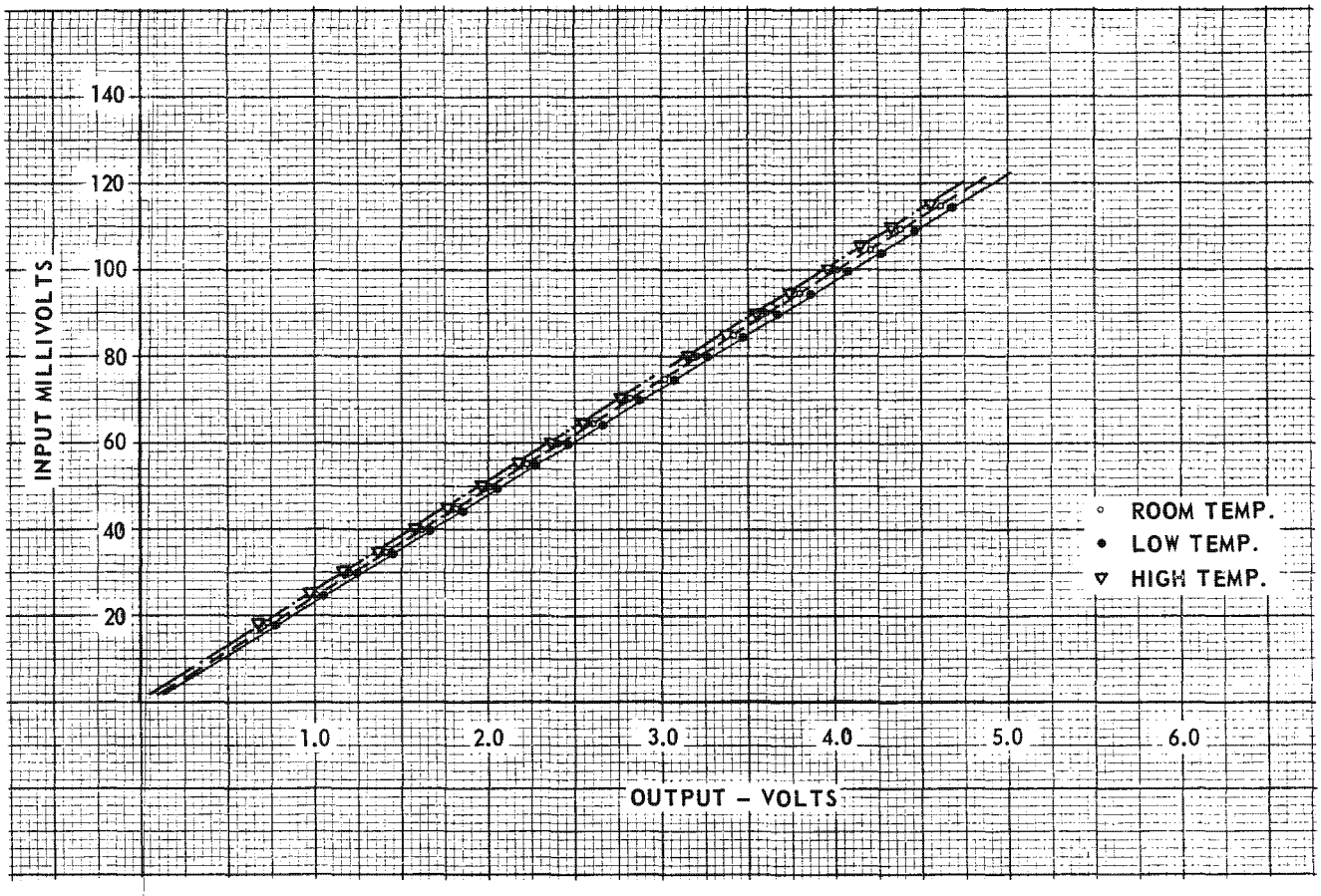

FIGURE 4.6-42 NON-INVERTING RESPONSE

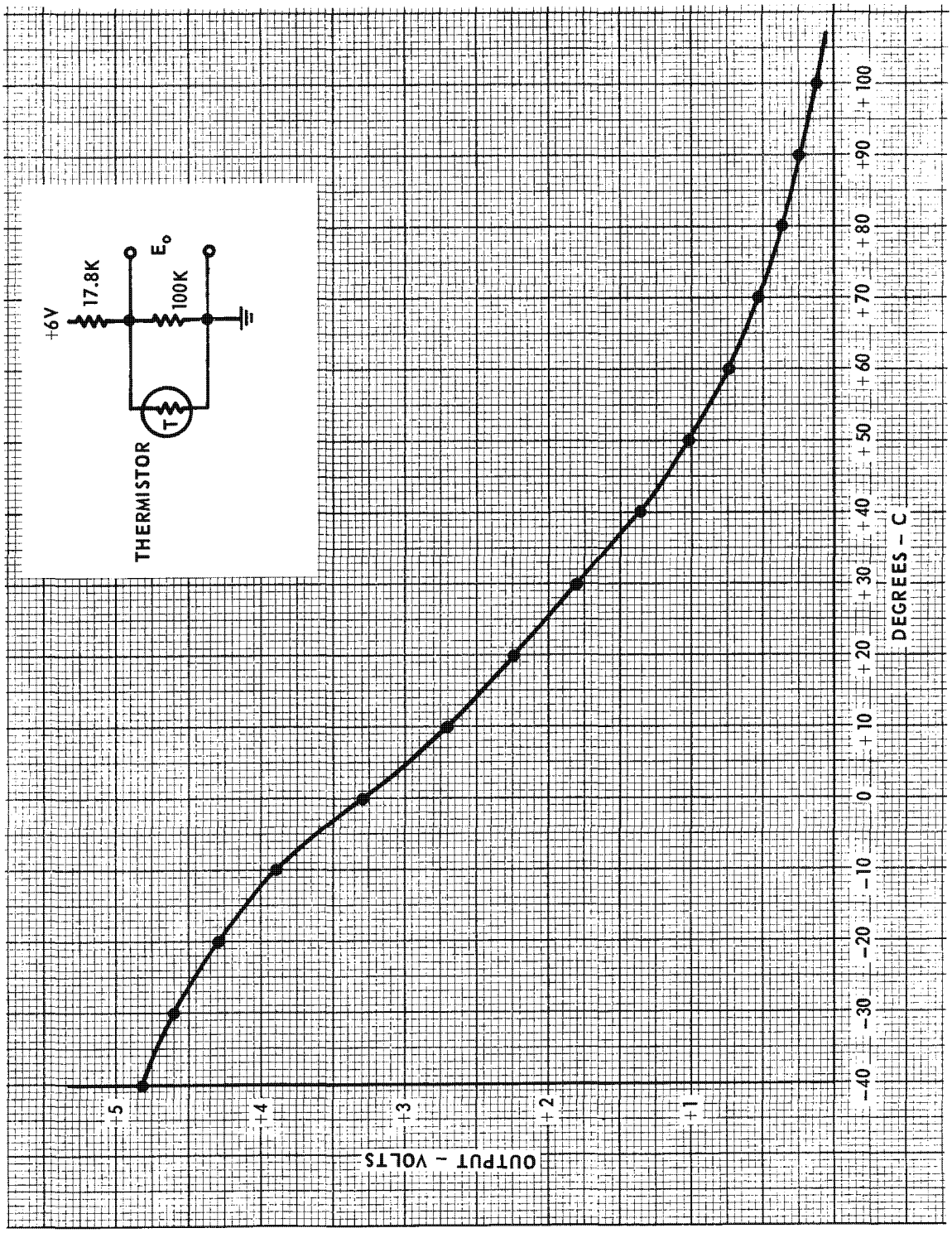

FIGURE 4.6-43 TYPICAL THREMISTOR RESPONSE

A typical response curve of one of these circuits with temperature is included in the same figure.

Greater accuracy is required of thirteen of these circuits because they drive 8-bit rather than 4-bit encoders. In order to attain maximum accuracy, the resistor-thermistor circuit which was initally used to obtain the thermistor response curve, is maintained in the system as a matched group. T/M points which fall in this category are TM 126, TM 127, TM 128, TM 129, TM 131, TM 133, TM 139, TM 142, TM 143, TM 145, TM 150, TM 151, and TM 152.

TM 57 -

The Input to this circuit is a 3-level return-to-zero digital signal from the marker generator register. The first stage consists of a differentiator (Resistor/Capacitor) which develops a positive spike for a "one" and a negative spike for a "zero". The negative spike is clipped by the diode and the base-emitter junction of the transistor. The transistor, connected as an emitter follower, provides a low impedence source to drive the divide-by-five counter.

Since the marker generator register always delivers an even number of "ones" (even parity), the output of the counter will normally rest in a different state after each marker word. This frequently changing counter output indicates that the marker generator is active.

TM 58

The input signal to this T/M circuit is a positive

pulse (16 sec wide minimum) which represents system output data to the C.S.U. The strobe pulse which samples the output signal is 125-usec wide. The divide-by-eight circuit of TM 58 is used to stretch the input signal out to 128-usec minimum, to improve the chances of strobing the signal each sample time. Since it is very unlikely that the data output to the CSU will form a regular pattern (101010....) the width of the output signal will normally be much greater than 128-usec.

TM 60

The circuit receives the clock output to the CSU, a 16 microsecond square wave, and expands it into a 512-usec square wave. This square wave clock occurs only during transmission of data to the CSU.

The TM Assembly also contains R-C filters which are used to filter out high frequency noise and to slow down fast rise time signals which might cause cross-coupling among cabled wires. TM signals conditioned in this manner are TM 13 through 36, 39 through 56, 59, 64 through 69, 101, 102, and 160.

4.7 Recognizer

4.7.1 Introduction

The Recognizer is a separately enabled subassembly which contains the logic circuits necessary to sort out and identify emitters according to selected intervals of frequency, pulse width, and pulse repetition rate. Once a desired signal has been identified the Recognizer requests use of the Data Storage Unit (DSU), initiates a predetermined record mode of operation, and stops the frequency scan at the point of signal identification. At the end of the record period the frequency scanning circuitry is enabled and search for another emitter is commenced.

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4.7.2 Theory of Operation

4.7.2.1 Turn On/Turn Off

The Recognizer must retain the data stored in the memory during the Turn On/Turn Off cycle. The control during these operations is in the Recognizer Programmer and the Data Handler.

The turn on procedure is initiated by the Recognizer turn on command to the Relay Interface Logic from vehicle. The relay logic turns on the logic power (+4.9, -4.9, and +12 volts) to the Recognizer. After a delay of 15 to 35 milliseconds a relay command from the Recognizer is issued to turn on the memory power (+10.5, -10.5, and +6 volts).

The turn off procedure is initiated by the Recognizer turn off command to the Relay Interface Logic. This command turns off the memory power and instructs the Data Handler to turn off logic power. The "turn off" of the logic power will occur from 125 to 250 milliseconds after the memory power has been turned off.

4.7.2.2 Read In/Read Out Mode

Before the Recognizer can successfully identify an emitter for recording on the DSU it must first receive and store the predetermined limits of the emitter parameters for use during the Search mode. The Read In mode is employed to store these parameter limits in the Recognizer core memory.

The Read In mode is initiated by the receipt of a Recognizer Input Mode command from the Relay Assembly. This command causes the memory to be completely erased to prepare it to accept new information. The information to be stored in the memory is then presented to the read-in logic in the form of a serial 448 bit data word at a rate of approximately 1 KHz. This data word consists of eight 56 bit sub-words (Set A through Set H), each of which contains upper and lower limits of frequency, pulse width, and pulse repetition interval. A sub-word format is shown in Figure 4.7-1.

The serial data word is shifted into a 14 bit shift register, while the shift pulses are counted in a separate counter. When the counter indicates that the first 14 bits have been shifted into the register a memory write cycle is generated to store these 14 bits in the first address of the memory. When the counter indicates that the second group of 14-bits has been shifted into the register another write cycle is generated to place these 14 bits in the second memory address. This process is repeated until all 32 of the 14 bit data groups have

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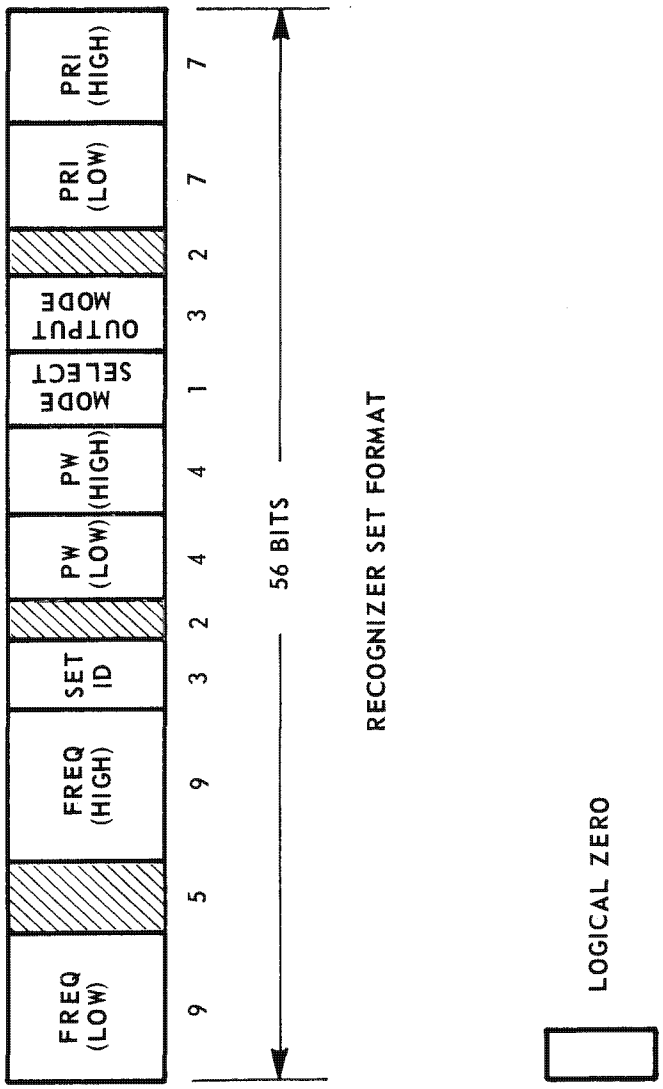

Figure 4.7-1. Subword Format

been stored, thus placing the full 448-bit data word in the memory. The Recognizer Input Mode command is then disabled to complete the Read In mode operation.

The function of the Read Out mode is to provide a non-destructive readout of the memory contents in serial form. In addition, this mode also reads out the contents of the Partial Scan storage register (36 bits). These two data words are combined into a single continuous 484-bit serial data word at the output of the Recognizer.

The Read Out mode is initiated by receipt of 128 KHz shift clock, shift clock enable, and a readout command. When the command is received a memory read/restore cycle is generated to read out the first address (14 bit byte) from the memory and place it in the same shift register used during the Read In mode. The restore operation writes the data back in the same address immediately to make the readout operation non-destructive. Since the 36 bits of Partial Scan limits is to be readout first in time the first 36 shift pulses (128 KHz) are routed to the Partial Scan register in the Data Handler to shift out this data. This data is circulated in the register during readout so that it is not destroyed. When the logic detects that the Partial Scan data readout is complete the next shift pulse is directed to the 14 bit Recognizer shift register to begin shifting out the 14 bit byte previously unloaded from the memory. When the shifting of this byte is complete another read/restore cycle is generated to place the second address data in the register. This data is then shifted out by the next 14 shift pulses. This process is continued until

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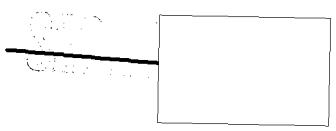
all 448 bits have been unloaded from the memory and shifted out. The readout command may then be disabled to complete the Read Out mode of operation.

4.7.2.3 Search Mode Operation

Operation of the Recognizer in the search mode is initiated by the receipt of a Read In (RI) command. Once this command has been issued the Programmer (see block diagram in Figure 2.1-1)waits for a Change Frequency Command (CFC) signal from the Data Handler. When a CFC is received the Programmer generates the necessary signals to the Input/Output Control logic and Addressing logic to read out the lower and upper frequency limits of Set A from the memory frequency code of the local oscillator (LO) counter in the Data Handler is gated to the Comparison logic and compared with the frequency limits of Set A. If the comparison shows the LO frequency to be greater than the lower limit and less than (or equal to) the upper limit the Decision logic stores this result by generating a "favorable comparison" pulse which stores the identification code (Set ID) of Set A in the Addressing logic. This comparison operation is repeated for Set B through Set H, each time storing the Set ID of those sets



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producing favorable comparisons of frequency. The number of favorable comparisons stored during this phase of the search mode is limited to four in order to reduce processing time and logic complexity. Therefore, all favorable comparison of frequency limits greater than four are ignored by the system. The above frequency comparison cycle is performed each time a CFC is received and is completed within the LO settling time. In the event no favorable frequency comparisons are obtained on a given LO frequency step the Programmer resets all logic and waits for the next CFC. For one or more favorable frequency comparisons the Programmer sets the logic for processing the Ungated SI signal.

The Inhibit Logic, Threshold Buffer and Pulse Width Encoder are enabled for the next Ungated SI pulse as soon as the Data Handler is ready to process an Ungated SI. If an Ungated SI pulse occurs its pulse width is measured by the Pulse Width Encoder, the amplitude threshold code is stored in the Threshold Buffer, and the confirm signals from the IF assembly and Data Handler are stored in the Inhibit Logic. If all confirms are present the Programmer issues the necessary signals to the Addressing Logic to readout the upper and lower pulse width limits from the memory of the first set which produced a favorable comparison during frequency limit comparison. The encoded pulse width from from the Pulse Width Encoder is then is then compared with these limits and if a favorable comparison

is obtained the Programmer then examines the Mode Select bit for the set (which was read out of the memory with the pulse width limits). If the Mode Select bit is a logical zero (single pulse mode) the Record Mode of operation is enabled and the Programmer instructs the Addressing Logic to readout the Output Mode code for the set under consideration from the memory. This code is used by the Record Mode Control logic to determine the length of recording time for the pre-detected signal. A pulse is then generated to request use of the Data Storage Unit (DSU). If the DSU is available a signal is issued by the Record Mode Control logic to block the CFC to the LO counter. If the DSU is not available and the Output Mode code is either 001, 010, 011 the Programmer will reset all logic and wait for the next CFC. However, if the DSU is not available and the Output Mode code is 100, 101, or 110 a "Block CFC" signal is issued and the system begins a sixty second wait period. If during this interval the DSU becomes available the system immediately records for the proper period as determined by the Output Mode Code. If the DSU does not become available during the wait period the Programmer resets the system at the expiration of the wait period and waits for the next CFC. If a favorable comparison of pulse width is not obtained for the first set readout of the memory, the other sets which matched on frequency comparison (if any exist) are then read out and compared in the same manner until either a pulse width match is obtained or all sets

have been compared unsuccessfully. If no matches are obtained the Programmer resets the logic and waits for another CFC.

If, during the pulse width comparison mode described above the Mode Select bit is found to be a logical one (intercept mode) it is then necessary to examine the pulse-repetition interval of the Ungated SI pulse before the Record Mode may be entered. The pulse-repetition-interval (PRI) code for the emitter being received is computed in the Data Handler. When this information becomes available to the Recognizer the Programmer instructs the memory to readout the PRI limits of the set under consideration. A comparison of the received PRI and the stored limits is then made by the Comparison logic. If a favorable comparison is obtained the Record Mode is enabled and operation proceeds as described above for the single pulse mode. If a favorable comparison of PRI is not obtained for the first set of PRI limits readout of the memory the other sets which matched on pulse width comparison (if any exist) are then readout and compared in the same manner until either a PRI match is obtained or all sets have been compared unsuccessfully. If no matches are obtained the Programmer resets the logic and waits for another CFC.

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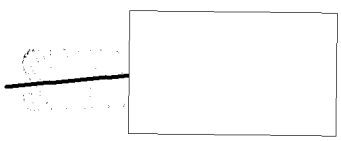
4.7.3.1 Input/Output Control Logic

The input/output control logic provides the proper pulses and levels required to perform the Read In and Read Out modes described in 4.7.2.2. This logic consists of assemblies A10B (4124-63202), A11A (4124-63211), and A11B (4124-63212) in the Recognizer and A21A (4124-64249) in the data handler.

The Recognizer is commanded to read the 448 bit data word into the memory by a change of level on A11A, pin 37 to a ZERO. This triggers the single-shot circuit comprised of M4 and M5 and produces a 2 usec pulse at pin 41 which erases the memory to prepare it to receive the new data word. The 448 bit serial data word is presented to the Recognizer on two separate lines; one line for pulses representing logical ones and another for pulses representing logical zeroes.

After passing through level converting interface circuits in the data handler these two signals are applied to pins 40 and 28 of A21A in the data handler. Here they are combined in a logical OR gate to produce the required shift pulses for insertion of the data into the shift register. Card A21A also contains two counters, a module 14(M1-M5), and a module 32 (M6-M10) which is driven by the module 14. During the Read In mode the module 14 counter counts the shift regis-



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ter clock pulses and generates a signal on pin 74 to indicate when 14 bits of data have been inserted in the register. The Modulo 32 counter counts the number of outputs from the module 14 counter to determine when the full 448 bits of data have been stored in the memory. When a negative transition appears on pin 76 the read in operation is complete.

Card A21A is also used to control the loading of the Partial Scan frequency limits into the Partial Scan shift register. The 36 bit serial word representing the Partial Scan limits appear on the same two lines used for the memory data when a "Partial Scan Input Mode" command is received on pin 16. When the data appears on pins 40 and 28 the 36 shift pulses produced are routed to the Partial Scan register via pin 10. These pulses are also counted as in the memory load operation and a signal generated on pin 72 indicates when 36 shift pulses have been forwarded to the Partial Scan register. This signal sets flip-flop M15 to provide a "block" level to M20, preventing any noise which may occur on the data lines after the 36 valid bits are completed from causing extra shift pulses. This block level is also produced at the completion of the memory load operation by a signal at pin 78.

The input data lines are connected to the input of a 14 bit shift register on pins 69 and 67 of A11A in the Recognizer. The shift pulses derived from the two data signals are applied to A11A, pin 75. When the signal on A21A,

pin 74 (Data Handler) shows that the first 14 data bits have been shifted into the register an 0.5 usec pulse is generated on A10B, pin 66. This pulse triggers the four stage shift register counter (M14, 15, 21, 22) used to produce the read/wirte pulses for the memory. During the memory load operation a master WRITE and INHIBIT pulse is generated at pins 44 and 42, respectively, each time the generator is triggered. During a memory readout cycle the master READ pulse appears on pin 12 in addition to the above signals. The WRITE and READ pulses are 1 usec duration while the INHIBIT pulses are 2 usec. The master INHIBIT pulse is applied to A11B, pin 14 which connects it to 14 separate gates used to control whether a ONE or ZERO is written into each of the 14 cores at a given address. The other inputs to these gates are the 14 stages of the input/output shift register. If a given blocked and no INHIBIT pulse will be sent to the memory Z-axis driver for that plane, thus allowing a ONE to be written in that core. If A ZERO is stored in the register stage the INHIBIT pulse is allowed to pass through the gate and to cause a ZERO to be written in the core.

A memory readout is commanded by a ONE level on A10B, pin 34. The 128 kHz readout shift pulses are applied to A10B, pin 8 and the readout enable signal to A10B, pin 64. If the readout command occurs while the enable signal is present no action is taken until it terminates. An RS flip-flop (M4) is then set which enables gate M3 and allows the 128 kHz pulses

to pass through to pin 58. These pulses are applied to A21A, pin 4 (Data Handler) and then to the Partial Scan register via A21A, pin 10 to shift out the Partial Scan data. These pulses are counted in the counter on A21A and when 36 shift pulses have been detected flip-flop M10 on A10B is set to a ONE by a negative transition on A10B, pin 16. This signals the completion of the Partial Scan readout and the beginning of the memory readout.

When flip-flop M10 on A10B is set the shift pulses on A10B, pin 58 are allowed to pass through M19 to pin 36. The first fourteen pulses which occur shift out the first 14 bit byte which was unloaded from the memory upon receipt of the readout command. These pulses are counted, and when an indication of 14 pulses is received at A10B, pin 6 a second read/restore cycle is generated at pins 12, 44 and 42 of A10B. Those cores which contained ONES produce a ground true pulse (via their sense amplifiers) at pins 5, 15, 19, 33, 47, 51, and 65 of A11A and pins 6, 20, 24, 38, 54, 58, and 68 of A11B. These pulses their respective flip-flops in the shift register to a ONE. Those planes containing a ZERO generate no pulse from their sense amplifiers, thus leaving the corresponding register stages in a ZERO state. Thus, the 14 bit byte stored at the second address is now stored in the register. This action occurs between the 14th and 15th shift pulse gated to the register so that the 15th pulse immediately begins shifting out the second

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byte of data. This process is repeated for all 32 bytes stored in the memory, each byte being read out of the memory each time the counter indicate the previous byte has been shifted out of the register. The register output, A10B, pin 32, is combined in gate M11 on A10B with the output of the Partial Scan register (A10B, pin 22) to provide a single line data output on A10B, pin 18. This signal is passed through a level converting interface circuit on A5 (4124-63217) and made available on a coaxial connector (A42J11).

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4.7.3.2 Addressing Logic

The purpose of the addressing logic is to control the location in the core memory where specific portions of the 448 bit data word are to be stored. This logic circuitry is located on assemblies A9A (4124-63215), A9B (4124-63216) and A10A (4124-63201).

Addressing of the 32 memory locations during both the Read In and Read Out modes is controlled by a five stage ripple counter located on A10A (M1, 2, 3, 6, 7, 8). This counter may be modified logically to step through only 16 states by control signals at pins 19 and 11 of A10A. This allows the counter to be used during the Search mode to sequentially determine the 16 memory addresses containing the upper and lower frequency limits of the eight parameter sets.

Before Read In mode of operation is commanded the counter is set to the all ONE state by a 31.25 kHz clock applied to A10A, pin 73. When the read in cycle begins, a "change address" signal is generated at A10A, pin 21 approximately 0.5 usec before each memory write operation is performed. The first such signal advances the address counter to the all ZERO state, which is decoded by the logic gates located on A10A

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to provide the address information. For each state of the counter four output gates are enabled, one each for an X-axis driver and switch and Y-axis driver and switch. The master WRITE pulse is applied to A10A, pin 63 and passes through the four selected output gates to drive the memory current driver circuits. The counter continues to advance just prior to the occurrence of each subsequent master WRITE pulse until the memory load operation is complete. The counter is employed in exactly the same manner for the memory readout operation.

During the search mode, since all eight sets of frequency limits are readout of the memory for each Change Frequency Command received, the addressing of each sixteen locations is sequential and may be determined by use of the same address counter. During the frequency comparison operation A10A, pin 19 is set to a ONE and A10A, pin 11 to a ZERO. This causes the counter to function as a 16 state device whose states define the 16 frequency limit locations in the memory. The "change address" pulses used to advance the counter in this mode are generated by the Programmer.

The addressing of the 16 locations containing the limits of pulse width and pulse repetition interval (PRI) are not addressed in a sequential manner. For example, during pulse width comparison only those pulse width limits of sets which provided a favorable frequency comparison are read out of the memory. Similarly, only those sets having favorable

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pulse width comparison have their PRI limits readout for comparison with the input PRI code. This technique is used to reduce the time required to process a given SI signal. The addressing of these memory locations is accomplished by using the 3-bit set identification (Set ID) code associated with each of the 8 sets to determine the pulse width and PRI addresses.

During the frequency comparison mode, each time a favorable comparison is obtained a pulse is generated in the Programmer and applied to A9A, pin 16. This pulse samples the 3 bit Set ID code located in the Storage Buffer and loads it into 3 RS flip-flops located on A9A. The trailing edge of the pulse advances a two stage counter (M4, 5) on A9B to enable a second set of 3 gates. Any subsequent favorable comparisons cause the set ID of the associated set to be stored in a second group of RS flip-flops, up to a maximum of 4 codes. When the pulse width comparison mode is entered these stored codes cause those pulse width locations to be selected which correspond to the sets which gave favorable frequency results. This is accomplished by applying the "change address" pulse generated in the Programmer to A9B, pin 4 where it transfers each 3 bit code from its buffer to the output of a common 3 bit buffer. The outputs of this buffer (pins 17, 47, and 69 of A9A) are applied to A10A where the determine the proper address. Comparison of pulse width limits then proceeds, with the outputs of the common buffer stored in another group of flip-flops each

time a favorable pulse width comparison is obtained. These stored codes then provide the PRI addresses to be interrogated during the PRI comparison mode.

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4.7.3.3 Storage Buffer and Comparison Logic

The storage buffer consists of 14 RS flip-flops which are employed as a temporary storage for data read out of the memory. The comparison logic compares the binary number in the storage buffer (parameter limits) with the binary number representing the actual frequency, pulse width, or PRI to determine if the actual parameter lies within the stored limits. This circuitry is located on assemblies A8A (4124-63213) and A8B (4124-63214).

When a memory address is read out, those planes containing a one will produce a positive true pulse on pins 7, 9, 39, 55, 61, 67 and 73 of A8A and pins 38, 44, 50, 56, 64 70 and 76 of A8B. These pulses are each gated with the master READ pulse (A8B, pin 4) to set a ONE into their respective RS flip-flops. The stored number is then ready for use by the comparison logic.

The comparison logic is implemented by using a subtractor circuit in which only the "borrow" output is utilized. The subtractor consists of 14 stages in cascade, each performing the following Boolean expression:

$$B_n = \overline{X}_n B_{n-1} + Y_n \overline{X}_n + Y_n B_{n-1}$$

where B_n = borrow output of the nth stage

X_n = nth digit of minuend

Y_n = nth digit of subtrahend

B_{n-1} = borrow output of the (n-1)th stage

The number "X" is the parameter limit stored in the storage buffer, while the number "Y" is the actual frequency, pulse width, or PRI being compared with stored limits. If a logical level occurs of the output of the most significant stage this signifies that the subtrahend (Y) is greater than minuend (X). If logic 0 results then the subtrahend is less than or equal to the minuend.

Since the different parameter limits are represented by different numbers of bits, the comparison logic must be segmented when comparing pulse width and PRI. This is accomplished using logic levels from the programmer which indicate which parameters are being compared at a given time. These levels section the logic into two 4-bit comparators for pulse width and two 7 bit comparators for PRI comparison. Three outputs are provided on pins 34 and 60 of A8B and pin 77 of A8A. These outputs are sampled by the decision logic 2 usec after each master READ pulse to determine if a "favorable comparison" has been achieved.

4.7.3.4 Parameter Control

The parameter control uses logic levels from the programmer to gate frequency, pulse width and PRI data to the fourteen inputs of the comparison logic. The logic required occupies most of the A4-B card.

The frequency code is available from the LO counter as logic levels. These nine bits of frequency data need only to be gated to the comparison logic by a logic level (A4-68) that begins at State 1 of the frequency mode (Figure 4.7-2) and ends at State 4 of the pulse width mode, Figure 4.7-3 .

The pulse width data, located in the pulse width encoder, is gated to the comparison logic by a logic level (A4-40) that begins at State 4 of the pulse width mode and ends at State 5 of the PRI mode, Figure 4.7-4 . Since both upper and lower limits are compared simultaneously, each of the four bits of the pulse width data must be gated into two of the comparison logic inputs.

Since the PRI data from the PRI encoder of the data handler is available in pulse form only, it must be stored in rs flip-flops for the comparison logic. These buffers are cleared during State 4 of the frequency mode (A4-58) and set by a ground true pulse 19.5 to 24.0 microseconds after a favorable SI. The data is held in the buffers until the next SI pulse is encoded by the recognizer. Since both upper and lower limits of the PRI are compared simultaneously, each bit of the seven bit

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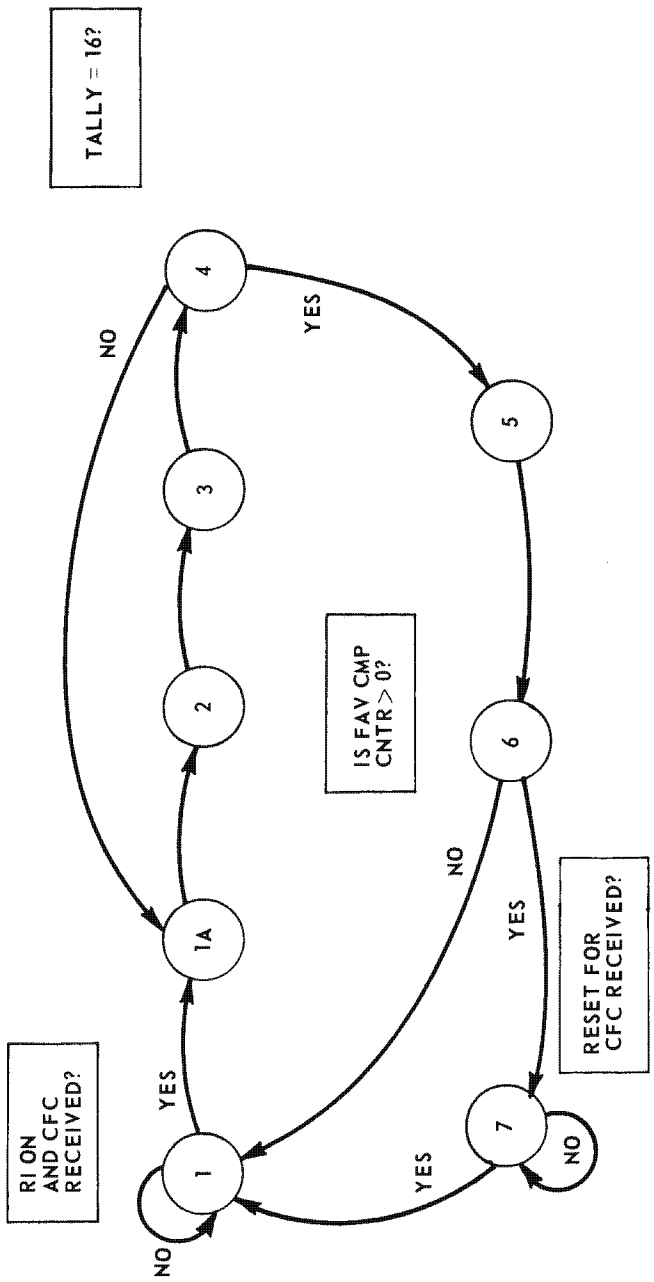

Figure 4.7-2. Frequency Mode State Diagram

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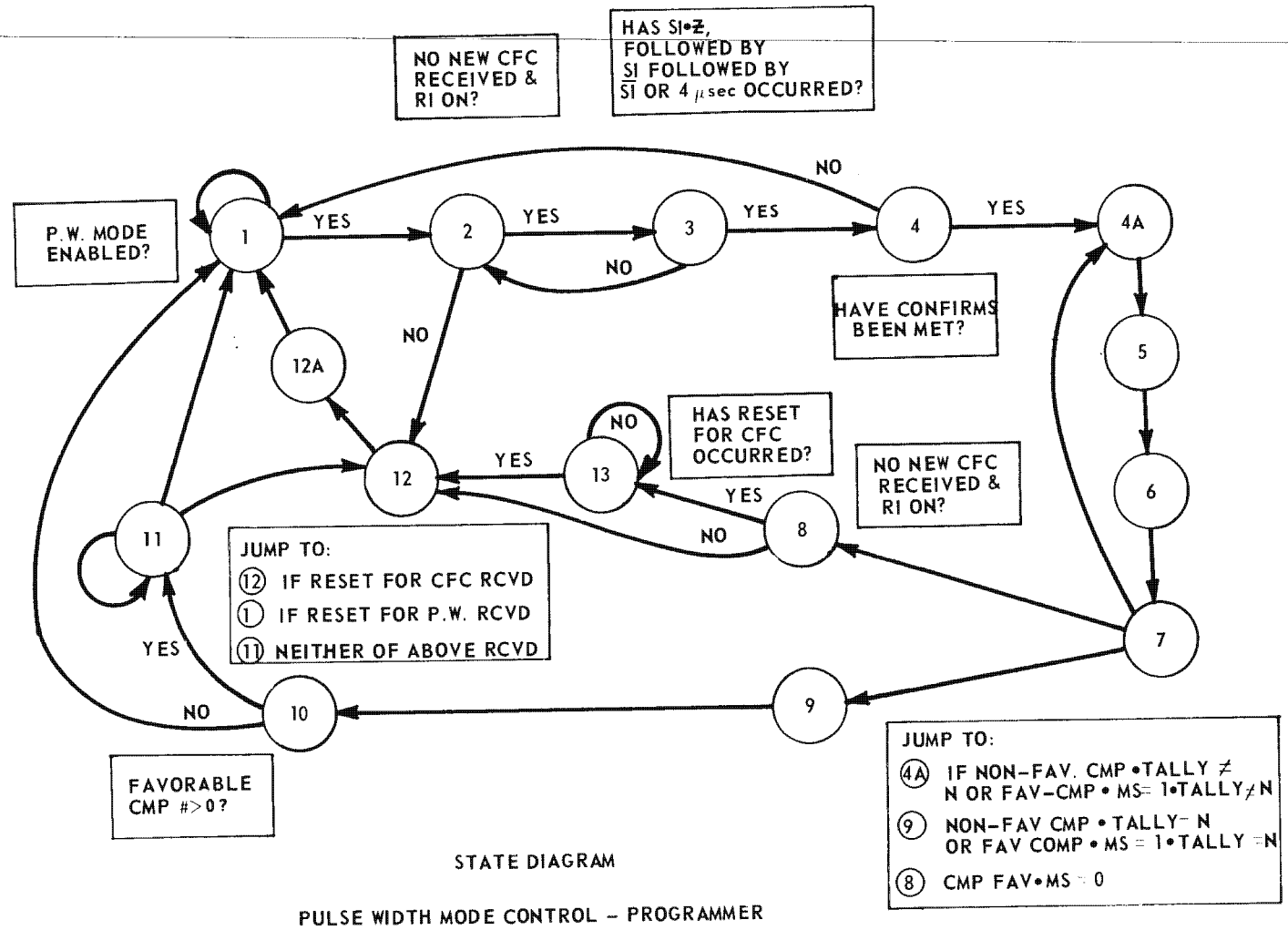

STATE DIAGRAM

PULSE WIDTH MODE CONTROL – PROGRAMMER

Figure 4.7-3. Pulse Width Mode State Diagram

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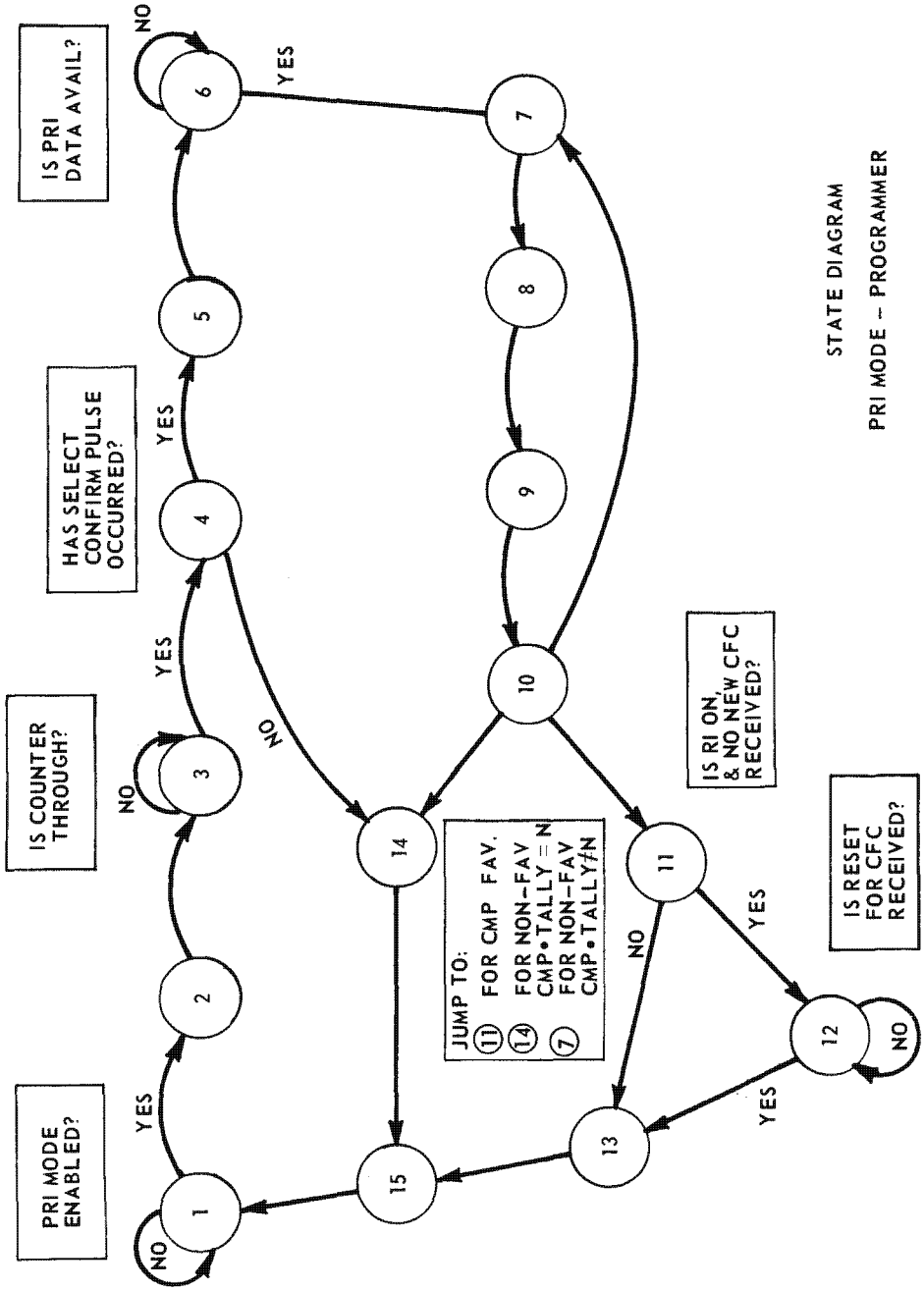

Figure 4.7-4. PRI Mode State Diagram

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PRI is gated into two of the comparison logic inputs by a logic level (A4-46) that begins at State 5 of the PRI mode and ends with a new CFC or State 4 of the pulse width mode.

Table shows the pin numbers of the outputs of the parameter control (to the comparison logic) and the corresponding input pin numbers that will be gated to the comparison logic during each mode. The dashes in the frequency and pulse width columns are gated to the comparison logic as logical zeros. The most significant bit (MSB) is noted in each column.

4.7.3.5 Pulse Width Encoder

The pulse width encoder is used to determine the pulse width of the ungated SI from the SI generator.

The pulse width encoder (located on A4-B) consists of a four bit ripple counter, with a four megahertz clock (A4-78) enabled by the ungated SI (A4-51) and a control signal from the programmer (A4-76). The signal from the programmer enables the encoder when State 2 of the pulse width mode , Figure 4.7-3 , is entered, the data handler is not processing, and no ungated SI pulse is present.

Since a four megahertz clock is used as the input to the counter, as long as the enables and ungated SI are present the counter will step one count every 250 nanoseconds. The maximum pulse width that can be measured is 3.75 microseconds. At this point the counter is full and the input clock is disabled.

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OUTPUTS TO COMPARISON LOGIC	FREQUENCY	PULSE WIDTH	PRI
A4-16 (MSB)	A4-14 (MSB)	Z8-6 (MSB	A4-18 (MSB
A4-22	A4-10	Z7-6	A4-24
A4-28	A4-4	Z6-6	A4-30
A4-38	A4-6	Z5-6	A4-36
A4-48	A4-70	Z8-6 (MSB)	A4-44
A4-50	A4-66	Z7-6	A4-52
A4-62	A4-64	Z6-6	A4-60
A4-20	A4-12	Z5-6	A4-18 (MSB)
A4-26	A4-8	-	A4-24
A4-32	-	-	A4-30
A4-34	-	-	A4-36
A4-42	-	-	A4-44
A4-54	-	-	A4-52
A4-56	-	-	A4-60

TABLE DATA TO COMPARISON LOGIC

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The outputs of the four flip-flops of the encoder (Z5-6, Z5-6, Z7-6 and Z8-6 on A4-b) go to the inputs of the parameter control logic on the same card.

The pulse width information is stored in the flip-flops until the programmer returns to State 1 of the pulse width mode.

4.7.3.6 Inhibit Logic

The inhibit logic stores the confirm signals associated with an SI and issues an inhibit signal to the programmer if all the necessary confirms were not present.

The inhibit logic, located on A1-B and A3-B, consists of four JK flip-flops used to store the real confirm (A4-76), amplitude confirm (A4-74), minimum pulse width confirm (A4-72), and frequency confirm (A4-64) and two RS flip-flops used to store the select confirm (A1-30) and pri available (A3-16).

The real, amplitude, minimum pulse width and frequency confirm flip-flops are enabled when the programmer is in State 2 of the pulse width mode, Figure 4.7-3, the data handler is not processing, and the ungated SI is a logical zero level.

When an ungated SI pulse appears, all confirm pulses that occur before State 4 of the pulse width mode are stored in their respective flip-flop. The inhibit signal (A1-44) will inhibit the processing of the SI unless the real

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confirm, amplitude confirm, minimum interval confirm or the frequency confirm or the frequency confirm disable (A1-48) have been received when the programmer enters State 4 of the pulse width mode.

The select confirm buffer is reset by the same signal that enables the JK flip-flops. The buffer is set if a select confirm pulse occurs before State 4 of the PRI mode and the data handler has not started processing another SI. The output of the buffer (A4-26) is used by the programmer during the PRI mode.

The PRI available pulse occurs 2.5 microseconds after the select confirm pulse and sets the PRI available buffer. The output of the PRI available buffer (Z22-8 on A3-B) is used by the PRI mode control of the programmer.

4.7.3.7 Decision Logic

The decision logic consists of the logic on AZ-B required to determine from the comparison logic outputs if a comparison was within the limits, and logic on A8-A to block the favorable comparison when the set under comparison is disabled.

The decision logic receives levels from the programmer to determine which limits are being compared. The enable for the frequency comparison mode (Pin A2-52) begins in State 1 of the frequency mode, Figure 4.7-2 , and lasts until State 4 of the pulse width mode, Figure 4.7-3 . The enable for the

pulse width mode (Pin A2-48) begins in State 4 of the pulse width mode and lasts until State 5 of the PRI mode, Figure The enable for the PRI mode begins in State 5 of the PRI mode and lasts until State 1 of the frequency mode.

In the frequency mode, a separate comparison is made for the upper and lower limits. For a favorable comparison for a particular set, output A of the comparison logic (A2-50) must be a logical one during the low limit comparison, and a logical zero during the upper limit comparison. An RS flip-flop is used to remember if the lower limit is favorable. The flip-flop is set during State 4 of the frequency mode (A2-42) if output A of the comparison logic is a logical one and Z10-6 on A2 is a logical zero, indicating low limit comparison. A one microsecond favorable comparison pulse is issued during State 4 of the frequency mode if output A of the comparison logic is a zero level and Z10-6 on A2 is a logical one, indicating upper limit comparison.

In the pulse width mode, a one microsecond favorable comparison pulse is issued during State 7 of the pulse width mode (A2-44) if outputs A and B (A2-32) of the comparison logic are a one and zero logic level respectively. In the PRI mode, a one microsecond favorable comparison pulse is issued during State 10 of the PRI mode (A2-46) if outputs A and C (A2-38) of the comparison logic are a one and zero logic level respectively.

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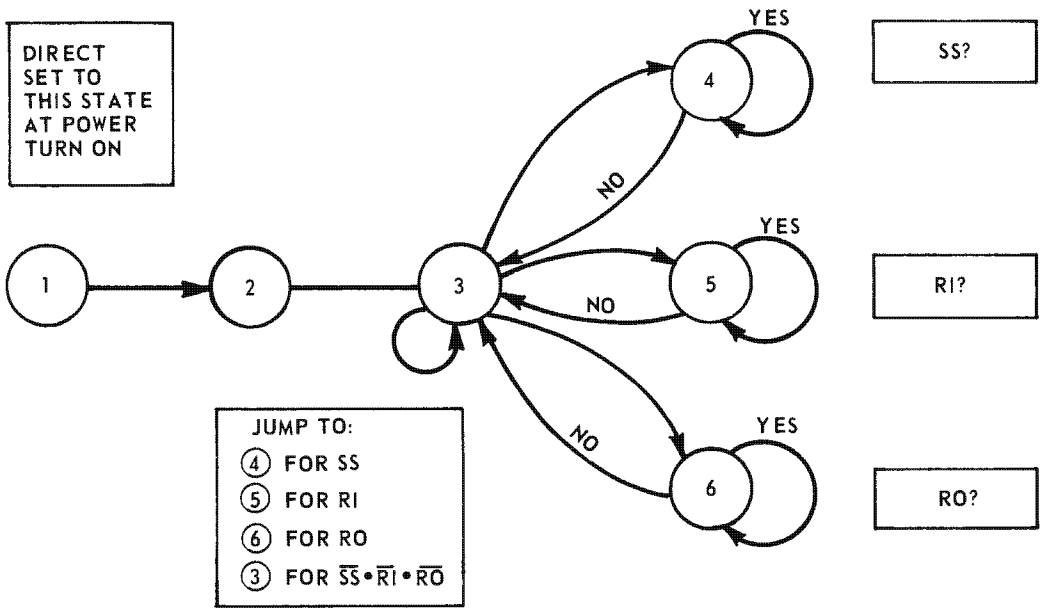
During the comparison of the upper frequency limit the set ID of the set being compared is in the storage buffer (A8-5 MSB, A8-11 and A8-37). Each set is decoded and logically anded with its set disable from the relay interface logic so that if a favorable comparison occurs in a set that is disabled, the favorable comparison pulse to the addressing logic and programmer will be blocked.

4.7.3.8 Programmer

The programmer may be broken down into four sequential networks and comparison counters. The first sequential network, the turn on control, is used during power turn on and to enable the other sequential networks. Each of the other sequential networks is used to control the comparison of a parameter. These networks are referred to as the frequency comparison control, pulse width comparison control, and the PRI comparison control. These networks use a 1MHz clock and may change states once each microsecond. In some cases the sequential network will continue to return to the same state, thus remaining in a given state for any length of time.

The turn on control is a sequential network used to set the programmer logic to its initial state, then turn on the memory power. The remaining function of the turn on control is to sense the RI on and recognizer read in/read out commands. The state diagram for the turn on control is shown in Figure 4.7-5.



STATE DIAGRAM

TURN ON CONTROL–PROGRAMMER

FIGURE 4.7-5. TURN-ON CONTROL STATE DIAGRAM

The programmer is set to its initial state by a circuit consisting of a 39 microfarad capacitor across the input of a nand gate with a charging path from the recognizer power through a 750 ohm resister. A resister to ground is also provided for a discharge path when the power to the recognizer is turned on, a ten millisecond pulse is issued from the nand gate (A1-31) that sets all sequential networks to the initial states.

Once the ten millisecond pulse is removed, the turn on control will enter State 2. The next trailing edge of the 30.5 Hertz clock (A12-32) will issue a 35 millisecond pulse (A1-3) that will turn the memory power relay on.

After one microsecond in State 2, the network will enter State 3 and wait until a command is received from the data handler.

The state that follows State 3 will be State 5 if the RI on command (A1-73) is issued. State 5 (A1063) is used to enable the other sequential networks in the programmer and the record mode control. Once the RI on command goes off, State 3 will be re-entered.

When the read in (SS- Pin A1-77) command is issued, the network will enter State 4. When the read out (RO- Pin A1-71) command is issued, the network will enter State 6. State 3 is re-entered when no command is present.

The comparison counters consist of a five bit "Tally Counter" used to count the number of comparisons made in each of the parameter comparison modes, and two three-bit counters used to count the number of favorable comparisons in the frequency and pulse width modes.

The tally counter is stepped each time State 2 of the frequency mode, Figure 4.7-2 (A2-77), State 5 of the pulse width mode, Figure 4.7-3 (A2-73) or State 8 of the PRI mode, Figure 4.7-4 (A2-75) is entered. Once the counter is full, a "tally = N" level (A2-66) is issued to the sequential networks. Before the frequency data is compared, State 1 of the frequency mode (E6 on A2-B) sets the tally counter such that sixteen pulses are required before the Tally = N level is issued. State 4 of pulse width mode is used to set the tally counter (A2-12) so that it will take the number of steps to the tally counter to issue Tally = N as is stored in the favorable frequency comparison counter. State 5 of the PRI mode is used to set the Tally counter (A2-12) so that it will take the number of steps to the tally counter to issue Tally = N as is stored in the favorable pulse width comparison counter.

The favorable frequency comparison counter is enabled from State 1 of the frequency mode until State 4 of the pulse width mode (A2-52) to count the number of favorable comparisons (A2-30) during the frequency comparison mode. A signal (A2-18) is used to indicate that no favorable comparisons

have been counted. This counter is reset during State 1 of the frequency mode (E6 on A2-B).

The favorable pulse width comparison counter is enabled from State 4 of the pulse width mode until State 5 of the PRI mode (A2-48) to count the number of favorable comparisons (A2-30) during the pulse width comparison mode. A signal (A2-20) is used to indicate that no favorable comparisons have been counted. This counter is reset during State 2 of the pulse width mode (A2-26).

The frequency comparison control of the programmer is a sequential network used to control the frequency comparison and the logic used to issue commands to the addressing and input/output control logic. The state diagram in Figure 4.7-2 is used to describe the sequential operations in the frequency mode.

The frequency comparison control network is set directly to State 1 at power turn on by a pulse (A2-17) from the turn on control, and remains there until an enable signal (A2-71) is received from the turn on control and a CFC (A2-63) is received from the data handler. The CFC sets an RS flip-flop, used to remember if a CFC has occurred.

All memory instructions issued by the programmer to the input/output control logic and addressing logic during comparisons are shown in Figure 4.7-6. The logic necessary to issue these instructions are included in the frequency mode

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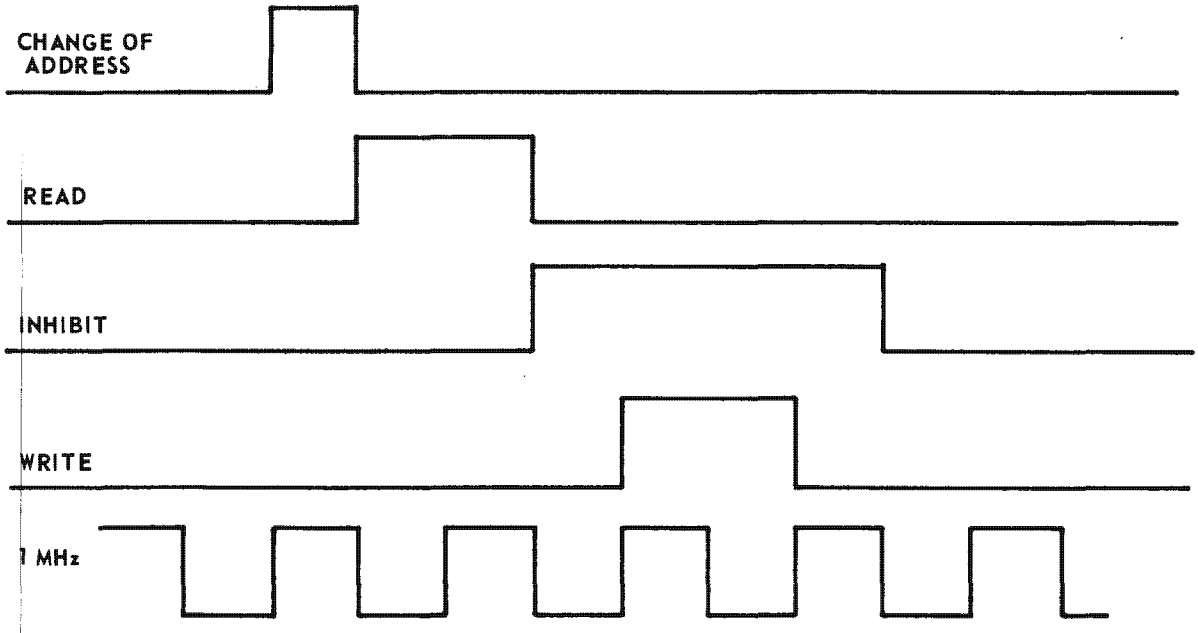

MEMORY INSTRUCTIONS

Figure 4.7-6. Memory Instructions Timing Diagram

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control. The change of address (A2-23) is a .5 microsecond pulse issued during State 1A of the frequency mode, State 4A of the pulse width mode and State 7 of the PRI mode. This pulse is generated by logically anded with the 1MHz clock with the states mentioned above. The read pulse (A2-57) is issued during State 2 of the frequency mode, State 5 of the pulse width mode, State 8 of the PRI mode and State 2 of the record mode. The inhibit pulse (A2-25) is issued by setting an RS flip-flop during State 3 of the frequency mode, State 6 of the pulse width mode, State 9 of the PRI mode and State 4 of the record mode. The RS flip-flop is reset by States 1A or 5 of the frequency mode, States 4A, 8 or 9 of the pulse width mode, States 7, 11 or 14 of the PRI mode and States 6 or 7 of the record mode. The write pulse (A12-41) is generated from the inhibit pulse by enabling a JK flip-flop to toggle on the 1 MHz clock (A12-45).

State 1A follows State 1, and during this microsecond, the change of address is issued and the inhibit flip-flop is reset. During the next microsecond, the State 2, the read pulse will be issued and the tally counter will be stepped one count. State 3 follows State 2, and during this microsecond, the inhibit flip-flop is set. During State 4 the decision logic is strobed (A2-33) allowing the comparison result to be stored.

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From State 4, the sequential network will return to State 1A if the tally=N signal from the tally counter (A2-53) has not been issued. If Tally = N has been issued, State 5 will follow State 4. The inhibit flip-flop is reset during the microsecond in State 5. State 6 follows State 5, and during State 6 the CFC buffer (RS flip-flop) is reset, thus the output of the buffer (A2-65) will remain in the reset state until another CFC occurs.

State 1 will follow State 6 if the favorable frequency comparison counter shows there have been no favorable comparisons (A2-55). If one or more have been recorded, State 7 will be entered. During State 7 the pulse width comparison control is enabled. State 1 will be entered after State 7, after a reset for the next CFC (A2-21) is received.

The Pulse Width Comparison Control consists of a sequential network with the state diagram in Figure and the logic needed to select an SI for a comparison.

The Pulse Width Comparison Control is set to state 1 at power turn on, and remains there until the enable (A3-7) from the Frequency Comparison Control is received. State 2 is entered after the enable is received, and a pulse (A3-3) is sent to the Tally Counter to load the number of comparisons to be made in the pulse width mode. The enable from the Turn On Control (A3-19) and the CFC buffer (A3-21) must indicate that the RI On command is on and no CFC has occurred since the buffer was reset before State 3 will follow State 2. Otherwise, State 12 will follow State 2.

An RS flip-flop is used to determine when the pulse width of the Ungated SI will be encoded and the comparisons made. This flip-flop is held reset while the Pulse Width Comparison Control is in State 1 (A1-7), and is set when no pulse is on the Ungated SI line (A1-19) and the Data Handler is not processing (A1-15). The output of this flip-flop (A1-11) is used to enable the Pulse Width Encoder and Inhibit Logic.

State 2 will follow State 3 until an Ungated SI rises and either falls or the pulse width encoder indicates the maximum pulse width is recorded (3-15); then State 4 will follow State 3. State 4A will follow State 4 if all the necessary confirms were met (A3-11); if not, the

network will return to State 1 .

The memory pulses (shown in Figure 4.7-6) are issued by the Frequency Comparison Control for all the parameter controls. The Change of Address is issued during State 4A , followed by the read pulse in State 5 . The Inhibit flip-flop is set by State 6 and reset by the state following State 7 .

The state following State 7 is State 8 if the comparison was favorable (A3-65) and the Mode Select Bit (A3-13) was a logical zero. State 7 will be followed by State 4A for a non-favorable comparison and Tally N or a favorable comparison, Tally N, and Mode Select Bit is a logical one. State 7 will be followed by State 9 for a non-favorable comparison and Tally =N or a favorable comparison, Tally =N, and Mode Select Bit is a logical one.

State 8 will be followed by State 13 if the enable from the Turn On Control is present and no CFC has been received since the system was reset. If either condition does not exist, State 12 will be entered. State 13 enables the Record Mode Control (A3-57), and remains in State 13 until a reset for CFC is received (A3-29) to send the network to State 12 .

State 9 is followed by State 10 . State 11 follows State 10 if the Favorable Pulse Width Counter indicates one or more favorable comparisons (A3-49). If no

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favorable comparisons were recorded, State 1 is entered.

State 11 enables the PRI Comparison Control (A3-45). The network remains in State 11 until a reset for a new CFC is received causing the network to enter State 12, or a reset for new SI pulse is received (A3-43) causing the network to enter State 1.

State 12 issues a reset to process a new CFC to the Frequency Comparison Control; then State 12A is entered followed by State 1.

The PRI Comparison Control consists of a sequential network with the state diagram shown in Figure 4.7-4. The network is set to State 1 by the Turn On Control (A3-24) at power turn on and remains in State 1 until the enable (A3-64) is received from the Pulse Width Comparison Control.

State 1 is followed by State 2, then State 3. The network will remain in State 3 until a Timer Thru pulse is received from the Timer logic. Once the Timer Thru is received, State 4 is entered. If the Select Confirm buffer is set (A3-72), State 5 will be entered. If the buffer is not set, State 14 is entered.

State 6 follows State 5, and the logic remains in State 6 until the PRI Available buffer is set. Once the PRI Available has occurred, State 7 is entered. The Change of Address pulse (memory pulses shown in Figure 4.7-6) is issued during State 7, followed by the Read pulse issued in

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State 8. State 9 follows State 8, and is used to set the Inhibit flip-flop. State 10 follows State 9.

State 11 is entered after State 10 if a favorable comparison is received (A3-4). If no favorable comparison is received and Tally =N, then State 14 is entered. If no favorable comparison is received and Tally N, State 7 is entered. The state following State 10 resets the Inhibit flip-flop.

The enable from the Turn On Control (A3-22) and the CFC buffer (A3-20) are checked to see that RI On is still on and no CFC has been received since the buffer was reset. If these conditions still exist, State 12 is entered. If they do not exist, State 13 is entered.

State 12 enables the Record Mode Control, and thelogic stays in State 12 until a reset for the next CFC is received. Once the reset is received, State 13 is entered. A reset for another CFC is issued (A3-66) during State 13. State 15 follows State 13.

A reset for a new SI is issued (A3-68) during State 14, and the number of pulse width comparisons is reset into the Tally Counter. State 14 is followed by State 15, then State 1.

Three RS flip-flops are used to indicate the comparison mode of the Programmer. The flip-flop indicating the frequency comparison mode (M_2) is set during State 1 of the

frequency mode (A8-16) and reset by the same signals that set the pulse width comparison mode (M_3) and the PRI comparison mode (M_4). M_3 (A8-20) is set during State 4 of the pulse width mode (A8-26) and State 2 of the record mode (A8-24). M_3 is reset by same signals that set the other two modes. M_4 (A8-32) is set during State 5 of the PRI mode (A8-10) and is reset by same signals used to set the other two modes.

4.7.3.9 Record Mode Control

The Record Mode Control is a sequential network that controls the record time once a match has been obtained. A 1 MHz signal (A4-3) is used as the clock for the network; thus the network remains in each state one microsecond, unless conditions are such that the network should stay in its present state. See Figure 4.7-7.

The Record Mode Control is set to State 1 at power turn on by a pulse from the Turn On Control (A4-5). The network remains in State 1 until a Record Mode Enable is received during State 13 of the pulse width mode (Figure 4.7-3)(A4-71) or State 1 of the PRI mode (Figure 4.7-4) (A4-73).

Once the record mode is enabled, State 2 is entered. During State 2 , the M_2 flip-flop of the Programmer is set (A4-61). State 3 is entered after State 2 , and during State 3 , a 40 millisecond one shot is triggered and a Read pulse issued. Following State 3 , State 4 is entered,

~~SECRET~~
~~SPECIAL HANDLING~~

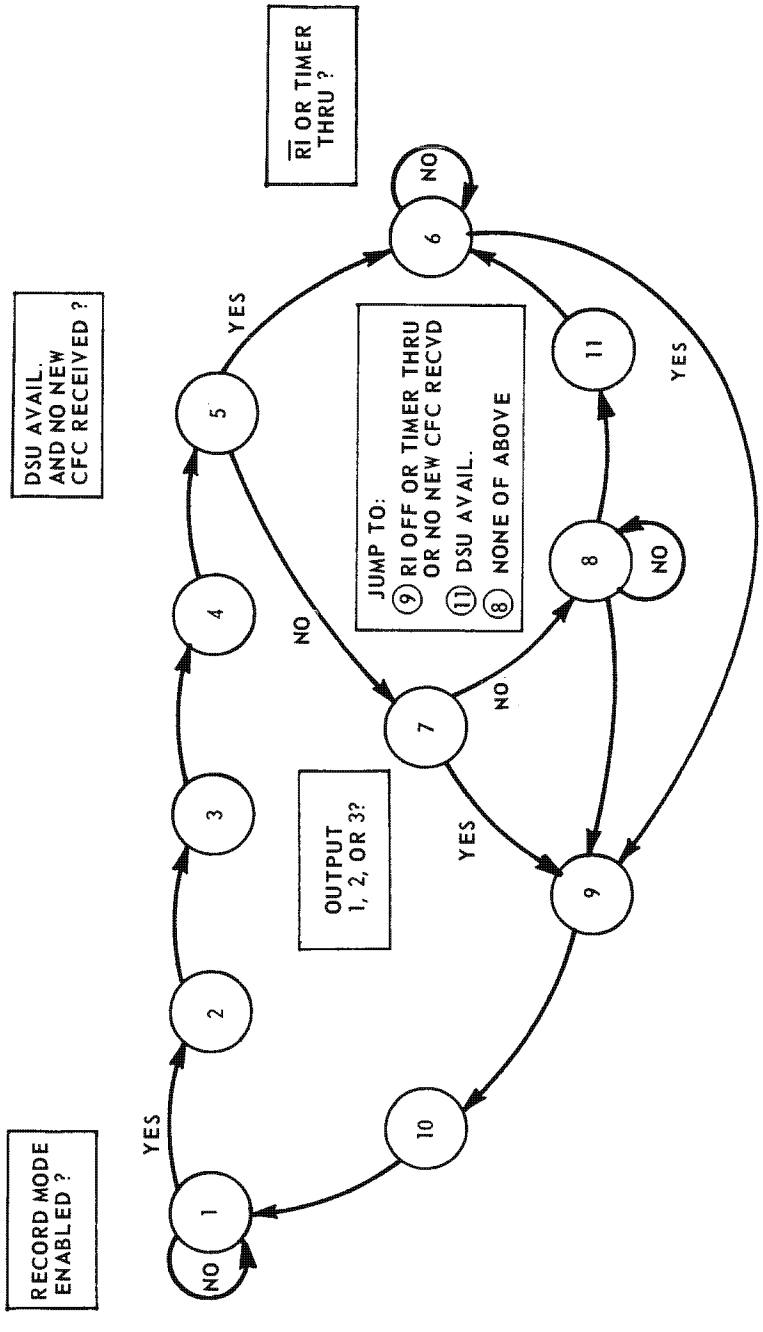

Figure 4.7-7. Record Mode State Diagram

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~~SECRET~~
~~SPECIAL HANDLING~~

and the Inhibit flip-flop is set. State 5 follows State 4 and the Output Mode code (A4-33, A4-35, and A4-37) are stored in RS flip-flops.

State 6 follows State 5 if the DSU is available and the CFC buffer has not been set since the frequency mode. If one of these conditions does not exist, State 7 will follow State 5 .

The 40 millisecond one shot triggered in State 3 is logically ended with State 6 for the DSU Request signal (A4-9). Also in State 6 a Start Timer (A4-11), Record (A4-7), and Block CFC (A12-18) signals are issued. The logic remains in State 6 until a Timer Thru signal is received from the Timer or the enable from the Turn On Control is removed when the RI On command is removed. State 9 is entered when either condition occurs.

If the Output Mode Code is 001, 010, or 011, State 9 will follow State 7 ; however, if the Output Mode Code is 100, 101, or 110, State 8 is entered. During State 8 , a Block CFC and Start Timer are issued. The logic will remain in State 8 until either the DSU becomes available and State 11 is entered or a CFC is received or Timer Thru is received or RI On command is removed, and State 9 is entered. During State 11 a Timer Reset pulse is issued; then State 6 is entered.

During State 9 , a reset for the next CFC (A4-75)

is issued. State 9 is followed by State 10 , then State 1

The Record Mode Control sends the time to be recorded to the Timer during States 6 and 8 . The record time in State 6 is determined by decoding the Output Mode Code as shown in Table 4.7-1 , and providing a pulse to the Timer during State 6 , for the time that was decoded. During State 8 a pulse (A4-) sets the Timer for a 60-second "wait" time.

TABLE 4.7-1. RECORD TIME

Mode Select Code	Time	Location
001	2 Sec.	
010 100	4 Sec.	
011 100	8 Sec.	
110	300 Sec.	

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4.7.3.10 Timer

The Timer is used to measure the period of time during a record operation and determine the interval since an Ungated SI occurred.

The Timer logic consists of a twelve-bit ripple counter and logic required to control the counter. The "Reset Timer" (A1-78) level hold the counter reset except during use. This reset is removed (1) during the period from State 2 of the pulse width mode (Figure 4.7-3) until State 8 of the pulse width mode or State 5 of the PRI mode (Figure 4.7-4) and (2) during all states of the record mode (Figure 4.7-7) except states 1 and 11 . The clock to the Timer (A1-18) is 1 MHz during the first period mentioned above, and 8 Hz during the second.

The timing is initiated by the "Start Timer" pulse (A1-4) that is generated when the Ungated SI pulse width is encoded and during States 6 and 8 of the record mode. Following the Start Timer pulse, a .5 microsecond strobe pulse is generated to set the time in the counter. When the counter reaches the all logical ones state, the input clock is blocked and a "timer Thru" pulse (A1-38) is generated.

4.7.3.11 Threshold Buffer

The Threshold Buffer is used to store the "Amplitude Information" from the Recognizer Threshold section of the IF until a match has been obtained; then the information

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is gated to the Marker Word Register and Control and Predetector (Figure 2.1-1).

The Threshold Buffer consists of three RS flip-flops (Outputs on A2-3, A2-15, and A2-10). The buffer is cleared during State 1 of the pulse width mode (Figure 4.7-3) and enabled by a level from the pulse width mode (A2-9) that occurs after State 1 of the pulse width mode when the Data Handler is not processing and no Ungated SI is present.

The"Amplitude Information" (A2-5, A2-7, and A2-11) pulses that occur before State 1 or 4A of the pulse width mode are stored in the buffer. The outputs of the buffer (Amplitude Thresholds) are available at the Marker Word Register and Control, and if a match is obtained this information is gated to the Predetector as Set Gains (gating to Predetector is located in the Data Handler).

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4.7.3.12 Interface Circuits

The interface circuitry is employed to make the Recognizer logic compatible with equipment external to the Reaper system. These discrete component circuits are located on assembly A5 (4124-63217) in the Recognizer. The following circuits are included:

a) Readout Enable Interface (Figure 4.7-8)
When a readout of the Partial Scan and Recognizer memories is commanded by the Command Programmer an enable signal is applied to A5, pin 77. This signal has a nominal pulse width of 62.5 usec and a peak amplitude between 2.1 and 6.1 volts. The 100 ohm resistor across the input provides a termination of approximately 93 ohms for the input signal. When the input goes to its high voltage level it causes Q6 to saturate, providing a low level at the output (A5, pin 75). When the input returns to its low state the transistor is cut off and the output is +4.9 volts. Thus, this circuit is a level converter between the Command Programmer and the Recognizer.

b) Readout Clock Interface (Figure 4.7-9)
The readout clock used to shift out both the Partial Scan and Recognizer memory data is a

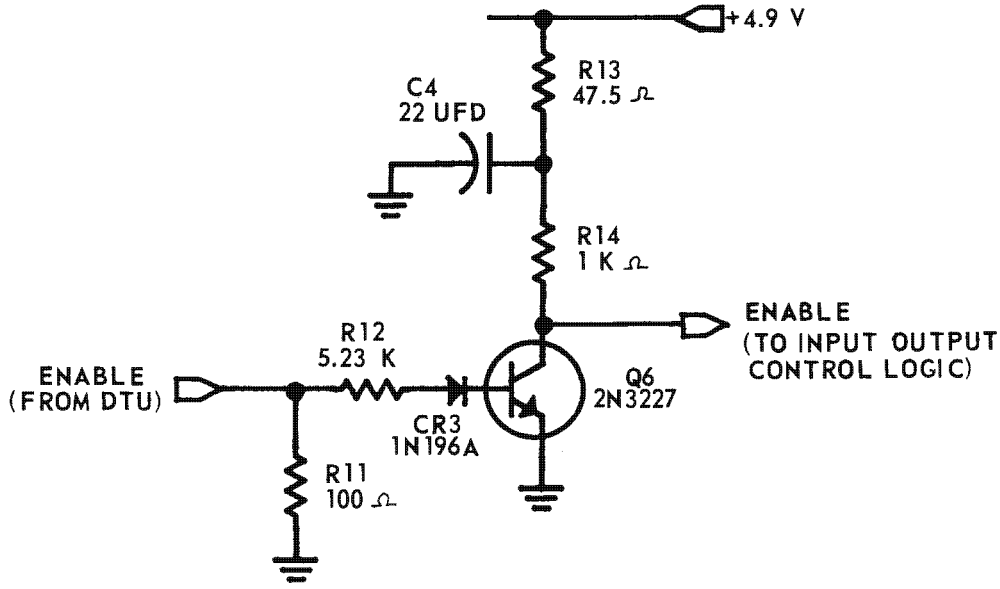

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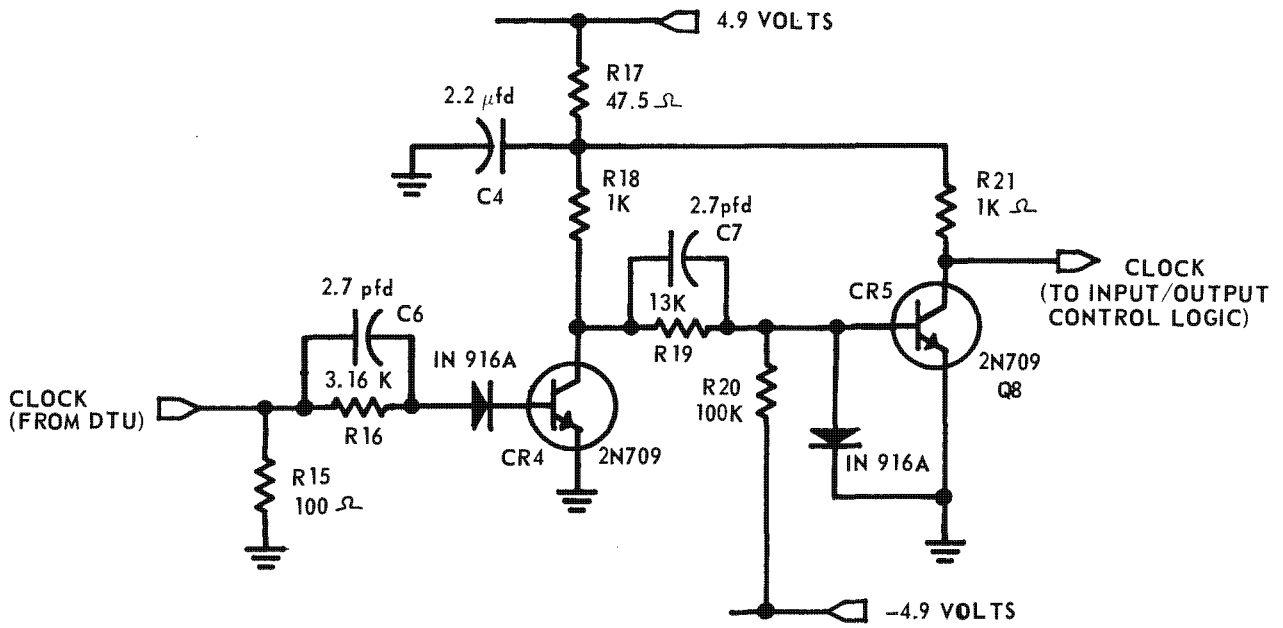
Figure 4.7-8. Interface Enable



INTERFACE
CLOCK

Figure 4.7-9. Interface Clock

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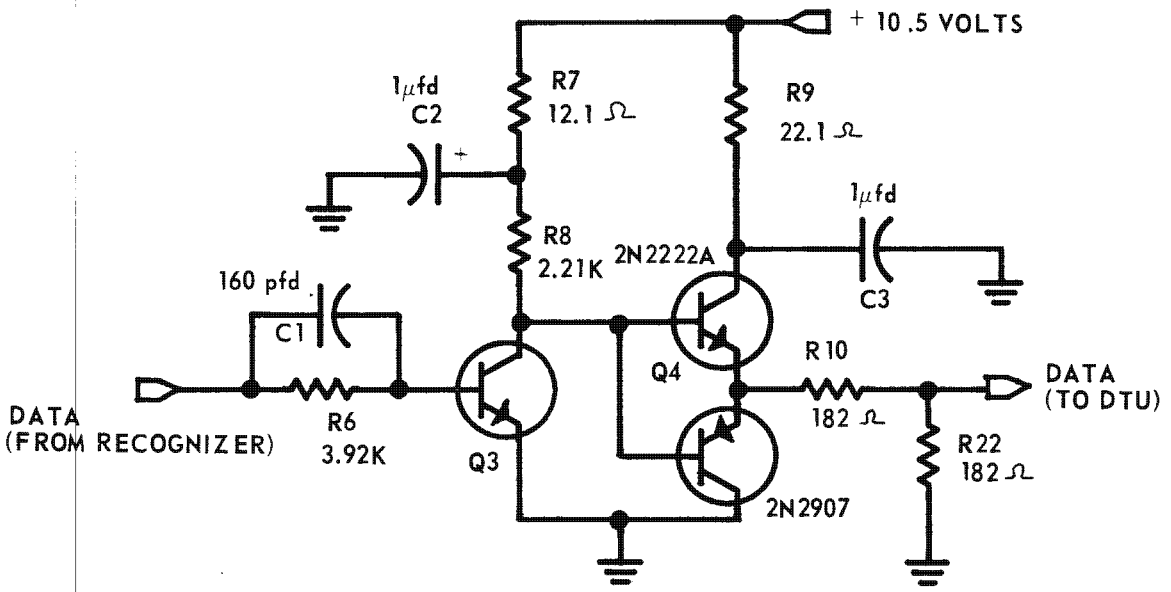

INTERFACE DATA

FIGURE 4.7-10. DATA INTERFACE

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128 kHz pulse train having a nominal pulse width of 1.0 usec and a peak amplitude between 2.1 and 6.1 volts. This signal is generated by the Command Programmer and applied to A5, pin 67. The interface circuit consists of two saturating inverters (Q7, Q8) used to convert the level of the input clock signal to those required by the Recognizer integrated circuits. Resistor R15 provides the required 93 ohm termination for the input signal.

c) Readout Data Interface (Figure 4.6-10)
The serial NRZ waveform representing the Partial Scan and Recognizer memory data is applied to A5, pin 17. This network consists of a saturating inverter (Q3), followed by a double-ended emitter follower (Q4, Q5). The input signal from the Recognizer logic, is inverted and presented at the output (A5, pin 7) as a signal having a peak amplitude between 3.6 and 5.9 volts and a source resistance of 93 ohms.

d) Memory Power Turn-On Relay Driver (Figure 4.7-11)
This circuit is not an interface with equipment external to the Reaper system but is used to sink the drive current necessary to operate

a relay. In operation the input (A5, pin 27) is held in a low voltage state which keeps Q2 cut off. When it is desired to turn on memory power the input goes high, allowing the current through R4 to be applied to the base of Q2, causing it to saturate. The collector of Q2 is connected through the relay coil to +28 volts.

e) DSU Request Relay Driver

This circuit is identical to the relay driver described above. The input signal (A5, pin 51) is a positive pulse from the Record Mode Logic which occurs each time a Recognizer match has been achieved.

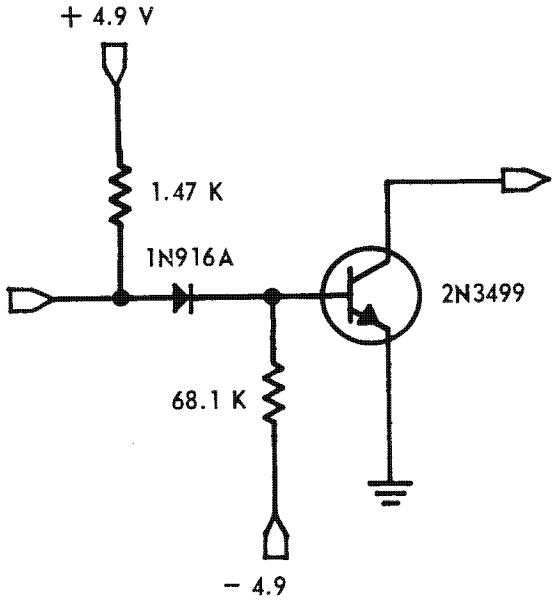

Figure 4.7-11. Relay Driver

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4.8 Power Supply

4.8.1 Introduction

The power supply is a switching-type high-efficiency power supply using integrated circuits in the control circuitry and high speed transistor switches for the power output stage. The extremely fast turn-on and off times of the output devices minimizes switching dissipation which allows high operating frequencies with smaller power transformers, and filters.

The overall power supply block diagram is shown in Figure 4.8-1.

The main power supply provides the following output voltages and their tolerances.

VOLTAGES	TOLERANCE	VOLTAGE	TOLERANCE
15 V Floating	±0.1	-8.0 V	±0.1%
+15 V	0.1	+6.0 V	±0.2%
+12 V	0.1	-6.0 V	±0.2%
+10.5 V	±1.0	5.0 V H.P.	+0.0%-4%
-10.5 V	±1.0		
8.0 V	±0.1	5.0 V	+0.0%-2.0%
+25 V	±0.5	-5.0 V	+2.0%-0.0%

The main power supply provides power for the Data Handler, Recognizer, IF Unit and RF Unit.

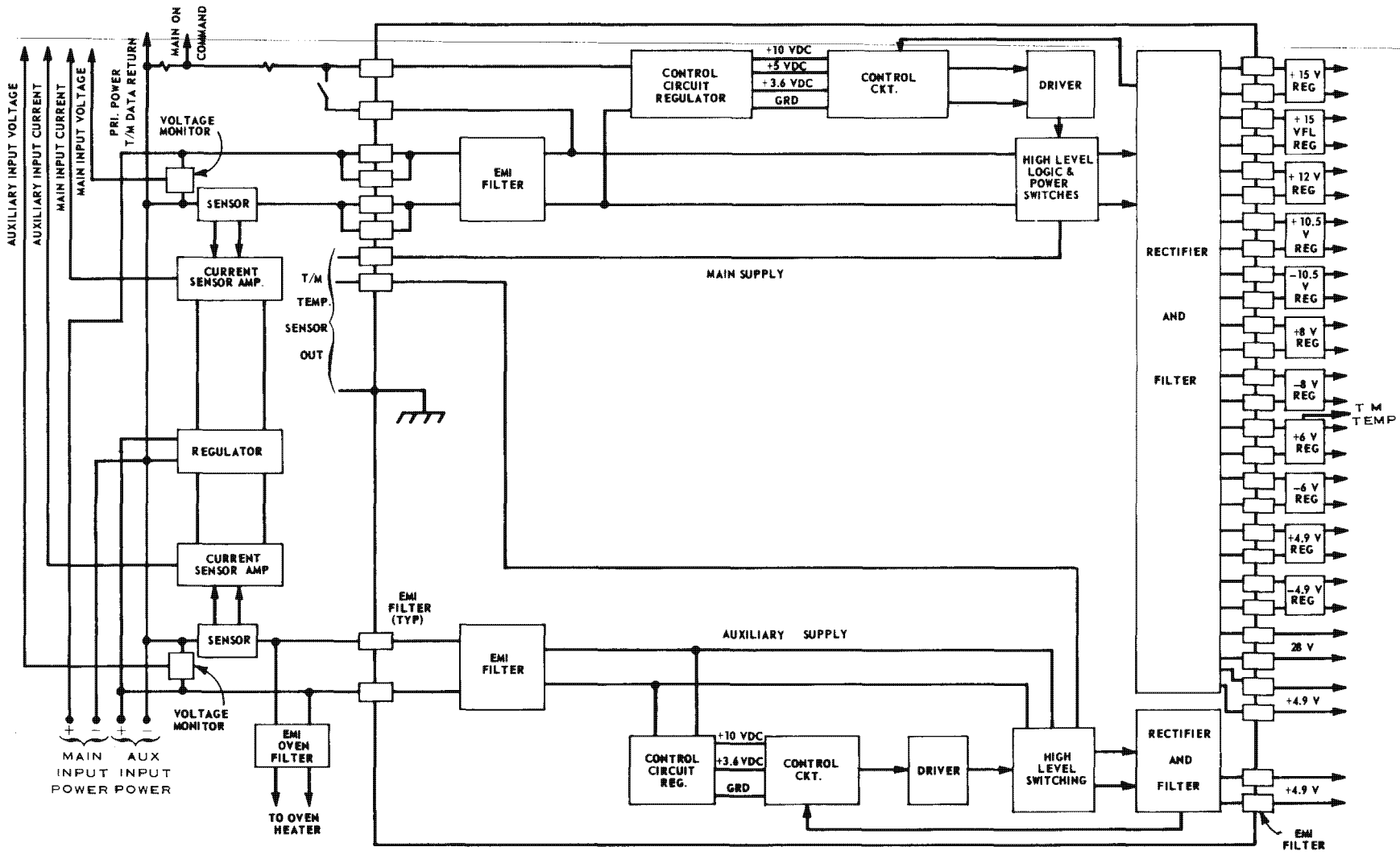

Figure 4.8-1. Power Supply Overall Block Diagram

The main power supply components are: Control Circuit, Driver, High-Level Logic and Power Switches, Rectifiers and Filters, and Regulators. The auxiliary power supply is essentially the same except that low level logic is used instead of high level logic. Current and voltage monitor circuits and EMI filters are also associated with both power supplies.

4.8.2 Control Circuitry

4.8.2.1 Introduction - The control circuitry of the main supply is shown in Figure 4.8-2. Waveforms are illustrated in Figure 4.8-3.

The square wave generator output A is both integrated and differentiated, producing waveforms B and C, whose sum D is a triangular peaked waveform appearing at one input to the comparator. The error voltage is applied to the other input. When the instantaneous value of waveform D passes above the error voltage, the output of the comparator changes level and a square wave is produced as in E.

As the level of the error voltage shifts up or down, the leading and trailing edges of the output square wave shift about the crossovers of the triangular wave and error voltage, varying the duty cycle. The positive and negative spikes on waveform D prevent an inoperative condition when the error voltage becomes larger or smaller than the peak values of the triangular wave alone.

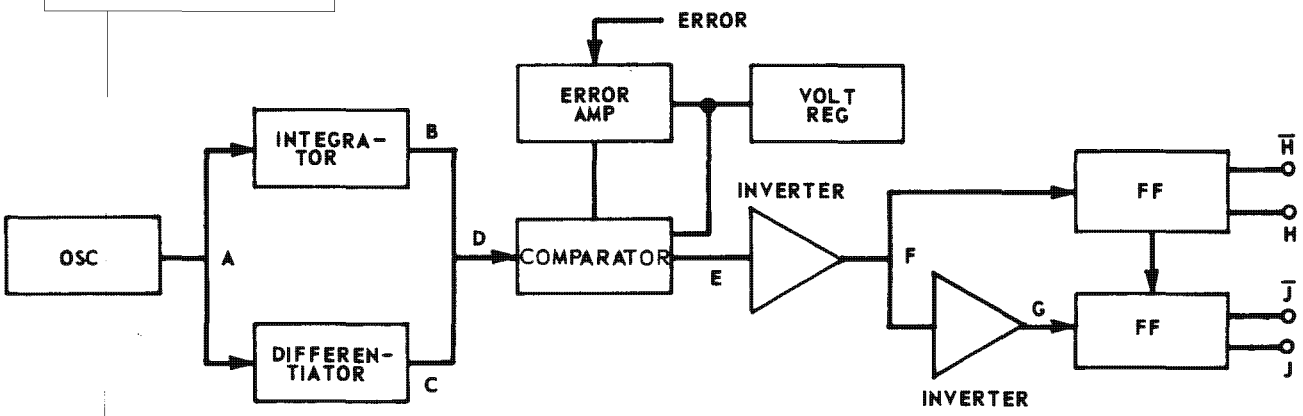

Figure 4.8-2. Control Circuitry Block Diagram

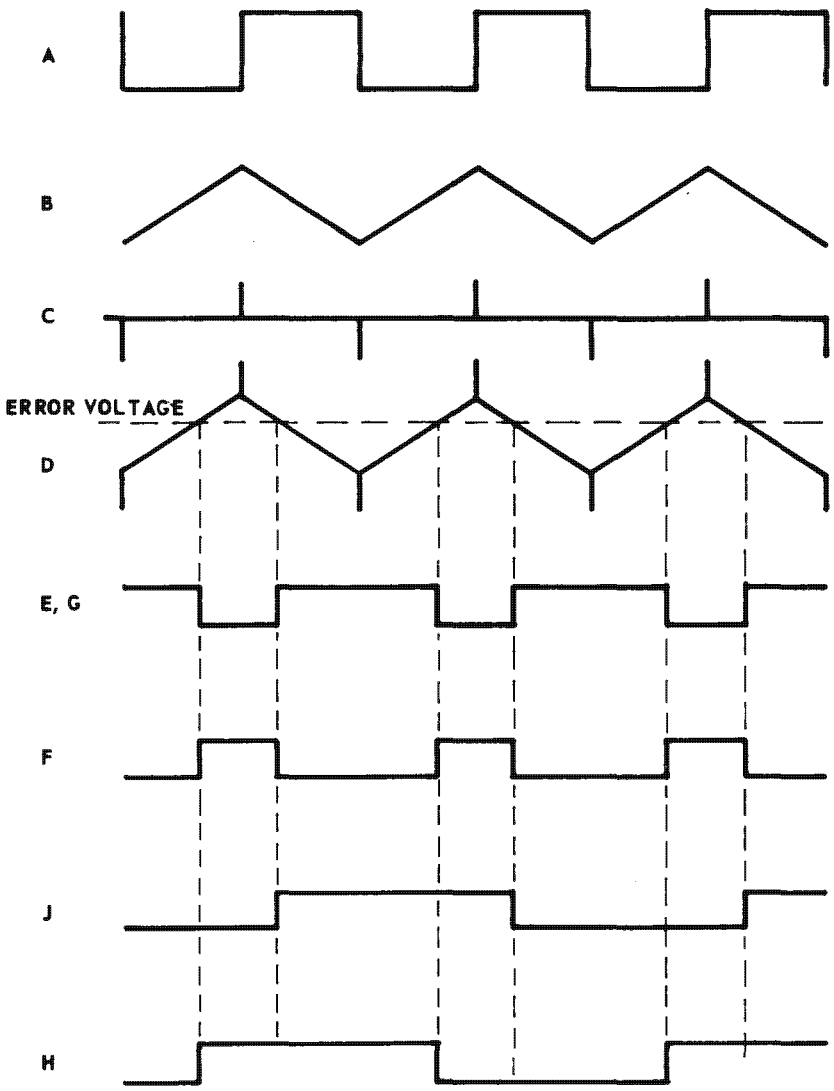

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Figure 4.8-3. Control Circuitry Waveforms

The inverter circuit produces complementary waveforms F and G to drive the flip-flops which produces symmetrical waveforms H and J. The phase difference at the corresponding flip-flop outputs is equal to the duty cycle produced by the error voltage. The flip-flops are interconnected so that the state of one controls the state of the other to prevent a 180-degree phase ambiguity when DC supply power is first applied.

4.8.2.2 Square-Wave Generator - The square-wave generator is a self-starting symmetrical multivibrator composed of two of the gates in a uL 927 quad inverter. The 24 KHz frequency is controlled by the equal time-constant pairs of RC networks connected to the base of two 1/4 parts of the uL 927. To ensure a square-wave output of approximately equal rise and fall times the collector of each inverter is also returned to the supply voltage by an external resistor and diode. The output is taken from the collector of the inverter where symmetry is maintained because the charging current from the coupling capacitors flows through the external resistor which is isolated from the output by a diode.

4.8.2.3 Integrator - The integrator is an integrating amplifier customarily referred to as a Miller integrator. The amplifier is biased Class-A and is direct coupled between the oscillator and comparator. The collector voltage is Zener regulated. The voltage driving the Zener is also regulated.

4.8.2.4 Differentiator - The differentiator circuit consists of a series capacitor and resistor with another resistor introduced at the output of the integrator. Current summing of the integrator and differentiated waves produces a triangular peaked waveform at the input to the comparator. This waveform is directly coupled to one input of the comparator and the controlling error voltage is introduced into the other.

4.8.2.5 Comparator - The comparator is a uA702A analog integrated element operating without feedback. The operational amplifier is biased with two positive voltages of +10 and +3.6 V. Since the triangular waveform is DC coupled, the bias level of the integrator is adjusted for the best operating level. A square wave of controlled duration is taken from pin 8.

4.8.2.6 Inverter - The inverter is two $\frac{1}{4}$ parts of the uL 927 connected as a cascaded pair of saturating amplifiers between the comparator and the flip-flops. They serve to provide complementary inputs to the flip-flops and thereby preserve the duty cycle information in the form of phase difference between the two symmetrical square waveforms of the flip-flops.

4.8.2.7 Flip-Flops - Two uL 948 J-K flip-flop elements divide the two complementary pulses by two, providing complementary, symmetrical outputs displaced from each other in time

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by the width of the comparator output pulse. To prevent 180-degree phase ambiguity when DC power is first applied, the flip-flops are interconnected so that the state of one controls the state of the other. Pin 11 of one is connected to pins 4 and 9 of the other. Complementary outputs are obtained from pins 9 and 6 of each flip-flop.

4.8.3 Driver Circuitry

The driver circuitry is a high current-gain circuit used to supply the drive for the driver transformers which in turn drive the high level logic circuitry and switching power amplifiers. It features push-pull operation with each driver conducting for 180 degrees. The driver transformer operates in square wave operation. Two identical sections of driver circuitry are used to handle the phasing required for the high level logic. See Figure 4.8.4.

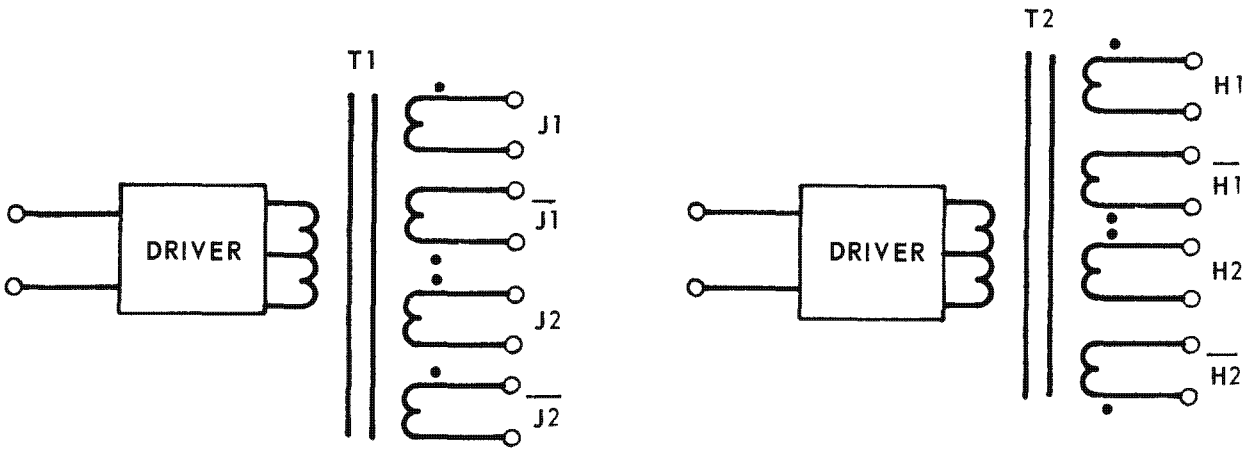

Figure 4.8.4. Driver Transformers

4.8.4 High-Level Logic Circuitry

The on-time of the ouptut power switch required to maintain constant input power with line voltage variations is determined by the control circuitry. This information is stored by the operation of the two flip-flops in two symmetrical square waveforms with their phase difference being proportional to the on-time of the cycle. These symmetrical square waveforms can then be easily handled and amplified. At a much higher power level, the turn-on will be recovered by the high-level logic and furnish drive for the output transistor power switch. See Figure 4.8-5.

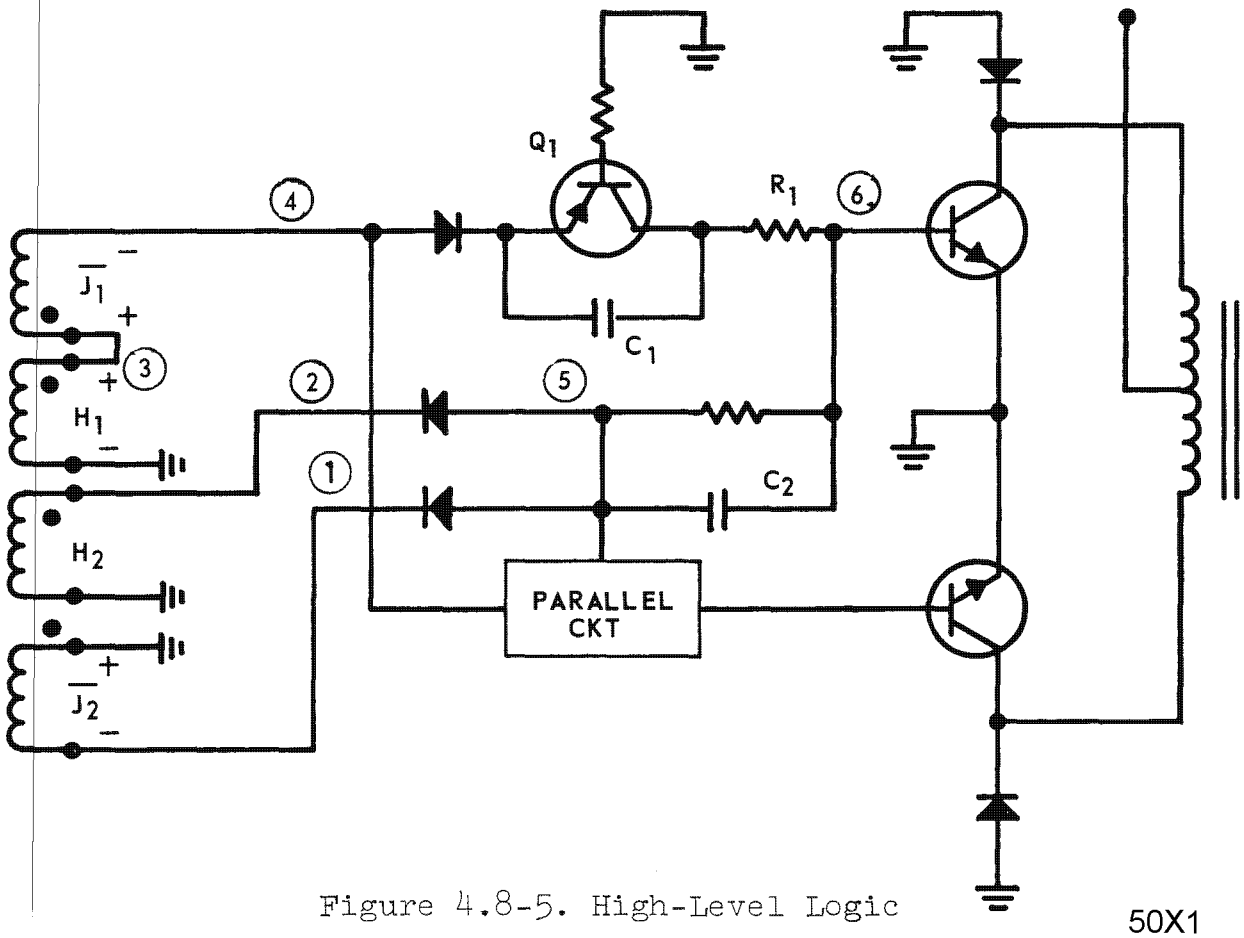

Figure 4.8-5. High-Level Logic

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The secondary windings of the driver transformers are connected to the high level logic circuits which recover the "on-time", determined by the control circuit, and drive the output power switches. The power switches are driven in push-pull operation and each half of the push pull has parallel power switches in keeping with reliable power dissipation tolerances. The diodes on the collectors of the switching transistors are for negative spike protection.

Figure 4.8-6 shows the waveforms in the high level circuitry.

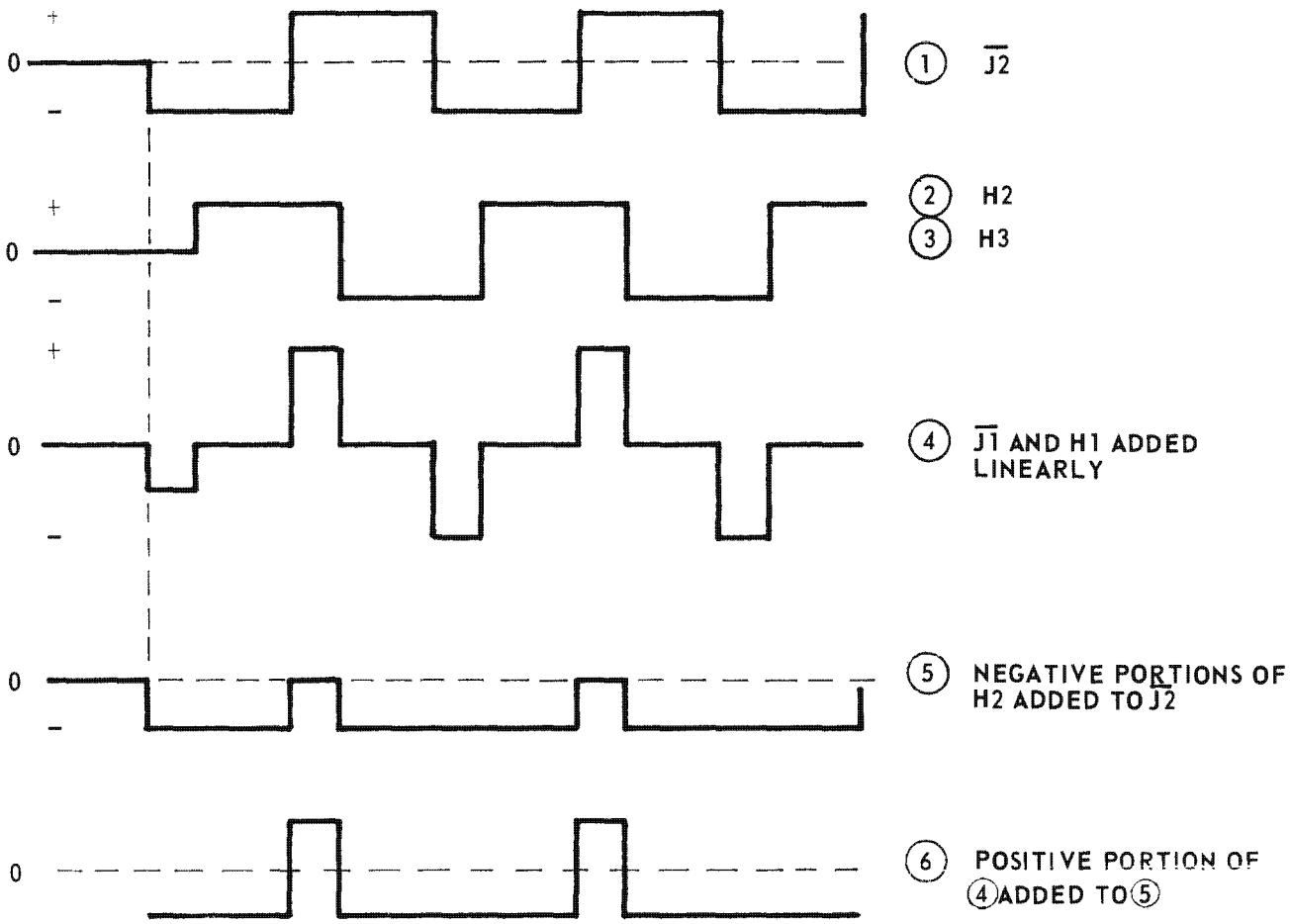

Figure 4.8-6. High-Level Logic Waveforms

Waveform 5 in figure 4.8-6 provides the turn-off signal at 6 and is generated by combining H2 and $\overline{J2}$ in a logical OR gate. When either H2 or $\overline{J2}$ is negative, 5 is negative; otherwise it is zero. The diodes to 5 junction assure that only a negative-going output will appear at 6. Capacitor C2 determines the charge initially removed from the output transistor base to effect turn-off, and the resistor in parallel serves as a discharge path for C2 and to provide a direct path to the output transistor base to maintain cut-off.

Waveform 4 in Figure 4.8-6 provides the turn-on power at 6 and is generated by adding J_1 and H_1 linearly. During the turn-on time, the diode at 4 junction is forward biased and Q_1 is driven into saturation. A path therefore exists to the output transistor base 6 for a turn-on current limited by resistor R_1.

Isolation between the turn-on and turn-off circuits is provided as follows. During the turn-off interval at 4 from Figure 4.8-6 the diode to the emitter of Q_1 is either 0 biased or reverse biased and Q_1 is held off. During the turn-on interval the diodes at 2 and 1 are reversed biased and the signal amplitude at 6 is less than the amplitude at 2 and 1 so that the diodes are held off.

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4.8.5 Output Stage

The output stage consists of four power-switching transistors transformer coupled to the rectifiers and filter circuitry. This stage supplies power to 13 loads, and voltage to a reference amplifier for input power regulation. A separate winding for the reference voltage is used to provide isolation between input and output. The four transistors are arranged in pairs in a push-pull configuration and held alternately on and off by positive and negative-going signals from the high-level logic circuitry. The output transformer operates as a linear transformer. The secondaries are center tapped and two diodes are used for full wave rectification. Output filtering uses LC components. Parallel rectification is used for the +5-volt to improve effeciency.

4.8.6 Reference and Error Amplifier

Voltage regulation for input power is provided by the error amplifier and voltage reference. The error amplifier is an MC1533F operational amplifier. This unit feeds back an error voltage to the uA702A comparator to adjust the duty cycle of the output square wave from the control circuitry.

4.8.7 Auxiliary Power Supply

The auxiliary power supply is also of the switching type with high efficiency using integrated circuits in the con-

trol circuitry. Due to the lower power requirement, the logic can be done at low level by the use of two integrators, two differentiators and two comparators. The comparators serve as the drivers to the output stage and the drivers used in the main supply can now serve as the output stage. The output transformer operates as a linear transformer. The secondaries are center tapped and two diodes are used for full wave rectification. LC filtering is used. The auxiliary supplies power to one load and to its own reference amplifier on a separate winding for input power regulation and input to output isolation.

The auxiliary power supply is used to provide continuous regulated power to the time encoder, TM circuitry for P/L ON, Partial Scan Buffer and associated relays.

A block diagram of the auxiliary power supply is shown in Figure 4.8-7.

4.8.8 Voltage Monitor

The voltage monitor is made up of colpitts oscillator with a transformer-coupled output for isolation from the main line. The detected output varies directly with the line voltage.

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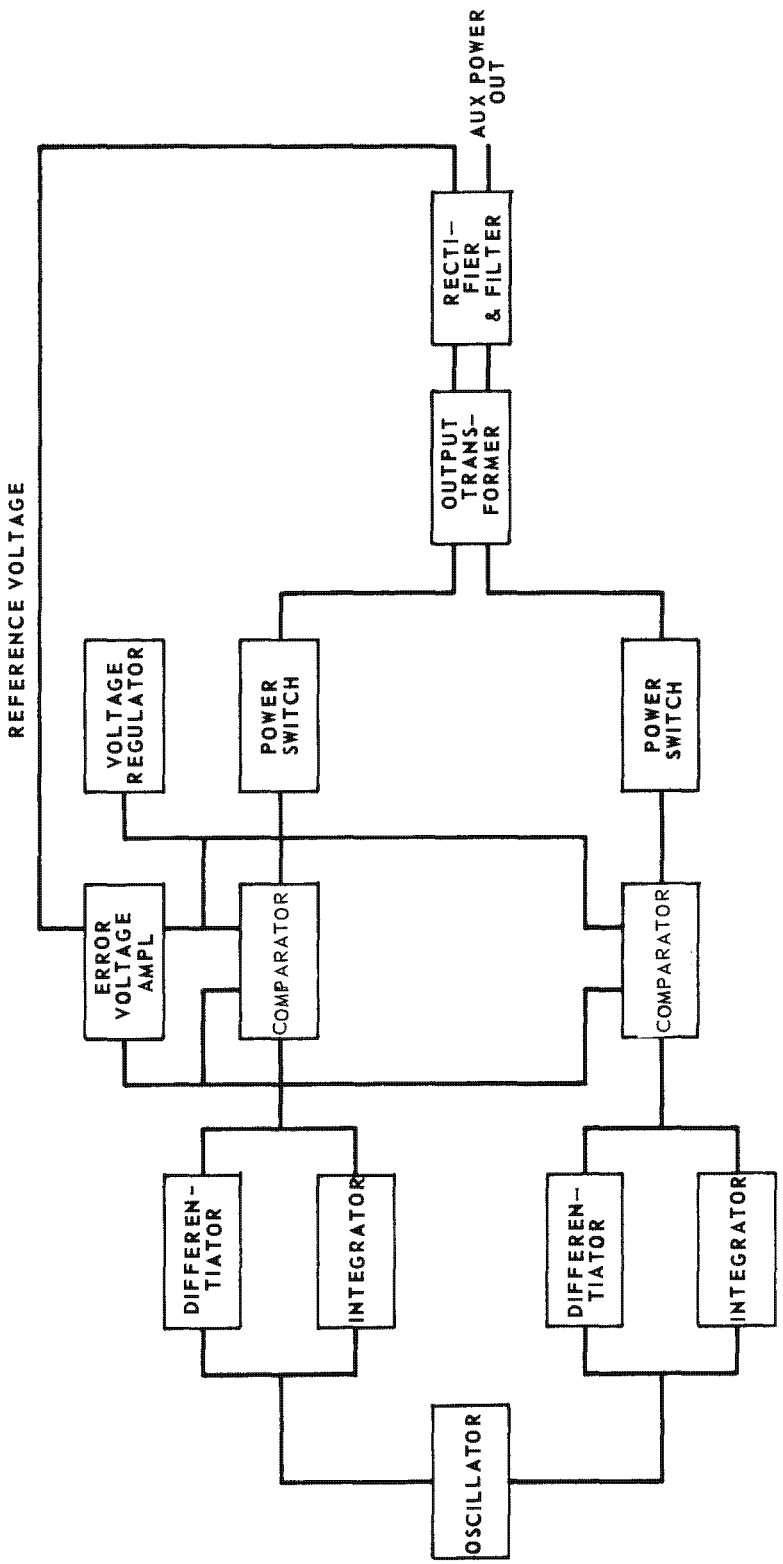

Figure 4.8-7. Auxiliary Power Supply Block Diagram

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4.8.9 Current Monitor

The sensing element for the main supply current monitor consists of two parallel strands of #18 (.040 dia.) Nichrome wire (0.414 ohm/ft.) 0.57 ± 0.005-inch long which measures 0.1 ohm. The auxiliary supply sensing element is a 1 ohm wire wound resistor. The voltage drop across this sensing element is amplified by an MC1533F integrated circuit operational amplifier. The primary voltage through a series regulator provides power for the current monitors.

4.8.10 EMI Filters

4.8.10.1 EMI Oven Filter - The oven filter is a balanced LC low-pass filter with a 12 db/octave slope starting at 200 cycles with greater than 70-db attenuation at 20 KHz.

4.8.10.2 EMI Line Filter - The EMI line filter for the main power supply is a balanced 4-pole critically damped Butterworth filter and is impedance matched. The EMI line filter for the auxiliary is of the same type.

4.8.10.3 RFI Filters - All lines in and out of the power supply are RFI filtered.

4.8.11 Voltage Regulators

The voltage regulator is a series regulator with unity feedback and with Zener reference comparison for temperature compensation and voltage control. The reference circuitry consists of a temperature compensated Zener and an MC1533F operational amplifier integrated circuit. The regulators

40 mv p-p output ripple to the load. The voltage ripple tolerance vs. frequency on the line voltage is also shown. The power supply will operate satisfactorily with input-line ripple considerably in excess of that specified.

50X1

supplying power to the recognizer are current limited for short circuit protection so that failure in the recognizer would not affect the operation of the rest of the system.

4.8.12 Power Supply Performance

Power supply performance is described in a series of typical performance graphs. Figure 4.8-8 shows the converter efficiency vs. source voltage with a total of 2% change from 22 volts to 29.3 volts. Figure 4.8-9 shows the converter efficiency at 22 volts source voltage vs. temperature from -40°C to +100°C. The efficiency with temperature varies from approximately 70% at -40°C to 61.5% at 100°C.

Figure 4.8-10 is a typical plot of the output voltage vs. temperature and source voltage for the auxiliary power supply. A maximum variation of approximately 3% is shown.

Figure 4.8-11 shows the variations of a high power output voltage, +5.0 volts, with respect to temperature and source voltage. The variation is less than 2%. Figure 4.8-12 shows a typical regulator performance from -40°C to 100°C with a variation of less than ±0.1% for the +8-volt load. Load changes effect on the voltage are much less than 0.1%. The +8-volt load was varied from 0 to 120% of rated load with less than 1.0 mv change on the voltage.

Figure 4.8-13 shows a susceptibility response for applied line voltage ripple vs. frequency for a constant

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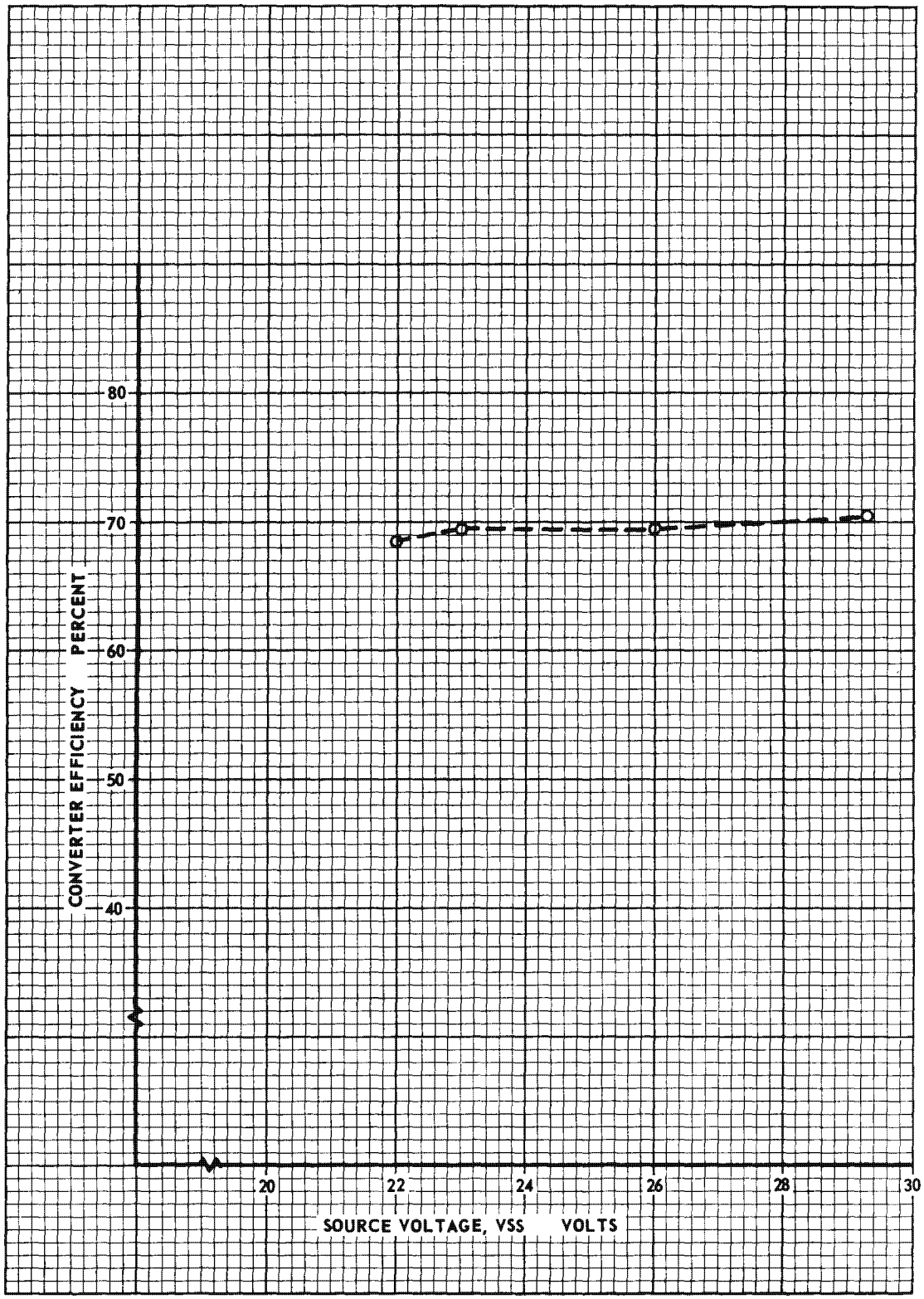

Figure 4.8-8. Converter Efficiency vs Source Voltage

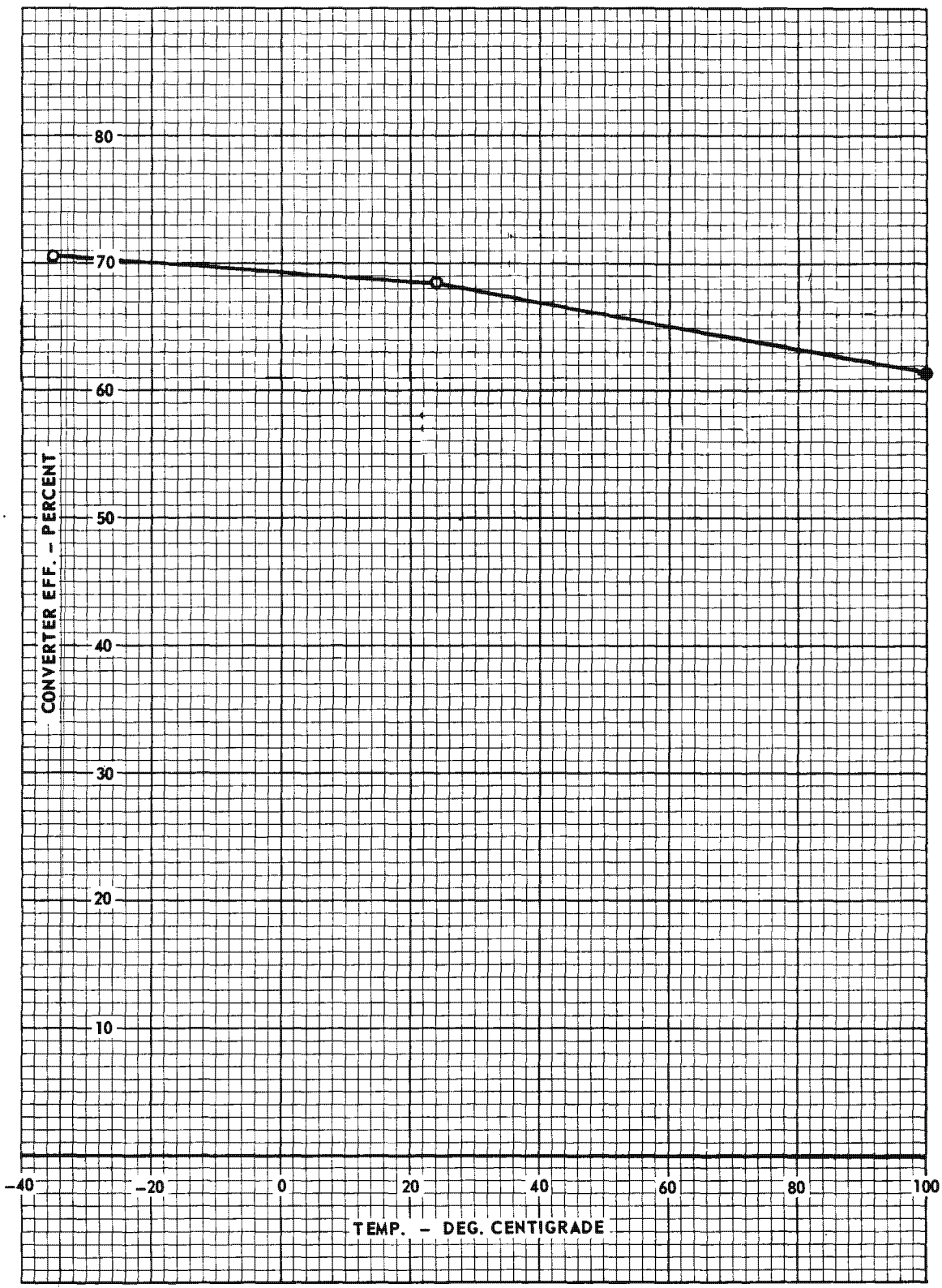

Figure 4.8-9. Converter Efficiency vs Temperature

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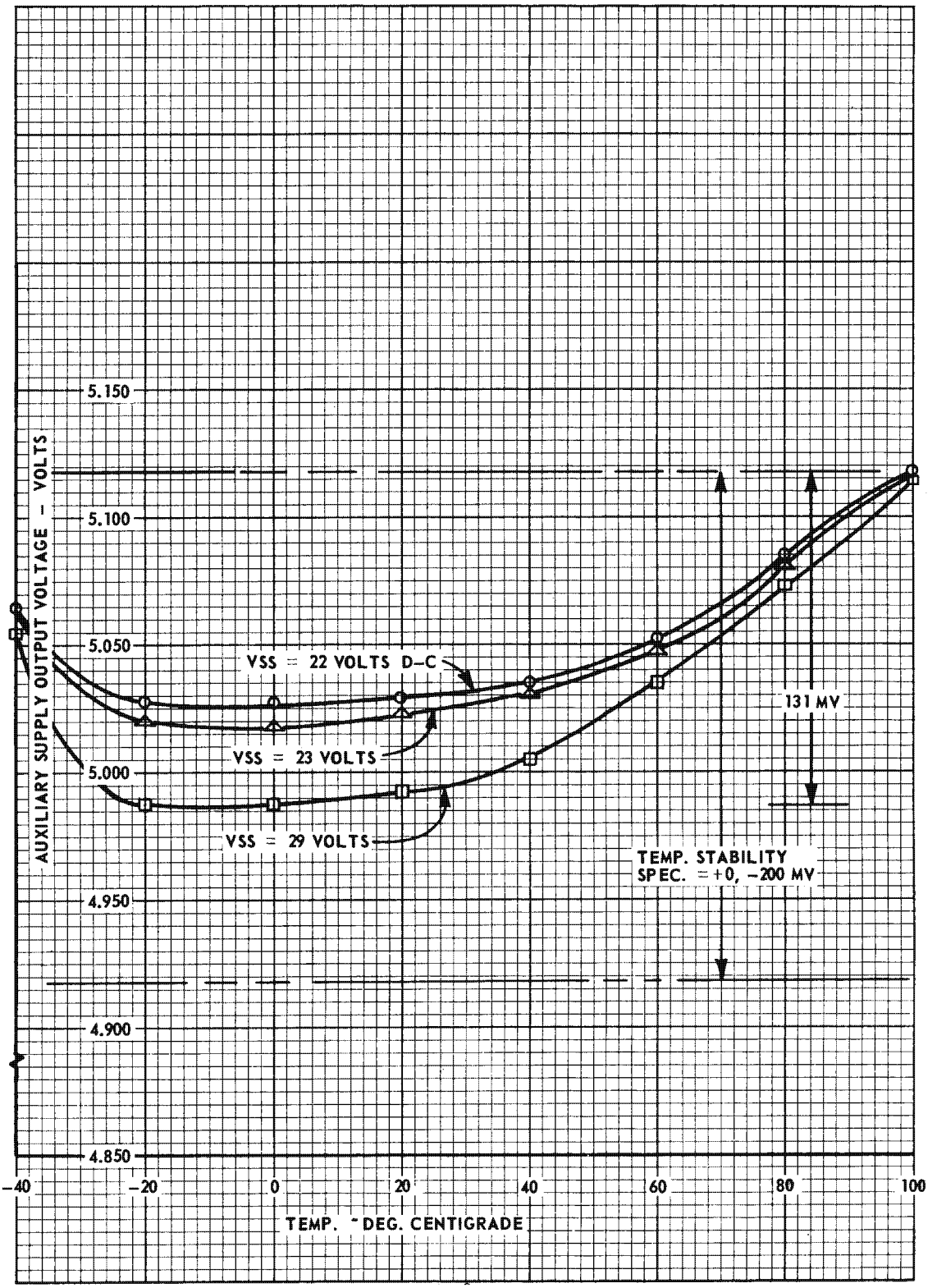

Figure 4.8-10. Auxiliary Power Supply Output vs Temperature and Source Voltage

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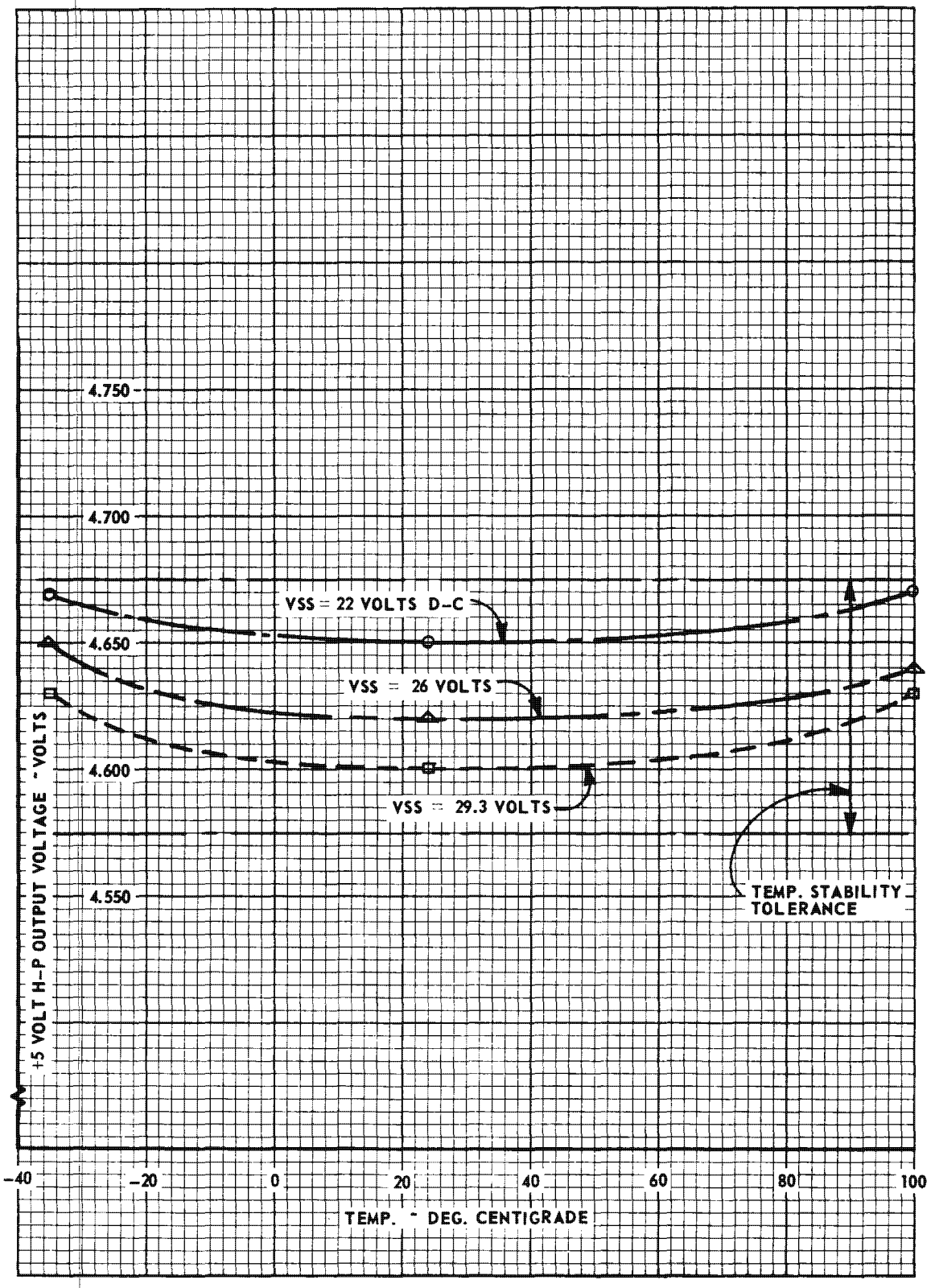

Figure 4.8-11. +5-Volt High Power Output vs Temperature and Source Voltage

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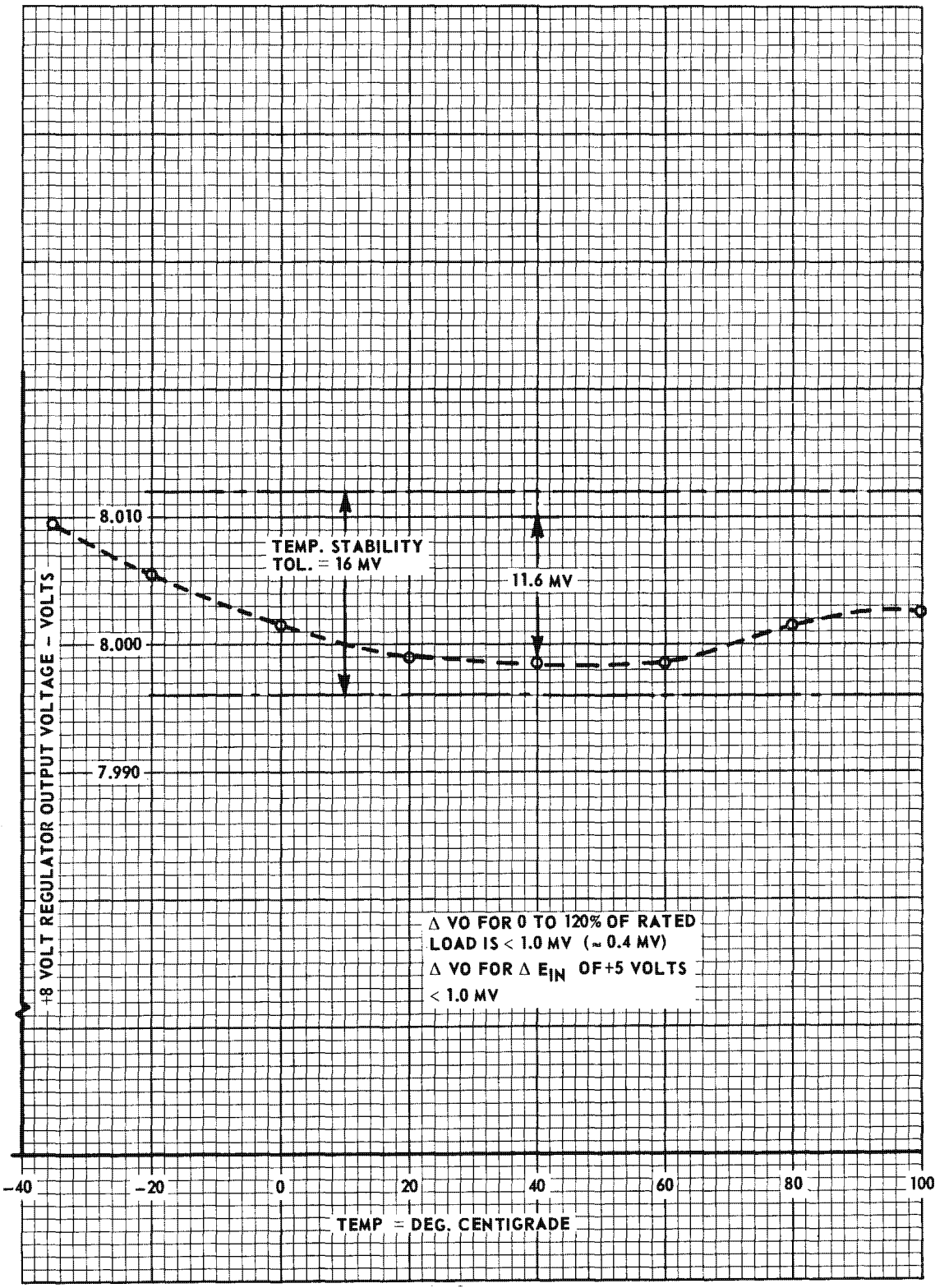

Figure 4.8-12. Typical Regulator Output

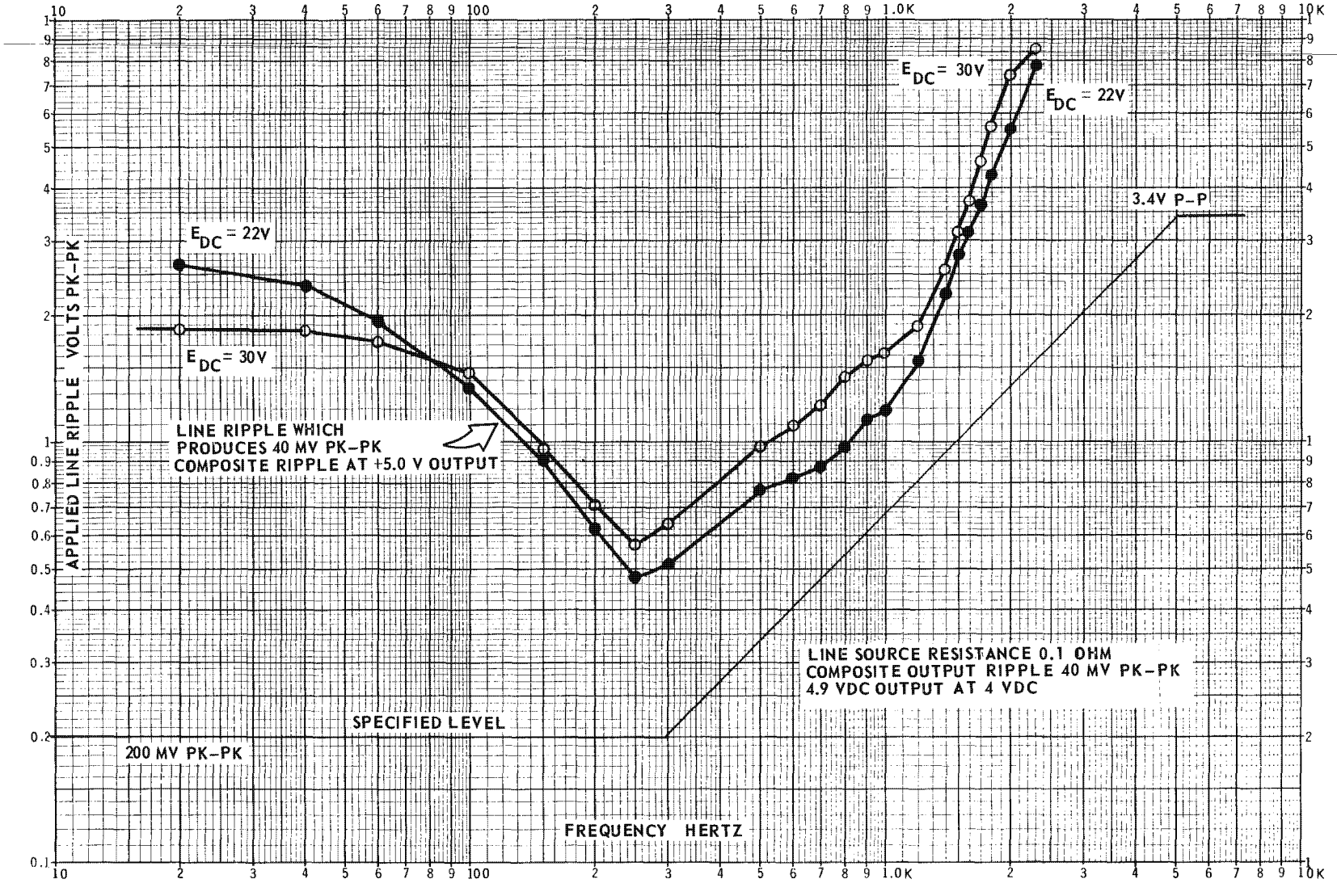

Figure 4.8-13. Susceptibility Response

4.9 Mechanical Design

4.9.1 Introduction

The major objectives in the Mechanical Design were to provide mechanical integrity, light weight and ease of test and check out. These objectives were achieved by employing a modular configuration providing the capability of testing at the subassembly level and access for circuit level repair.

System weight was specified at 234 pounds. A weight optimization indicated that to achieve this goal a common base plate must be provided for all subassemblies. To be an optimum structure both mechanically and from a weight standpoint, the material for the base plate was chosen to be aluminum honeycomb. Magnesium was used wherever practical to further improve on the overall weight budget.

With the use of magnesium and the aluminum honeycomb base plate, total weight for the system was estimated at 215.05 pounds. Actual weight proved to be pounds.

Figure 4.9-1 illustrates the assembled system.

The following paragraphs outline the detailed mechanical and packaging design used in the subsystem hardware.

4.9.2 Common Base Plate and Support Structure

The common base plate, to which all subassemblies attach, is a 1.032-inch thick panel with a 1-inch thick aluminum honeycomb core of 5059-H39 aluminum foil having a density of 5.7 pounds per cubic foot. The core foil is .002 inch

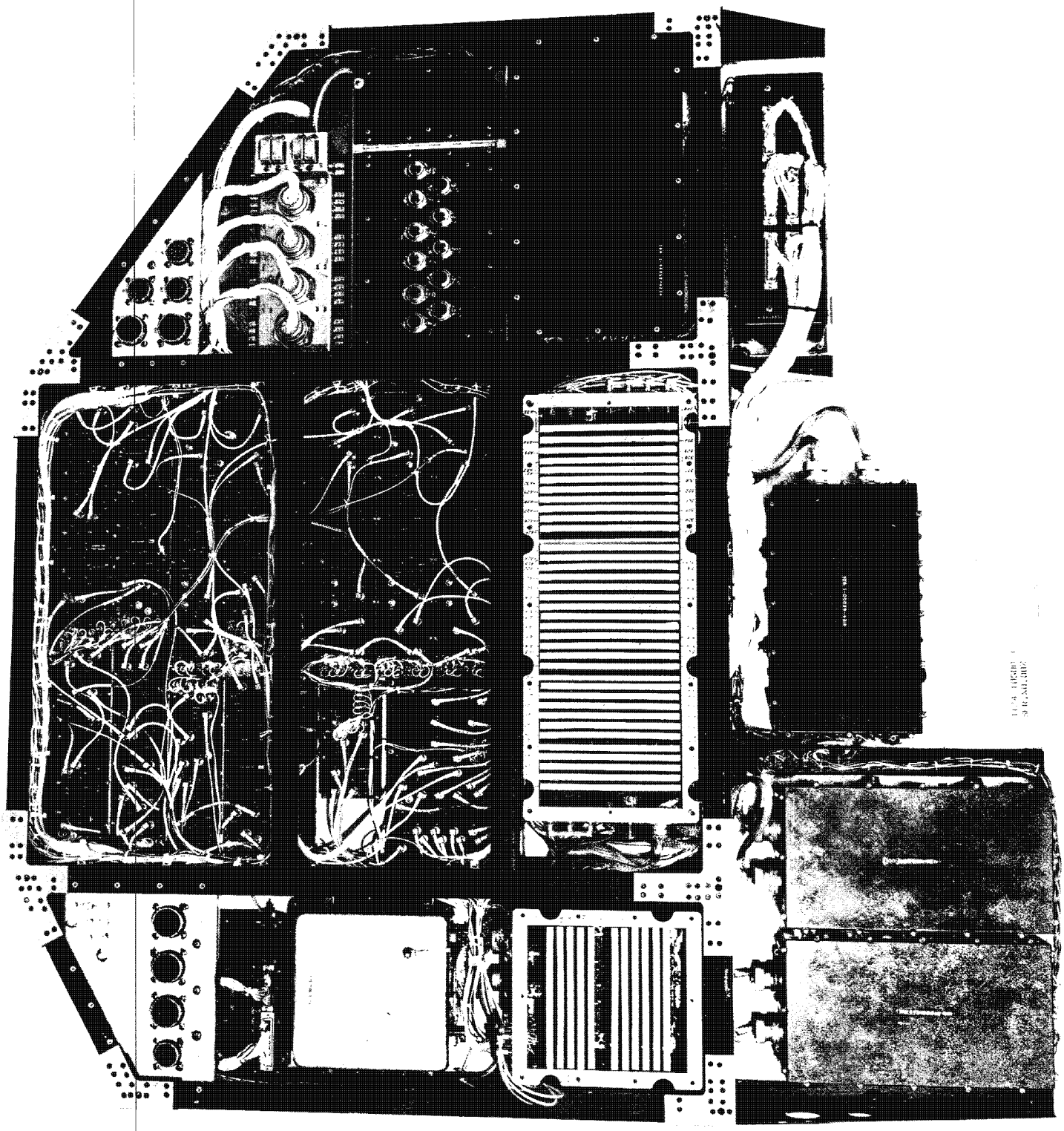

Figure 4.9-1 Complete System - Front View With Absorber Removed and Antenna Covers in Place.

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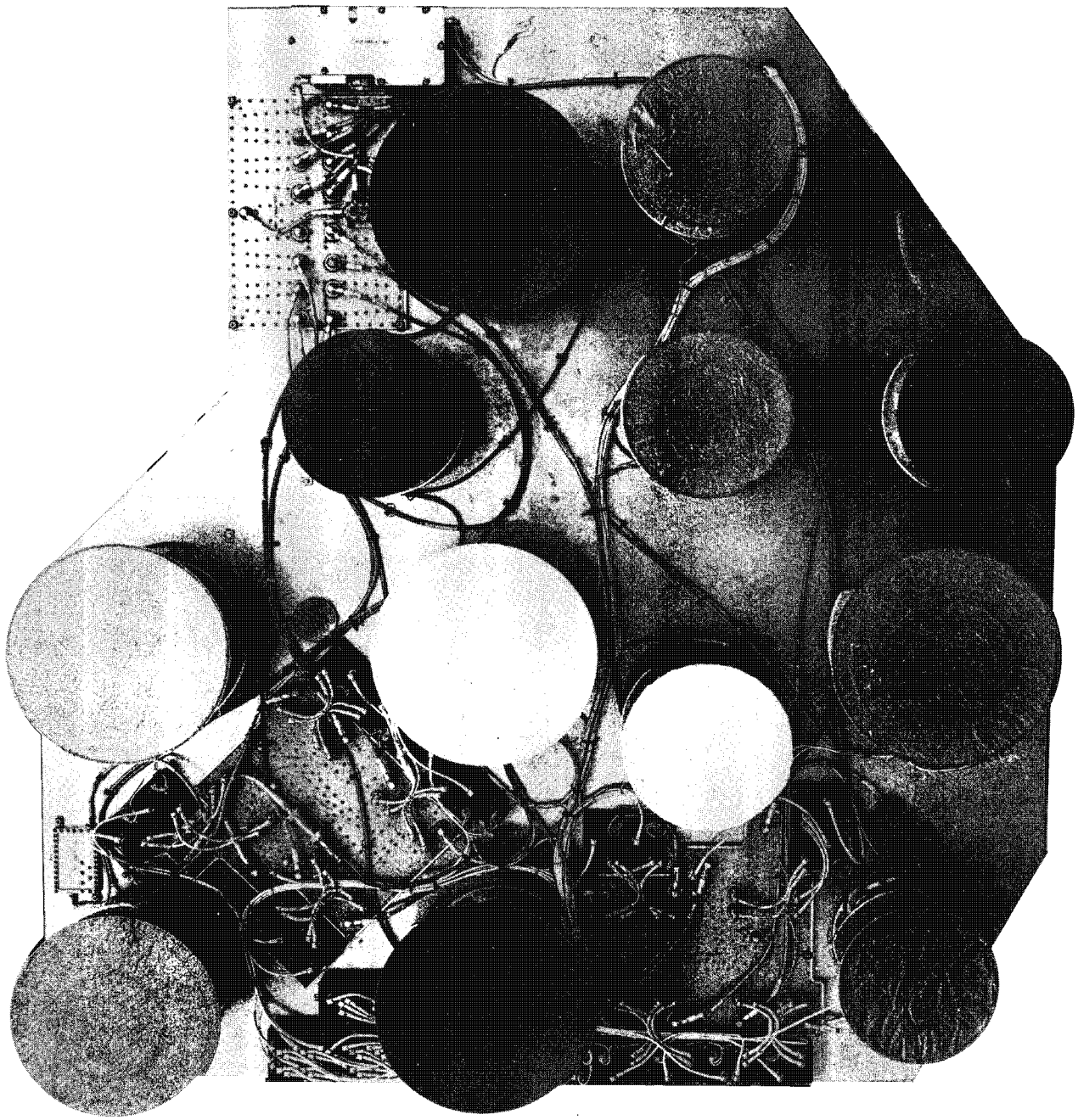

Figure 4.9-1 (Con't) Complete System - Rear View (Data Handler Covers Removed)

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thick and is perforated to allow air venting. Cell size is 5/16 inch. The facesheets of the panel are 0.016-inch thick 7075-T6 alclad aluminum and are bonded to the core using FM-1000 adhesive film. To attach subassemblies to the panel, threaded aluminum inserts are potted into the panel using EPON 828 potting compound, filled with 40% aluminum powder. Inserts are provided for two bolt sizes, 10-32 and 8-32.

To bridge the gap between the honeycomb panel and the mounting interface of the complete system an additional channel structure is used. The structure consists of 0.090-inch thick 6061-T6 sheet aluminum bent to form a U channel 3.65 inches high with 1.25-inch flanges. The sections of this structure are riveted together and the whole channel structure is attached to the honeycomb panel using a combination of 31 No. 10 bolts for good tension coupling and Bondmaster M777 adhesive bonding for good shear coupling. Figure 4.9-2 shows the combined structure.

4.9.3 Antennas

Two types of antennas are used in the system horns and spinals. The phase horn, of which there are 10 in the system, is shown in Figure 4.9-3 and consists of three parts. The receiving funnel and wave guide is composed of a single cast aluminum part. The resonant cavity is a separate casting. The two parts are bolted together with the antenna stripline and feed assembly sandwiched between them. The stripline and feed assembly

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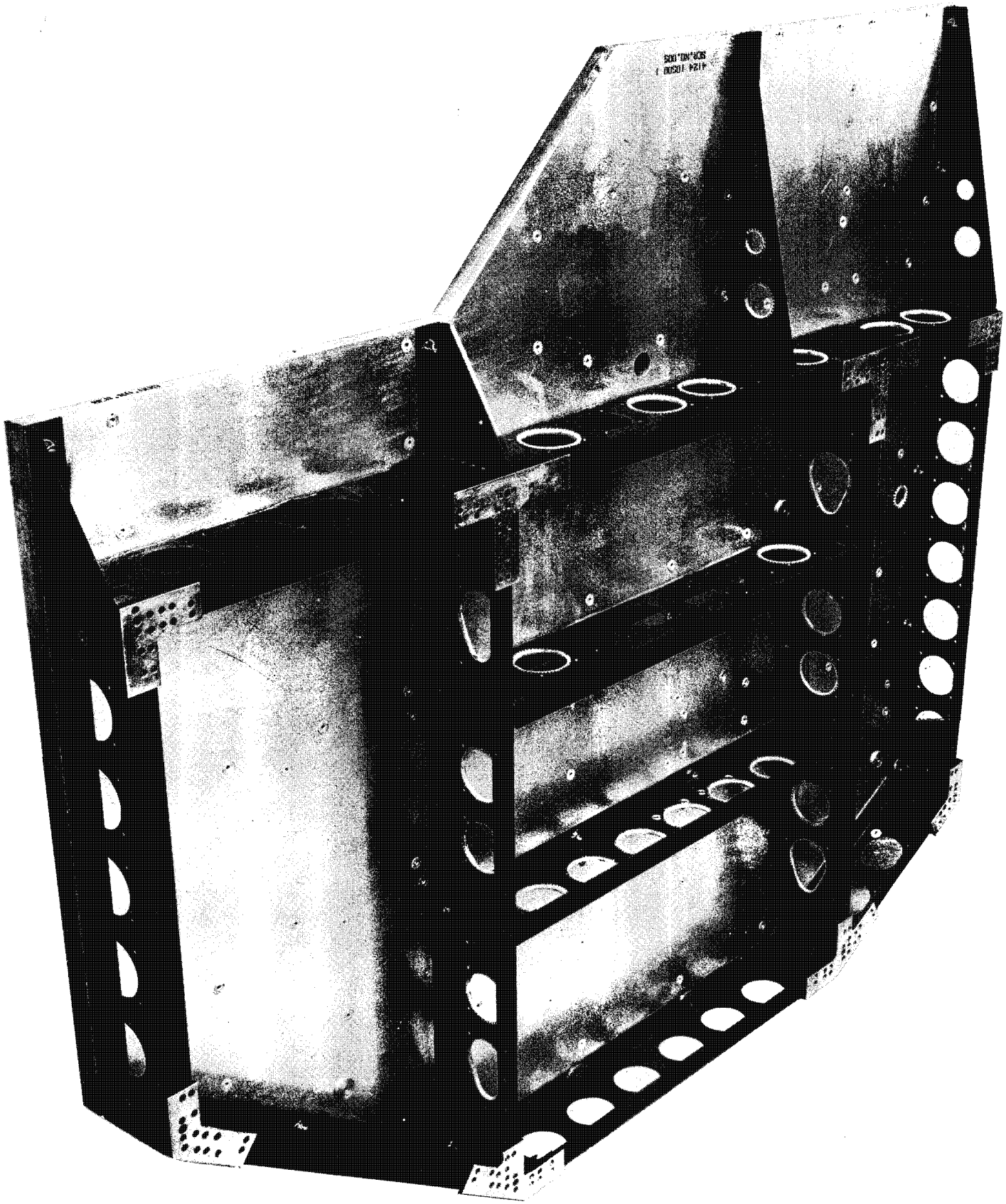

Figure 4.9-2 Support Structure

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FIGURE 4.9-3. PHASE HORN

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is composed of a copper printed circuit on a fiberglass reinforced teflon board substrate. The copper-teflon board is enclosed by aluminum plates on top and bottom and by aluminum foil around the sides. The stripline is covered with Humiseal 1A27 for moisture protection. All exposed aluminum surfaces of the antennas are protected by an alodine 1200S chemical finish. In addition the surface of the receiving funnel is painted white for proper thermal control. The amplitude spiral, of which there are two in the system, is shown in Figure 4.9-4.

4.9.4 IF Section and A/D Converter

The units of the IF Section and the A/D Converter are of similar packaging design. They include the IF Phase Channel, Log IF, Amplitude Ratio, R/I Logic, SI Generator, Frequency Confirm Predetector, Hybrid and Recognizer Threshold. Only one unit, the IF Phase Channel, will be described in detail. The general description is valid for the remaining units.

Figure 4.9-5 shows the IF Phase Channel. It consists of 26 cordwood modules mounted in two rows in a compartmental aluminum alloy housing. The compartments of the housing act as shielding between modules. The housing has an alodine 1200S finish on the interior surfaces and a black epoxy finish on exterior surfaces.

The cordwood modules consists of two 0.013-inch thick, double-sided, solder-plated, printed-wiring boards with components mounted between them. The printed-wiring boards are

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FIGURE 4.9-4. SPIRAL ANTENNA

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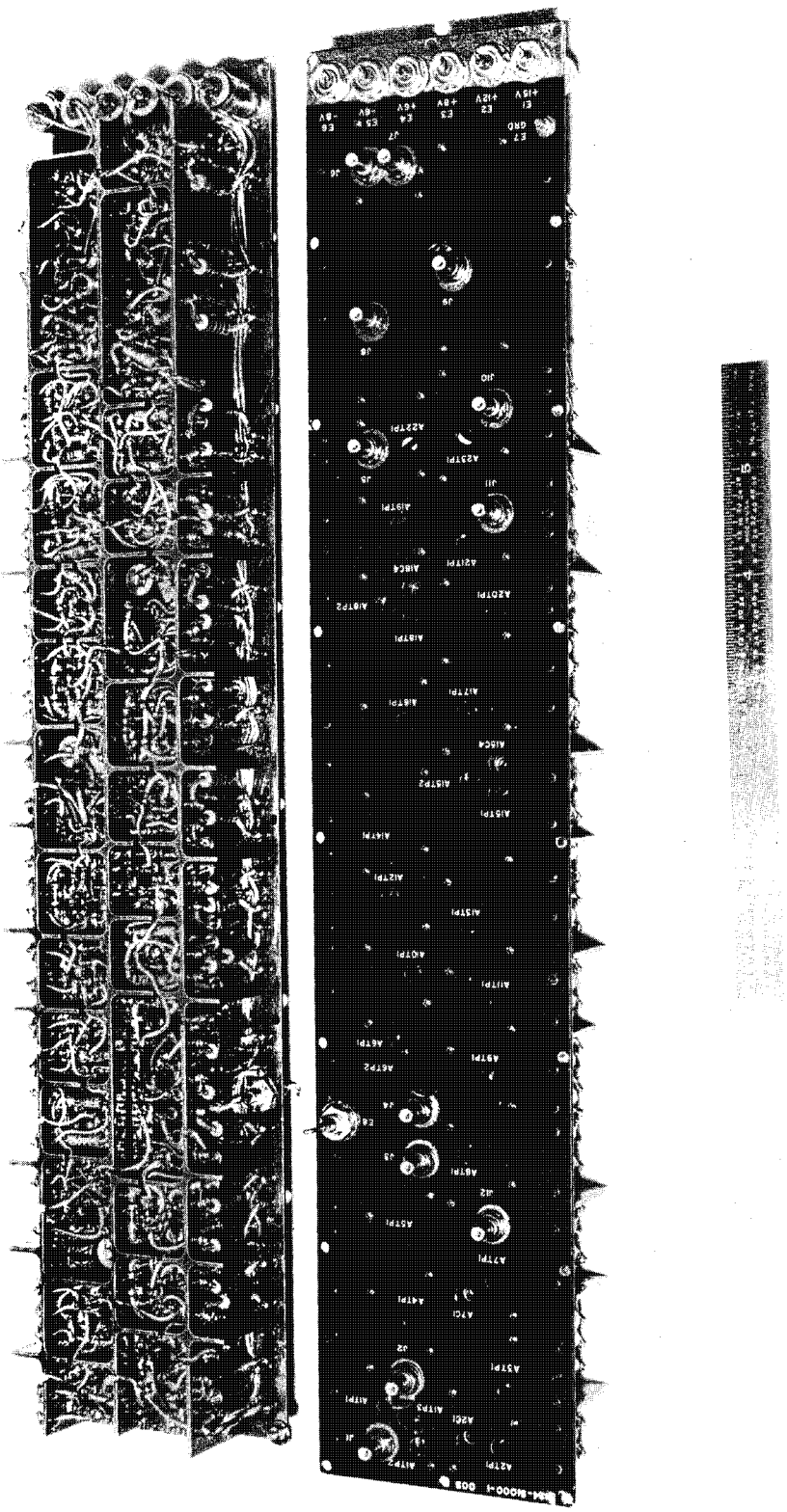

Figure 4.9-5 IF Phase Channel

designed with slots and access holes to enable components to be replaced with a minimum amount of time and without removing any other component. Component parts are supported only by their leads except in special cases where additional support is provided by the application of an RTV potting compound between the component and one or both of the printed circuit boards. The printed-wiring boards feature plated-through holes and plated edges to insure continuity on both sides of the board. Eyelets are used on the printed-wiring boards for terminating interconnecting wires.

Voltage decoupling components are mounted adjacent to each module on the chassis wall which isolates it from the module and the other decoupling. The decoupling components are mounted on standoff terminals which are pressed into the chassis wall. The terminals are hollow to permit connection of the voltage wires into the modules from the decoupling without losing RF isolation in the module. All signal sources, either entering or leaving the phase channel assembly, are shielded from RF interference by the use of gold plated subminiature RF connectors that meet or exceed the requirements of MIL-C-22557. Terminations, test points, and component adjustments are made accessible from one plane on the top chassis plate.

After the assembly is electrically checked, the cordwood modules are dipped in Humiseal 1A27 for environmental protection. The chassis is then mounted in one of two common

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housings containing the major portions of the IF Section. These common housing are in turn mounted directly to the honeycomb base plate.

4.9.5 Data Handlers

Construction of the two Data Handlers is similar to the IF Section construction. Figure 4.9-6 shows a Data Handler housing with the top cover removed. Figure 4.9-7 illustrates a typical Data Handler card. The housing is composed of aluminum alloy plates riveted together to form a ridged container closed on all sides except the side that mounts on the honeycomb base plate. This side is left open to save weight and to allow easier access to signal wires concentrated in the lower part of the housing.

Inside the two Data Handlers are more than 900 integrated circuits of the flat pack design. The integrated circuits are parallel-gap soldered to double-sided nickel-clad solder-plated printed-wiring boards. The boards are mounted in pairs on a 0.016-thick aluminum alloy frame. These frames serve a dual role of providing a means of heat transfer to the main housing and also providing a rugged sliding surface on each edge of a board-pair. The sliding surfaces fit into spring clips on each side providing a means for removing an individual board from the Data Handler for ease in check out of the system and for repair. The spring clips guide the boards into edge-type connectors which are interwired by soldered connections. The printed wiring

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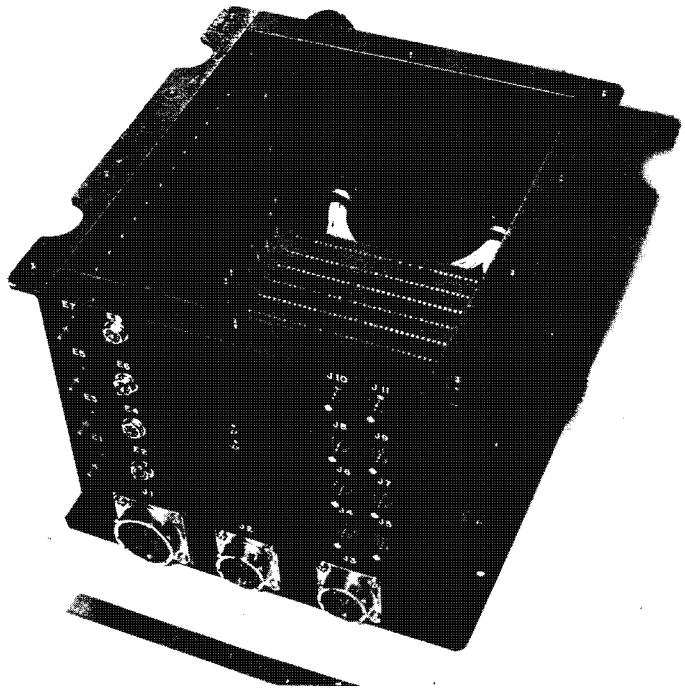

Figure 4.9-6 Data Handler Housing

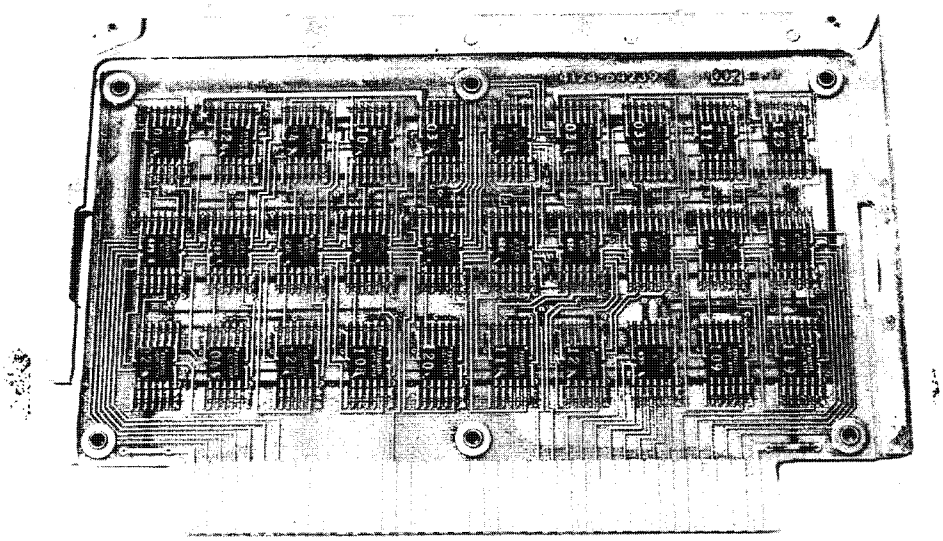

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Figure 4.9-7 Data Handler Card

boards incorporate many redundant circuits for increased reliability.

4.9.6 Memories

A typical memory is illustrated in Figure 4.9-8. There are three such memories, the buffer storage, the recognizer memory and the SWI memory. A typical memory consists of a housing and a top cover; both are machined from magnesium tooling plates.

Inside the housing, a large printed circuit board and a ferrite core stack sandwiched between two smaller printed boards are mounted on risers on the bottom. These components are separated by stand offs and 4 common stainless steel screws.

In the top cover, a second large printed circuit board is mounted using risers machined into the cover. The top cover is not completely removable from the housing because of the necessary cable connections between the two parts. It may be swung back off the main housing to permit accessability to all separate parts. Figure 4.9-9 shows the top cover opened on one of the memories.

The larger printed-wiring boards are approximately 11" X 6" and contain driver circuitry for the memory stack. The number of such circuits depends on the size of the ferrite core stack. The Recognizer stack consists of 14 planes with 2048 cores on each plane. The SWI and Buffer Storage stacks consists of 8 planes of 2048 cores each. There are 64 cores

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Figure 4.9-8 Buffer Storage

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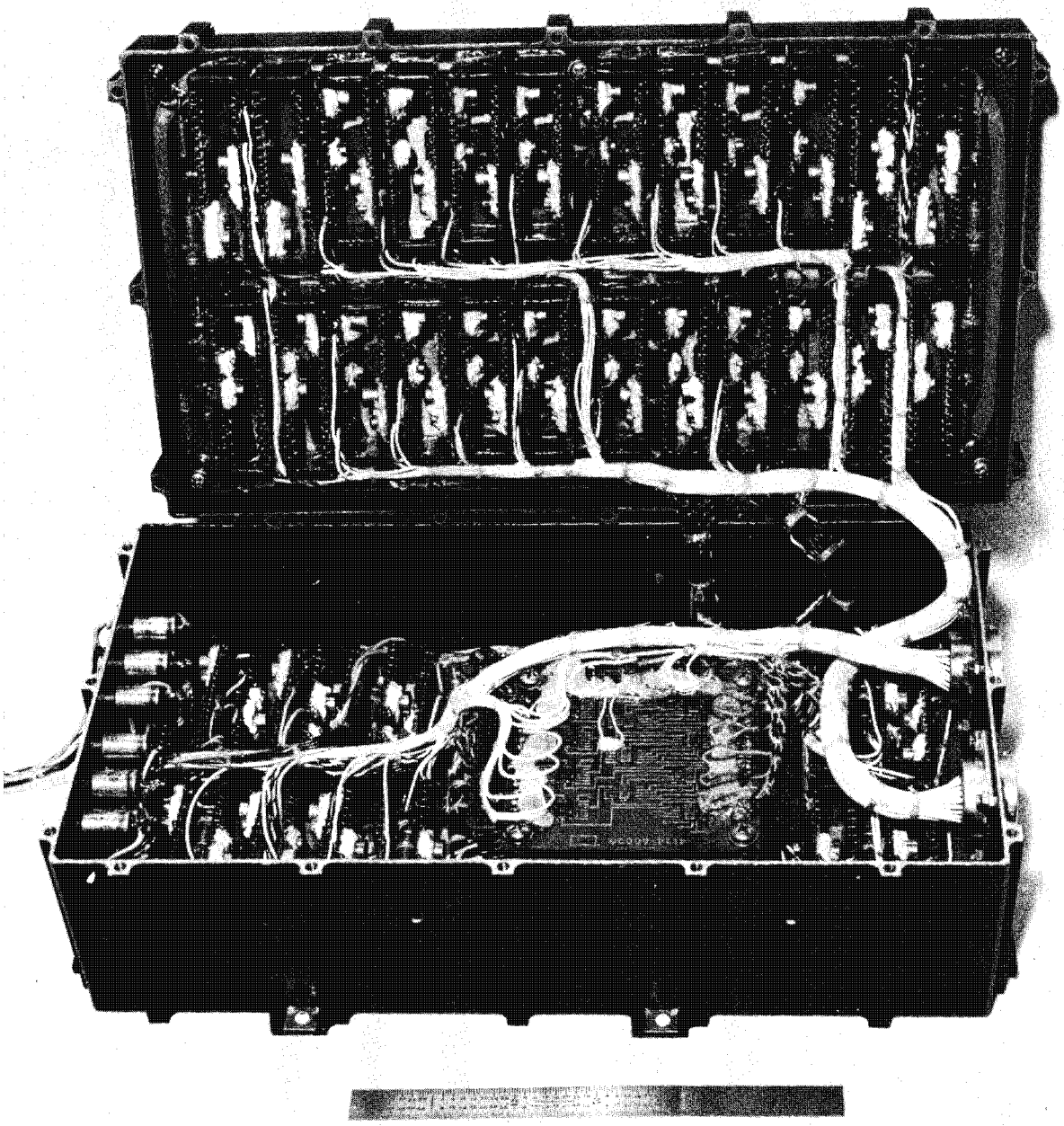

Figure 4.9-9 Memory With Cover Open

on each plane. Above and below the ferrite stack the smaller solder-plated printed-wiring boards contain flat pack integrated circuits which are the sense amplifiers. Driver circuits are modular in form and are composed of two slotted printed-wiring boards spaced approximately 0.5 inches apart. Electrical components mounted on the inside surface of each board. Individual driver circuits can be easily removed without disturbing any of the other circuitry on the large printed-wiring boards.

The inside and outside surfaces of the housing and top cover are finished with black epoxy paint to optimize removal of heat from the memory units.

9.9.7 Local Oscillator

The local oscillator is composed of three major circuit elements. The YIG oscillators, the current drivers and the D/A converter. The YIG oscillators and current drivers are housed in a common container.

The container is composed of an outer shell made from a deep drawn magnesium box. Because of the temperature sensitivity of the current drivers and YIG oscillators, the container is also constructed to be an efficient temperature control oven. This is accomplished by bonding a 1/2-inch layer of thermally insulating foam around all inner sides of the magnesium shell. The components are then mounted to a copper base plate, suspended in the container by the use of four nylon standoffs.

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The YIG oscillators are mounted to the underside of the copper plate with a secondary aluminum plate. On the top of the copper plate the current drivers are mounted with some components attached directly to the plate while others are mounted on two printed wiring boards attached to the plate on stand-offs.

In the center of the plate are four heater blankets controlled by a porportional temperature controller which maintains the temperature of the complete assembly above 120 F at all times. This packaging design permits good accessibility for test and check out while maintaining the thermal isolation of the compounds. Figure 4.9-10 shows the assembly with the cover removed.

The D/A does not require temperature control and is packaged in a separate machined aluminum housing. The components are attached directly to the housing walls. Figure 4.9-11 shows this assembly.

4.9.8 Main Stripline Assemblies

There are three main stripline assemblies, the low band, the high band and the RF check out stripline. One typical assembly is shown in Figure 4.9-12. A typical stripline is made of a gold plated copper-clad printed circuit board sandwiched between .031 inch thick aluminum skins. The aluminum is finished with alodine 1200S and the complete assembly is conformal coated with Scotchcast 208 for protection from the elements. This construction yielded good electrical and mechanical stability with

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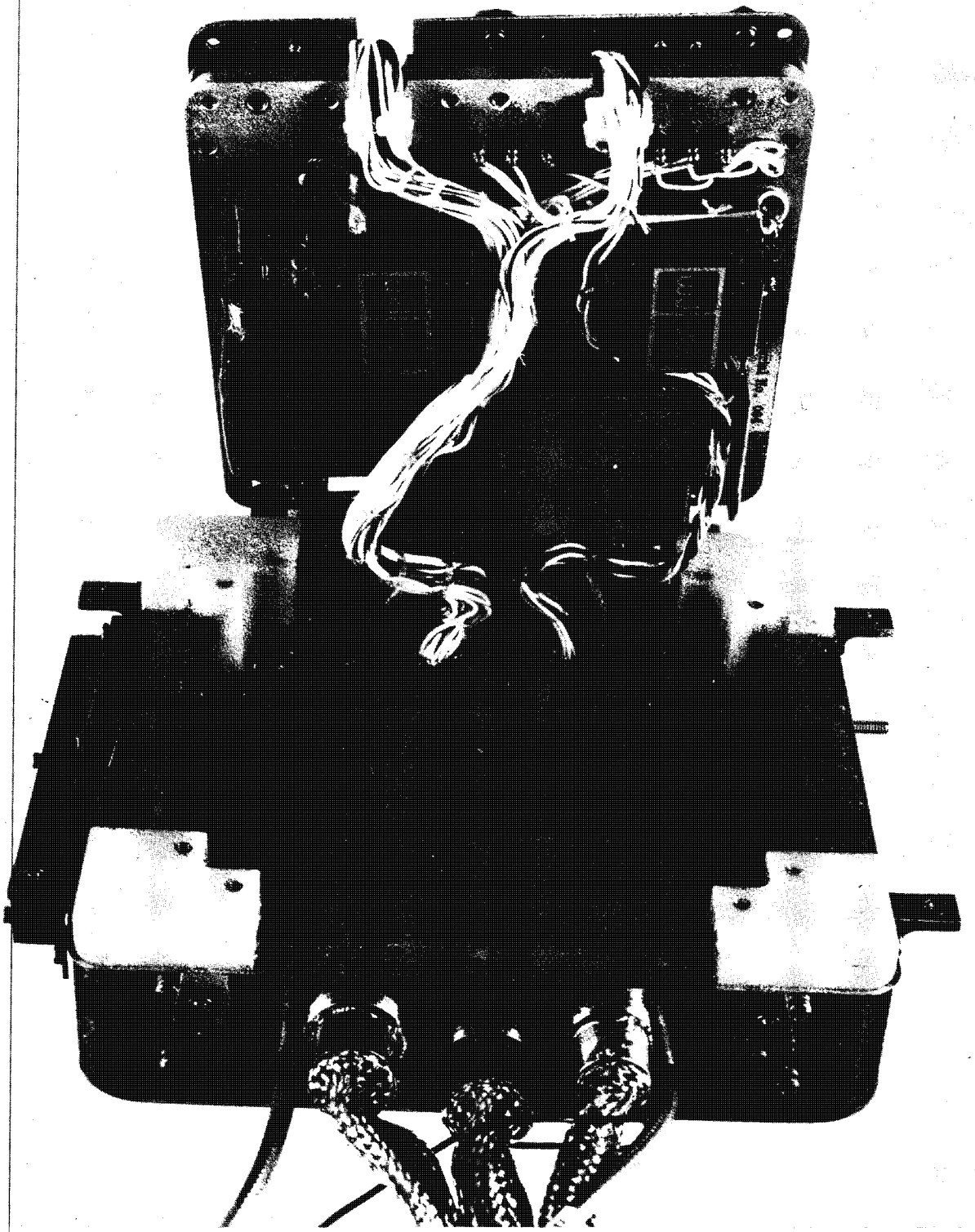

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Figure 4.9-10 LO Housing - Bottom Half with Electronics Exposed

FIGURE 4.9-11. D/A ASSEMBLY

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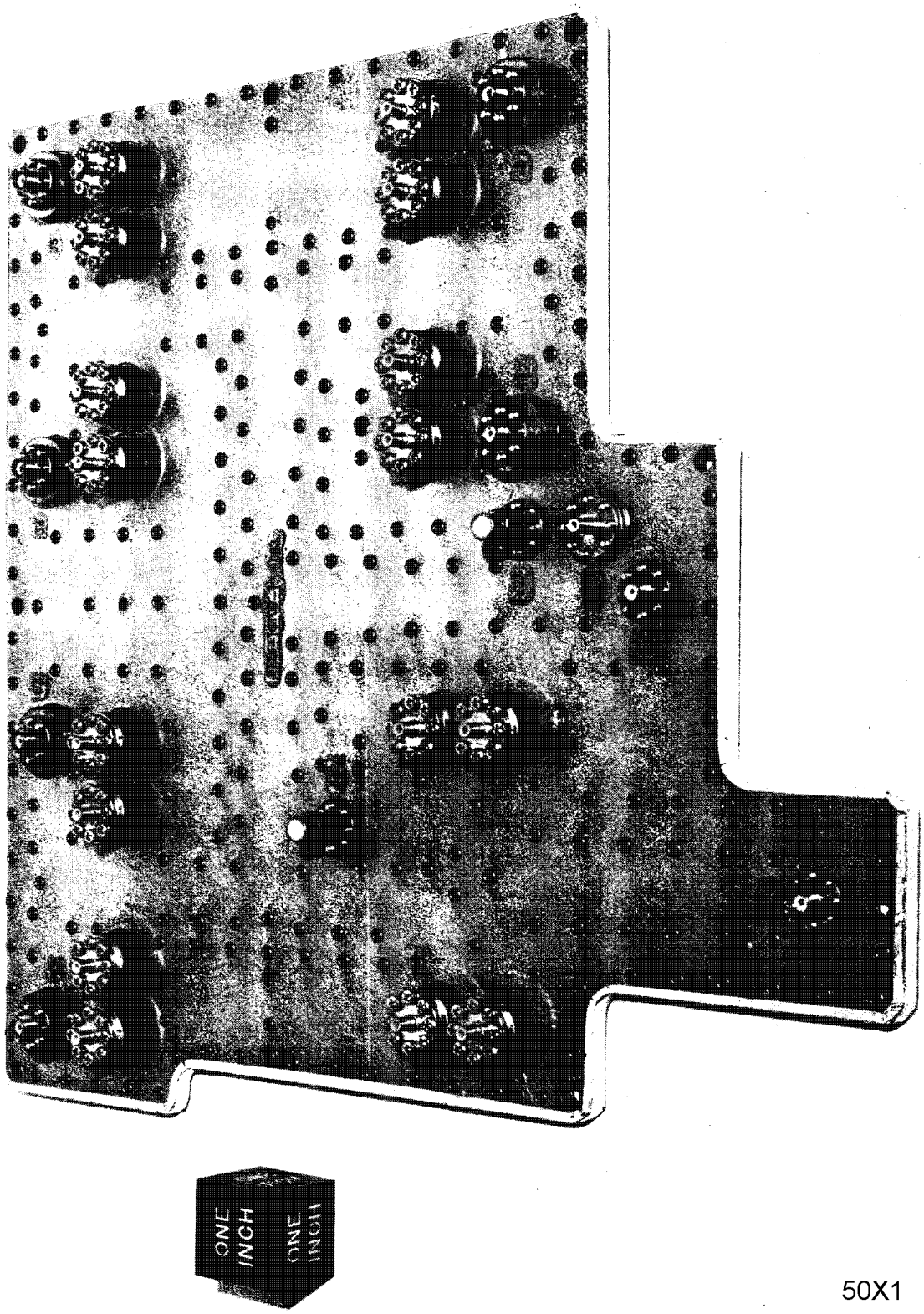

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Figure 4.9-12 Stripline Assembly

minimum weight.

4.9.11 RF System Calibrator

The RF System Calibrator consists of filters, attenuators and a low frequency oscillator integrated into a machined aluminum housing. Housing construction was chosen to provide an effective shielding between components and to insure mechanical stability. Figure 4.9-13 shows one view of the RF System calibrator.

4.9.12 IF Preamplifiers

The IF Preamplifiers are mounted in close proximity to the main striplines and are constructed similar to the IF Section, described in paragraph 4.9.4. There are a total of 16 separate IF preamplified in the system. Figure 4.9-14 shows one of the units.

4.9.13 Power Supply

The power supply housing consists of four parts, each of machined aluminum plate or blank. The four parts are: the top cover, the main power supply housing, the auxiliary power supply housing and the bottom cover.

The top cover and two housings are carefully sized to produce the optimum thermal characteristics for the unit. Heat dissipating components are evenly distributed within the separate parts to prevent an extreme buildup of heat at any location. Where hot spots cannot be prevented they are kept to a minimum by using methods such as intimate contact between components and housing as is represented by the power transistors

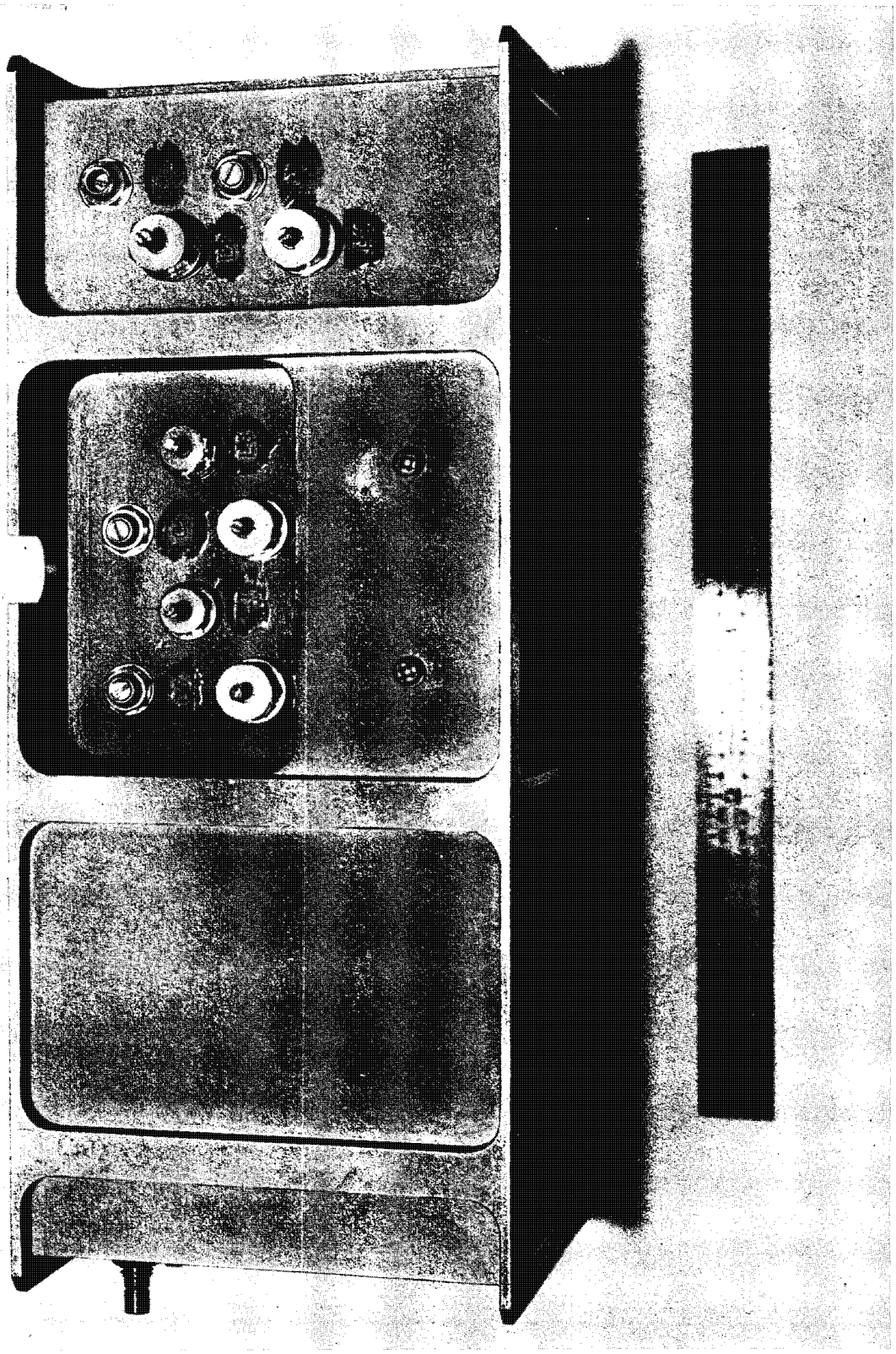

Figure 4.9-13 RF System Calibrator

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FIGURE 4.9-14. IF PREAMPLIFIERS

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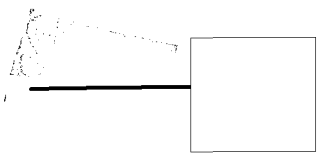

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which are mounted to a machined flange on the top cover. The cover is then made sufficiently thick so that heat is conducted to all parts of the plate with no significant thermal gradient.

The parts of the housing fit together with RF gasket interliners for optimum RF shielding. The bottom cover is primarily a RF shield serving no structural purpose. All power lines leave the unit through feed-through filters placed in the housing walls. This packaging concept provides an efficient unit from both an RF shielding and a thermal standpoint.

The power supply housing is illustrated in Figure 4.9-15.

4.9.14 Power Distribution Assembly

The power distribution assembly is composed of 0.062 aluminum plates rivited together. One of these plates serves as a horizontal base upon which 10 main terminal strips are mounted. A two part cover, each part being hinged to a vertical wall, provides a mounting access surface for the voltage regulator to most parts of the power distribution assembly without being completely removeable from the unit. The vertical wall also serves as support for additional bulkhead mounted voltage regulating elements.

Figure 4.9-16 shows the power distribution assembly with top covers hinged open.

4.9.15 Relay Assembly

The relay assembly housing consists of 0.062 thick aluminum plate formed into a channel with mounting flanges. The

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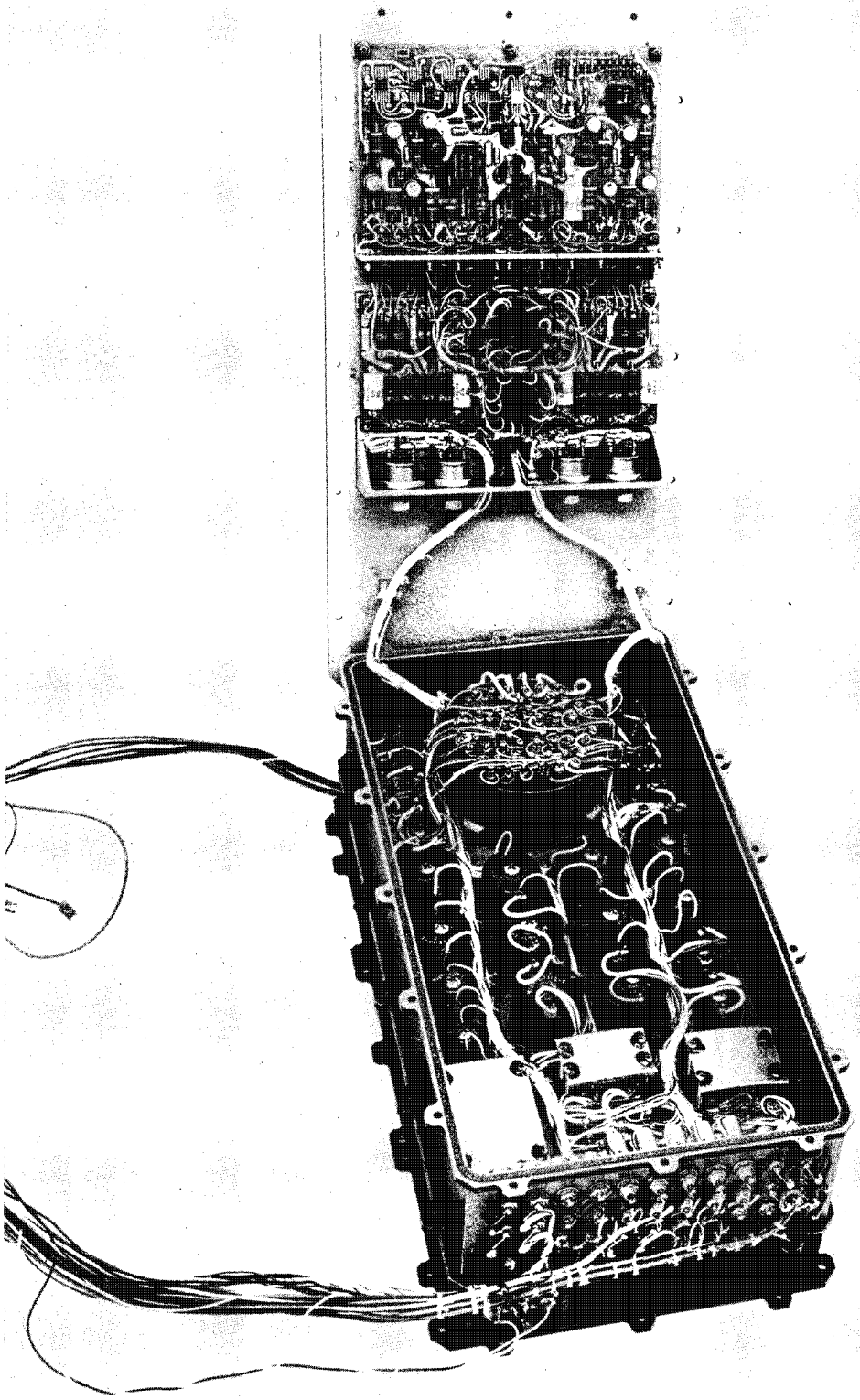

Figure 4.9-15 Power Supply with Top Cover Open

FIGURE 4.9-16. POWER DISTRIBUTION ASSEMBLY

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sides of the channel are pierced with slotted holes to provide bulkhead mountings for 37 Potter and Brumfield DPDT 2 amp relays. The top of the channel is used as a base for four 66-pin connectors through which power enters and leaves the assembly. On the top of the channel are also mounted four DPDT 10 amp relays, on a specially designed bracket mounted on top of the channel. Vertical terminal boards, approximately 3 inches apart within the channel help stiffen the whole assembly. This unit presents an extremely high packing density for the relays and interwiring.

Figure 4.9-17 shows the relay assembly.

4.9.16 T/M Assembly

Housing for the T/M assembly is made from 0.063 thick aluminum alloy sheet which is formed into a 5 sided box and all edges welded closed and contour ground. A narrow channel section of 0.063 thick aluminum alloy sheet forms the base plate of the housing. The top cover mounts to the base plate using eight anchor nuts. Components are mounted in the top cover either directly on the cover or on printed circuit boards which are mounted to the cover on standoffs. T/M signals enter and leave the assembly through five connectors in the top of the cover.

Figure 4.9-18 shows a view of the T/M assembly.

4.9.17 Mechanical Specifications

The following are the significant mechanical specifications of the complete system.

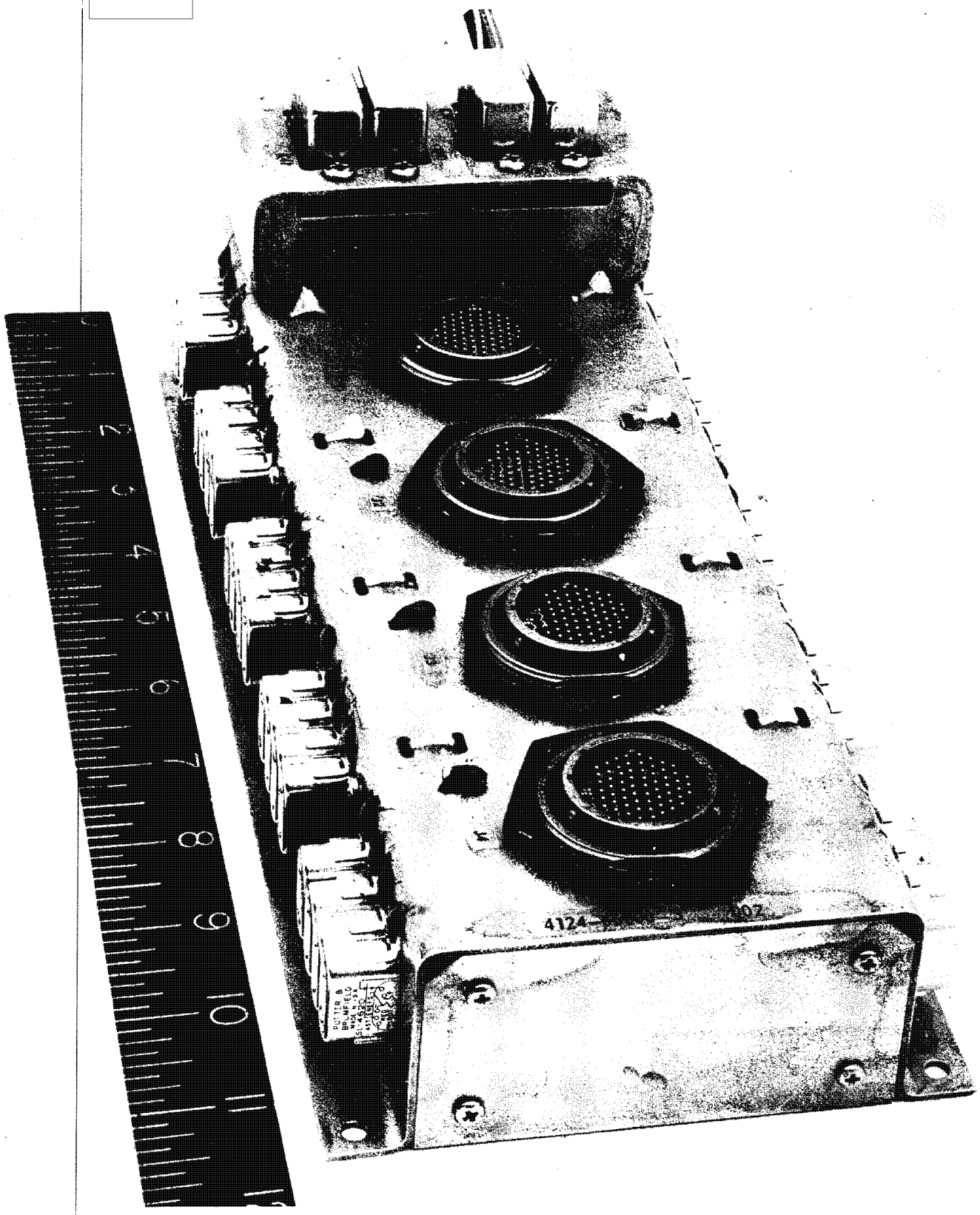

Figure 4.9-17 Relay Assembly

FIGURE 4.9-18. T/M ASSEMBLY

(To Be Published In Final Report)

4.9.17.1 Weight

To be supplied at a later date.

4.9.17.2 Center of Gravity

To be supplied at a later date.

4.9.17.3 Mounting Interface

The system mounts to the primary support structure with 8 type LS8758-5-t bolts. The mounting surface is flat to within .010 inches. The bolt pattern is as specified in the interface specification AA1654-3.

4.10 Thermal Design

4.10.1 Introduction

Thermal design of the system required that heat removal and addition be obtained by radiation coupling to the surrounding structure of the auxiliary rack. This requirement was predicated by the location of the system within the vehicle auxiliary rack and the electrical requirements for a low density, low conductivity RF barrier on the earth side of the system.

The temperature of any part of the system is therefore dependent upon an energy balance with the supporting structure immediately surrounding that part of the system. This temperature is modified to some extent by conduction into and across the base plate of the system. Temperature is also modified by the exterior surfaces of the system which are not radiatively coupled to the auxiliary rack structure or which do not require the low density, low conductivity barrier such as the outer

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surfaces of the channel support sections.

Reliability conditions require that the resulting thermal characteristics of the system be such that the average surrounds temperature of the equipment be approximately 75°F with maximum and minimum excrusions never failing outside the range of 0 F to 130 F. Actual equipment operating temperatures should be as close to the surrounds temperature as possible using reliable thermal design techniques (i.e. passive means). The equipment hot spot temperatures should in no event exceed the maximum reliability derated limits for the electrical components which create the hot spots.

The thermal design has achieved this goal, being aided by the extensive use of silicone transistors rather than the lower temperature rated germanium semiconductive devices. Completely passive thermal control is employed except for the extremely temperature critical current drivers and YIG oscillators. The active temperature control for these devices is accomplished by using a heater element and both a solid state controller and a mechanical thermostat safety device. This type of active control is highly reliable.

4.10.2 System Thermal Characteristics

4.10.2.1 Thermal Coatings

To achieve the desired thermal response of the system, appropriate thermal coatings are used. Figure 4.7-1 shows the utilization of these coatings on the system. The

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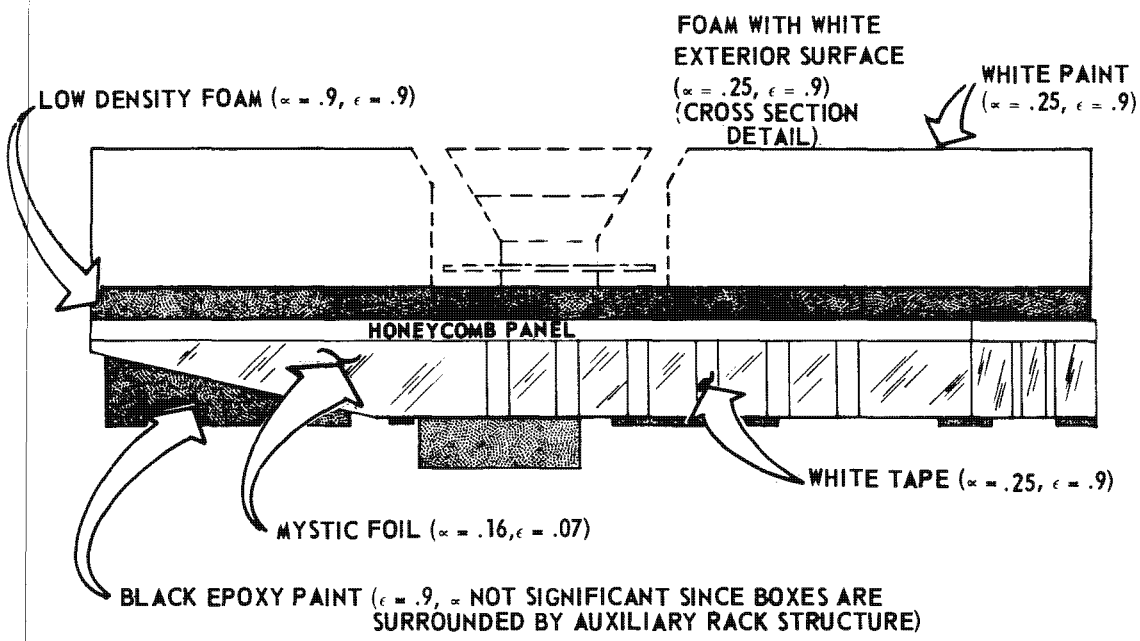

Figure 4.10-1. System Thermal Finishes On -Y Side

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coatings and their approximate purposes are given in the following paragraphs.

On the underside of the system, all main surfaces are covered with a black epoxy paint, Andrew Brown type A316. This paint with its high infrared emissivity ($\epsilon \approx .9$) assures maximum radiation coupling with the surfaces of the auxiliary rack which in turn have a high emissivity finish of Dow 17 over a magnesium base ($\epsilon \approx .7$). Around the edges of the system, on the exterior of the 3.65 inches wide aluminum support channels, a finish consisting of Mystic 7402 aluminum tape is applied. These surfaces do not contribute significantly to the overall thermal response of the system and are finished with a thermal coating that acts as an effective radiation barrier ($\epsilon \approx .06$).

Over the low emissivity surface on the -Y side of the system, type LAC 24-4224, color 101 (white), thermal tape is applied in sufficient quantity to cover 30% of the total exterior area on this side. This tape prevents this one area from becoming too warm during certain orbital conditions, a condition which could produce unwanted hot spots on the units of the system immediately behind the support channel on this side.

On the side of the system which faces the earth, the thermal finishes were chosen based on the need to maintain all antenna temperatures within narrow limits. The resulting finishes include a 8" thick layer of low density, flexible polyurethane foam which covers the major area of the front of the

honeycomb panel. A high emissivity ($\epsilon \approx .9$) low absorptivity ($\alpha \approx .25$) white paint is applied to all exposed phase horn surfaces.

4.10.2.2 Thermal Inertia of the System

Because the major mode of heat transfer is by radiation exchange with the surrounding walls, the quantity known as the "radiation time constant" is of great significance in determining the overall thermal characteristics of the system. This quantity is given by:

Where:

$$\tau = \frac{mc}{4(EA)_{EFF}\,\sigma\,T_o^3} \qquad 4.10\text{-}1$$

τ = Radiation Time Constant (Hours)

m = Total Mass of the System (Pounds)

c = Average Specific Heat of the System (BTU/LB - 0^oF)

$(EA)_{EFF}$ = Effective Overall Radiation Coupling With the Surrounds (FT^2)

T_o = Equilibrium temperature of the System which is generally an average of the separate equilibrium temperatures of the

various parts or the system under certain thermal loading conditions (degrees Rankine).

σ = Stephan-Boltzman's Constant

Equation 4.10.1 expresses the rate with which the total system will respond as the temperature of the surrounding surfaces change with time. It does not give the detailed transient response of individual units of the system nor of local hot spots within each unit. The use of this quantity is shown below:

$$\tau = \frac{mc}{4(EA)_{EFF}\sigma\ T_o^3} \qquad 4.10\text{-}2$$

The values of the quantities in the equation above are given by:

m = 200 lbs (the antenna weights are not included in this quantity)

c = 0.2 BTU/lb- F^o (Typical for an electronic assembly)

$(EA)_{EFF}$ = 15^2 (this quantity is determined primarily by the area which sees the auxiliary rack structure)

T_o = 660^oR

which gives for the radiation time constant.

$$\tau = \frac{(200)(0.2)}{(4)(15)(1.725 \times 10^{-9})(2.85 \times 10^{10})} \quad 4.10\text{-}3$$

$$= 1.36 \text{ Hours}$$

At an orbital altitude of 268 n.m. the orbital period is 95 minutes = 1.58 hours. The radiation time constant is thus the same order of magnitude as the orbital period. This means that the system will respond in a time period comparable to the orbital period. Thus even if the walls of the auxiliary rack cycle between two extremes during any one orbit, the thermal inertia of the system is sufficiently high that no appreciable temperature change will occur as a result of the cycling. The temperatures of the auxiliary rack walls are assumed to be at their orbital average temperatures in determining the thermal response of the system. Therefore, there is no requirement to perform a tedious transient analysis of each section of the auxiliary rack. A quasi-steady state analysis can be performed to determine only the average temperature of each surface for any given orbit (this average will of course change as the orbital thermal inputs slowly change with time).

4.10.3 System Thermal Analysis

4.10.3.1 Thermal Inputs

The auxiliary rack and the temperatures of separate sections of system are determined by a radiation balance between the total thermal inputs and the total radiating efficiency of the external surfaces to space. The thermal inputs include earth shine, albedo, direct solar radiation and average power dissipation

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within the auxiliary rack and the system. These inputs generally change with respect to the orbital sun angle (β angle) having a maximum value for a β angle of 90° (called "the twilight orbit") and a minimum for a β angle of 0° (called "the high noon orbit").

Analysis for these two conditions gives the upper and lower extremes for the temperature range of the system. The overall long-term, average temperature is essentially then given by the T average of these two extremes, i.e.,

$$\overline{T} = \sqrt[4]{(T_u^4 + T_L^4)/2} \qquad 4.10\text{-}4$$

Where:

$\overline{T}$ = Overall Time Average Temperature (degrees Rankine)

T_u = Upper bound of the system temperature range (degrees Rankine)

T_L = Lower bound of the system temperature range (degrees Rankine)

The average thermal inputs required to calculate the two temperature extremes are derived as follows.

(1) Earthshine: For a vehicle which retains a constant attitude with respect to the earth, the thermal input from

earthshine is essentially constant for all angles. The value of the input only depends upon the orientation of a particular surface with respect to the earth.

(2) Direct Solar: For a β of 90° the sun presents a constant input to one side of the orbiting vehicle (the -y side). The other side is in complete shadow. As β decreases to 0° the sun gradually moves to a position that illuminates the plus and minus z sides of the vehicle. However, in this condition the vehicle is exposed to the rays of the sun only 65% of each orbit.

The constant attitude with respect to the earth also causes the sun to seemingly precess around the vehicle from +Z to -Z during the daylight portion of the orbit. The average direct solar input for a β of 0° is thus obtained by taking the average projected area of each surface to the sun as it precesses around the vehicle, i.e.,

$$\overline{S} = \frac{S}{2\pi}\int_{\theta_1}^{\theta_2} \text{Cos}\ \theta p\ d\theta p \qquad 4.10\text{-}5$$

Where: $\overline{S}$ = Orbital average solar flux (BTU/Hr-FT^2)

θp = Angle between the normal of the surface being considered and the direction of the suns rays

θ_1, θ_2 = The value of p when the sun first strikes the surface being considered and when the sun's rays last strikes the surface every orbit.

Equation 4.10-4 can be used to calculate the average direct solar flux impinging on each surface. The equation must be used with caution if there are any perturbances which will partially block the sun's rays during certain positions of the vehicle. The Granary antenna is one such perturbance. (See Figure 4.10-2). This partial shadowing effect of such appendages must be carefully taken into account.

(3) Albedo: Solar energy reflected off the earth's surface is also strongly dependent on β angle. The average albedo input is a maximum for $\beta = 0^0$ and a minimum for $\beta = 90^0$.

4.10.3.2 System Analysis

Using the average thermal inputs, as stated, a

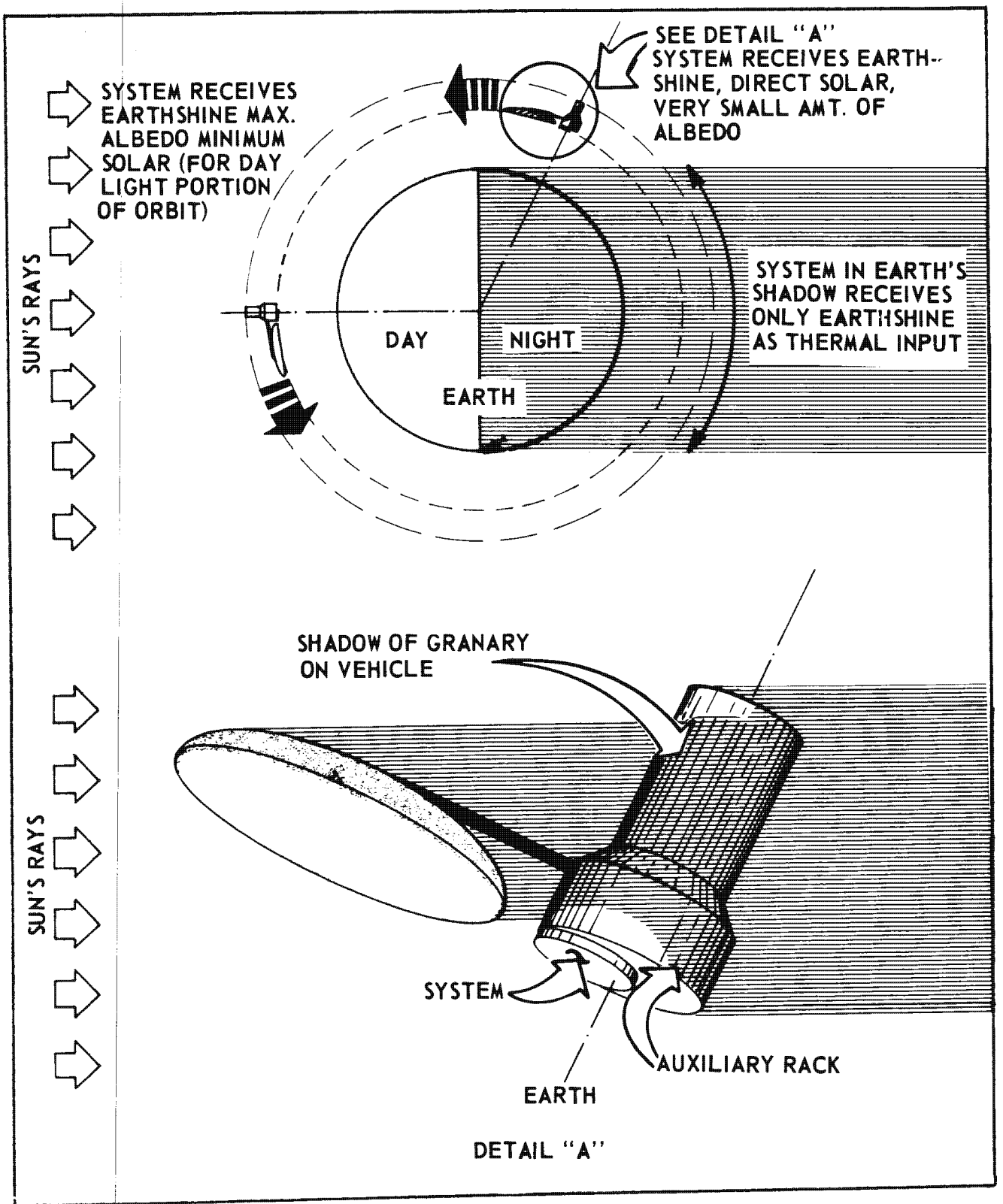

Figure 4.10-2. High Noon Orbit Schematic

steady-state, energy-balance equation can be written for each main surface of the system-auxiliary rack combination. The equation for one such surface is given by:

4.10-6

$$\left[\sum_n G(i,n) + (\epsilon_i A_i)sp\right]\sigma \overline{T}_i^4 - \sum G(i,n)\,\sigma \overline{T}_n^4 =$$

$$\overline{Q}_i + \alpha_i \overline{S}_i + \alpha_i \overline{\mu}_i + \epsilon_i \overline{\rho}_i$$

Where:

$G(i,n)$ = Radiation coupling between surfaces i and n (FT^2)

$(EiAi)sp$ = Radiation coupling from surface i to space (FT^2)

$\overline{T}_i$ = Orbital average temperature of surface i (degrees Rankine)

$\overline{T}_n$ = Orbital average temperature of surface n (degrees Rankine)

σ = Stephan-Boltzman Constant

$\overline{Q}i$ = Average electrical power dissipated on surface i (BTU/Hr)

α_i = Solar absorbtivity of surface i

ϵ_i = Infrared emmissivity of surface i

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$\overline{S}_i$ = Orbital average direct solar flux onto surface i ($BTU/Hr-FT^2$)

μ_i = Orbital average albede flux onto surface i ($BTU/Hr-FT^2$)

ρ_i = Orbital average earthshive flux onto surface i ($BTU/Hr-FT^2$)

For the system analysis, ten surfaces are chosen as significant thermal surfaces and are shown schematically in Figure 4.10-3. The three surfaces on the system are essentially dummy surfaces. The selected surfaces are picked merely to facilitate obtaining the average temperatures of the auxiliary rack surfaces. After these auxiliary rack temperatures are obtained, the system is broken down into its separate units, which in general have less surface area than shown in Figure 4.10-3.

Thermal analysis of each unit is then obtained using the derived auxiliary rack average temperatures as radiation surrounds temperature. This analysis is described in detail in paragraph 4.10.4.

For the system analysis the values of Q_i, S_i, μ_i and ρ_i are obtained as discussed in 4.10.3.1. Radiation coupling factors are obtained between surfaces using the tabulated data from the NASA Technical Note 2836, "Radiant-Interchange Configuration Factors" by D. C. Hamilton and W. R. Morgan and the use

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of a high finish on all interior surfaces. Values for ϵ_i and α_i are dependent upon the exterior point pattern of each section of the system and the auxiliary rack structure.

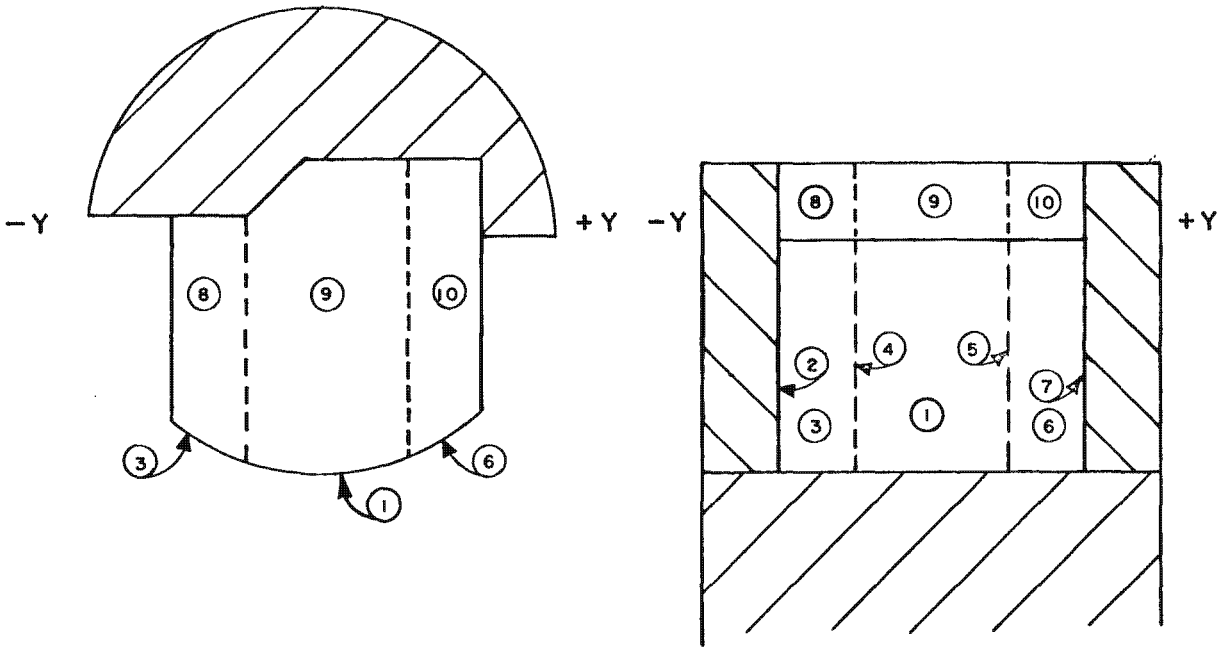

Figure 4.10-3. Payload-PV Node Numbers

The values of the upper and lower band for the temperature range of each major section of the auxiliary rack as determined by the analysis is shown in Table 4.10-1. The values are believed to be conservative and generally agree with a similar preliminary analysis performed by LMSC. The temperature ranges fall within the desired limits.

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TABLE 4.10-1 RESULTS OF SYSTEM ANALYSIS

Rack Section	Average Temperature = 90°	= 0°
-Y Bay	130°F	20°F
Center Bay	100°F	20°F
+Y Bay	70°F	20°F

4.10.4 Individual Hot Spot Analysis

4.10.4.1 Introduction

The type of analysis in Section 4.10.3 is adequate to obtain the overall thermal response of the system. However, in determining the magnitude of local hot spots within individual units a more careful analysis generally has to be performed. These hot spots are caused by very local power dissipation and can change rapidly with time, even though the housing of the unit and the system as a whole is changing much more slowly.

Average power dissipation cannot be used to accurately predict the maximum temperatures of these points; using average power could result in errors of over 50 F in some instances. Steady state analysis would also be improved in some instances. In these cases, the duty cycle of the unit is critical as the hot spots never reach a steady state level in the normal 30-out-of-95-minute duty cycle. For these reasons, the analysis of individual hot spots is performed with one basic philosophy. If a steady state temperature analysis of a hot spot, using maximum power dissipation, resulted in a temperature

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which is within acceptable bounds, this temperature is given as the maximum worst case for that hot spot. This maximum temperature may not be obtained due to the Finite thermal inertia of the hot spot components in actual operation. If the steady state analysis indicated a temperature which was unacceptable, the hot spot was examined in close detail, with the actual transient response calculated. This method is much more tedious and time consuming than a steady state method, and was limited as much as was practical. In one case, a combination of the two types was utilized.

The resulting maximum temperature predictions are conservative in all instances and a tolerance is given for each point, indicating the range in which the actual maximum operational temperatures are expected to be.

4.10.4.2 Analysis of the Data Handler and Recognizer Rack Hot Spots

The Data Handler and Recognizer Rack are of similar construction and power distribution and dissipation. The Recognizer Rack is located in the section of the system which looks down into the -Y bay of the auxiliary rack. It will thus see the worst thermal environment (Table 4.10-1). An analysis for this unit will then suffice for both. The analysis was performed on a steady state basis due to the nature of these units as described in the following paragraphs.

The Recognizer Rack is composed of an aluminum

housing painted black on all exterior surfaces and with a low emissivity alodine finish on interior surfaces. Within the housing, 24 printed circuit boards are mounted in pairs to the sides of an .016-inch thick aluminum plate. The aluminum plate is attached to the housing by spring clips on either end of the plate. Each printed circuit board has an even distribution of flat packs which in general dissipate power uniformally.

The total power consumption of the unit is 15 watts during the normal duty cycle of the system. Each pair of circuit boards dissipates 1.5 watts, maximum. Pairs of circuit boards are stacked at intervals of approximately .5 inches. Figure 4.10-4 illustrates the unit with the top cover off and some of the printed circuit boards removed.

Thermal analysis was conducted on one of the center cards, at which location of the hottest point will be achieved near the center of the card. Because of the light weight of the card pairs (.04 pounds), the thermal inertia of the card will be small; a steady state analysis will closely approximate the actual maximum temperature achieved on the card. The following conservative assumptions were used in the analysis.

1) There is no heat exchange with the aluminum honeycomb base plate.
2) This is no radiation exchange between adjacent card pairs.
3) Heat will be removed primarily

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by conductor from each card pair into the spring clips and thus into the side walls of the housing. From these walls the heat will be radi-

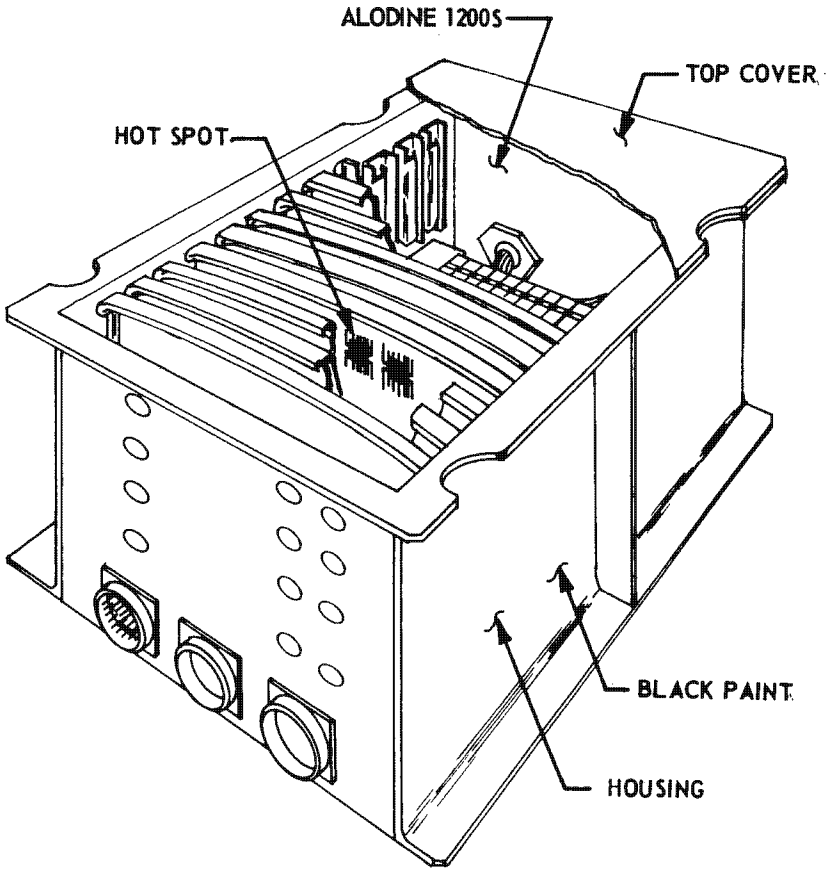

Figure 4.10-4 Data Handler No. 2 Thermal Layout

The temperature rise between the surrounds and the center of the card can be broken up into three general increases.

(1) With uniform power dissipation over the cards, the heat flow will be essentially one dimensional from the interior

of the cards to the location of the spring clips along the two edges. The temperature rise from the edge to the center of the card can then be found from the one-dimensional Fourier equation:

$$\frac{d^2T}{dX^2} = -Q/KA \qquad 4.10\text{-}7$$

Where:

T = Temperature (degrees Rankine)

X = Distance measured from center of card (FT)

Q = Power dissipation per unit length (BTU/Hr-FT)

K = Conductivity of Material (BTU/Hr-FT-^{o}F)

A = Conduction cross sectional area (FT^2)

The solution is:

$$T = \frac{Q}{KA}\frac{X}{2} + \left(T + \frac{Q}{KA}\frac{L}{4}\right)^2 \qquad 4.10\text{-}8$$

Where T_o is the temperature at the edge of the card, and L is the total width of the card between the spring clips. The maximum temperature is at the center, where X = 0, and its magnitude above the temperatures at the edge is:

$$T - T_o = \frac{Q}{KA}\left(\frac{L}{4}\right)^2$$

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For the Recognizer Cards:

Q = .2 watts/inch = 8.2 BTU/Hr-FT

K = 99 BTU/Hr-FT-OF (This is the conductivity of the aluminum plate. The circuit boards contribute very little to the conduction transfer in this direction)

A = .0004 FT^2 (The cross sectional area of the aluminum plate in the direction of heat flow)

L = .5 FT

Giving a maximum gradient from the edge of the card to the center of:

$T - To = 12.7^{o}F$ 4.10-9

The gradient from the front surface through the printed circuit board is only approximately $.1^{o}F$ due to the low power density on the board; therefore, 4.10-9 closely represents the maximum gradient from the edge of the aluminum plate to the center of the front surface of the printed circuit boards.

(2) The second gradient is that across the surface contact between the spring clip and the aluminum slide plate.

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There is approximately 1 in^2 of contact area on each spring clip so the thermal loading on each clip is .625 watts/inch = 31 $BTU/Hr\text{-}FT^2$. However, the contact pressure is not well defined for these surfaces and, as a result, the thermal contact conductance may be very low. To insure a conservative calculation, a low thermal conductance value of 2.46 BTU/Hr-FT - °F was chosen. Under these conditions, the gradient between the aluminum sliding surface and the spring clip is:

$$T = 31/2.46 = 12.5°F \qquad 4.10\text{-}10$$

(3) The third and final significant gradient is that from the housing of the unit to the surrounding surfaces (assumed to be at 130°F).

Steady state methods were used in the preceeding parts of the analysis. In determining the housing temperature, an averaging method was considered to be more accurate for the normal duty cycle of 30 minutes out of 95 minutes. Average power dissipation of the Recognizer Rack is 4.7 watts. The area of the two sides of the housing is 94 in^2 and the view factor to the surrounding surfaces is approximately .50. This results in a temperature gradient between the housing and the surrounds of:

$$T_H - T_S = 30.5°F \qquad 4.10\text{-}11$$

Adding 4.10-9, 4.10-10 and 4.10-11 indicates the overall maximum gradient between the center of a card and the surrounds. The maximum temperature is, with a surrounds of 130°F.

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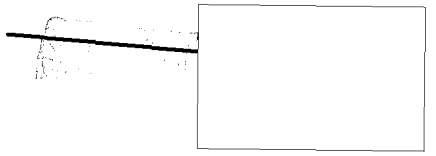

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T_{MAX} = 185.2°F ± 20°F 4.10-12

This temperature is well below the maximum rated temperature of the flat packs on the printed circuit cards.

4.10.4.4 Hot Spot Analysis of the Recognizer Memory, Buffer Storage and SWI

The internal configuration of the Recognizer Memory is similar to both the Buffer Storage and the SWI. A detailed description of the analysis of this one unit will then suffice for all three.

Figure 4.10-5 illustrates the layout of the Recognizer Memory. The memory consists of a ferrite memory stack in the approximate center of the unit with two sense amplifier printed circuit boards at the top and bottom of the stack. Between each sense amplifier board and the cover of the unit is a larger printed circuit board with additional electronic circuitry.

The total power dissipation of this unit (4.5 watts) is divided into 1.05 watts maximum, for each sense amplifier board and approximately 1.25 watts for each larger board. The sense amplifiers are 3" X 3", resulting in a power density of 0.11 watt/inch^2. The larger boards are 6" X 11" giving a power density of .019 watts/inch^2.

The only significant mode of heat transfer is by radiation. The separate boards are tied together structurally with four steel screws located at each corner of the sense amplifier board, but the size of the screw and the low conductivity

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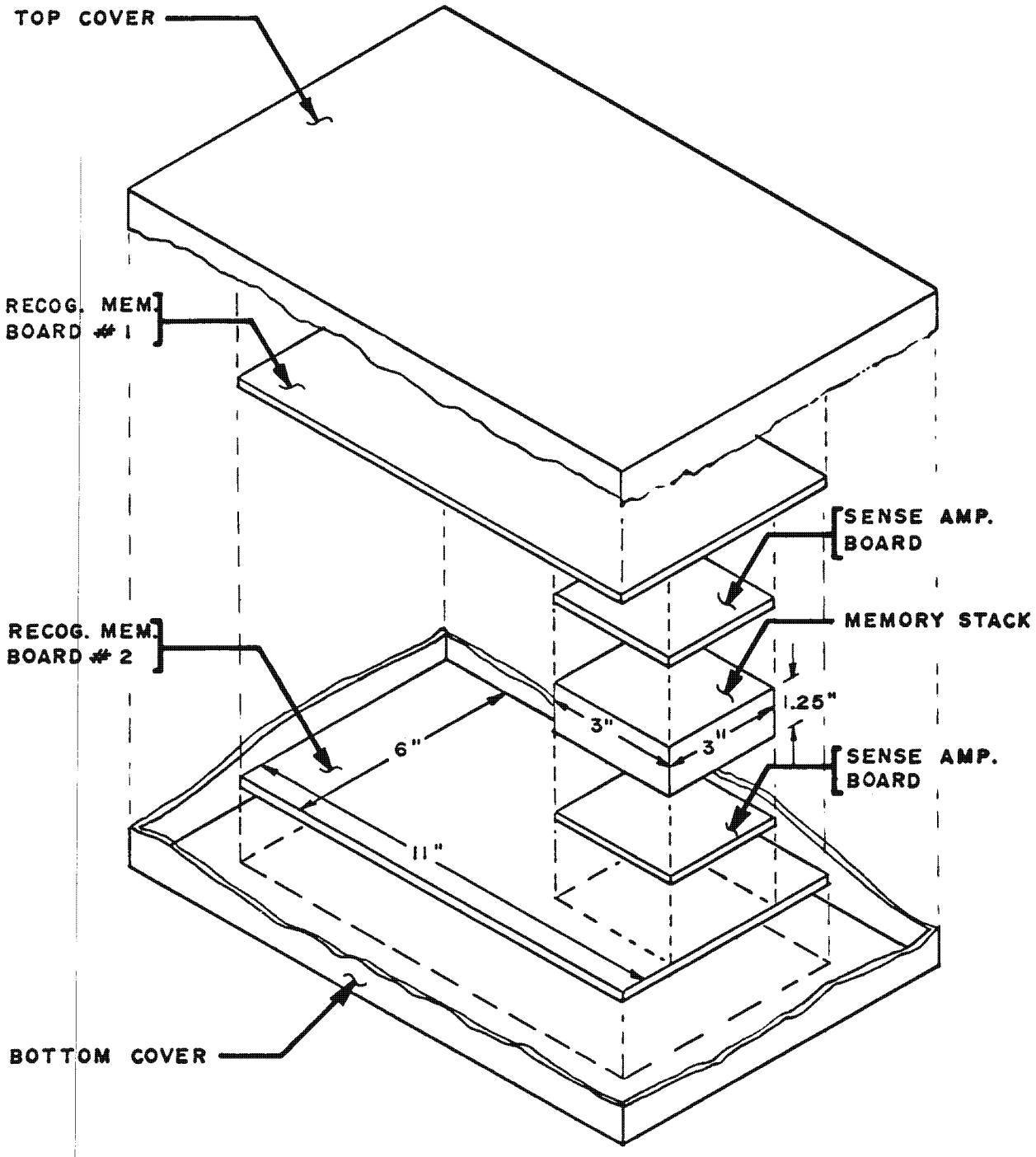

Figure 4.10-5. Recognizer Memory Thermal Layout

material reduce the conduction transfer to an insignificant level in comparison with radiation. Conduction transfer will therefore be neglected.

A steady state heat transfer equation can be written for each separate part. Let T_1, T_2, T_3, T_4, T_5, and T_s represent the temperature of the top sense amplifier board, the bottom sense amplifier board, and memory stack, the top large board, the bottom large board and the radiation surrounds, respectively. The equation for the top sense amplifier board is written as:

$$F_{12}\epsilon_{12}(\sigma T_1^4 - \sigma T_2^4) + F_{13}\epsilon_{13}(\sigma T_1^4 - \sigma T_3^4) + F_{14}\epsilon_{14}(\sigma T_1^4 - \sigma T_4^4) + F_{15}\epsilon_{15}(\sigma T_1^4 - \sigma T_5^4) + F_{1s}\epsilon_{1s}(\sigma T_1^4 - \sigma T_s^4) = Q_1 \qquad 4.10\text{-}13$$

Where:

F_{1n} = configuration factor between body 1 and body n

ϵ_{1n} = emissivity factor between body 1 and body n

σ = Stephan-Boltzmann's constant

Q_1 = internal power dissipation of body 1

It should be noted that the cover does not enter into the calculations directly, but is represented by the F_{1s} ϵ_{1s} term. In this term, the effect of the cover as a radiation barrier is included. Cover temperature is not considered important since the orbital thermal telemetry points for these units are all at internal points. The configuration factors between

bodies were generally obtained from Hamilton and Morgan and the emissivity factors were generally assumed to be ln l n due to the large surface emissivities. The cover is painted black on both sides.

A similar equation exists for each body, resulting in 5 equations and 5 unknowns (T_s is assumed from Table 4.10-1 to be 130°F). Solving this set of equations produced the following maximum orbital temperatures:

$$T_1 = 150^\circ \pm 10^\circ F \qquad 4.10\text{-}14$$
$$T_2 = 170^\circ \pm 20^\circ F$$
$$T_3 = 150^\circ \pm 10^\circ F$$
$$T_4 = 145^\circ \pm 10^\circ F$$
$$T_5 = 175^\circ \pm 20^\circ F$$

A wider tolerance is placed upon T and T because of the assumption of no exchange with the honeycomb baseplate. In reality there will be some thermal exchange and it is expected that these two temperatures will more probably be in the lower tolerance band (i.e., between 150°F and 170°F for T_2). All of these temperatures represent average board temperatures.

The individual integrated circuits on the various boards are rated for 257°F (125°C) and only dissipate a maximum of 0.15 watts each. No significant gradient can exist between the integrated circuits and the epoxy boards; therefore, the analysis indicates an adequate thermal design. Similar temperatures are expected in the Buffer Storage. In the SWI, temperatures

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will generally be 30 F lower due to the less severe surrounds temperature (T_S = 100°F).

4.10.4.5 Hot Spot Analysis of the IF Deck

The IF Deck consists of two common housings for several individual chassis, generally referred to as IF phase channels. The total power of 40.6 watts is evenly distributed among these individual chassis with a maximum of 3.94 watts in one channel. The channel itself consists of a chassis which is machined from an aluminum bar to produce an "egg crate" configuration with a common mounting plate and several compartments, each isolated from the other for RFI shielding. Into each of these compartments a "cordwood" module is placed. The cordwood module consists of electronic components mounted between two small epoxy printed circuit boards and protected with a dip coating of Humiseal. Figure 4.10-6 shows the general arrangement of one of these channels.

It has been determined from past experience with this type of unit that the hot spot occurs on a type 2N1492 transistor which is located in several of the cordwood modules.

The transistor dissipates only 0.04 watts but the method of mounting results in a high thermal resistance path between the case of the transistor and the chassis. The thermal conduction path to the chassis consists of 3 Kovar leads of 0.00096 in cross section, approximately 0.2" long, and having a conductivity of 0.208 watts/in/°F. This produces a conduction

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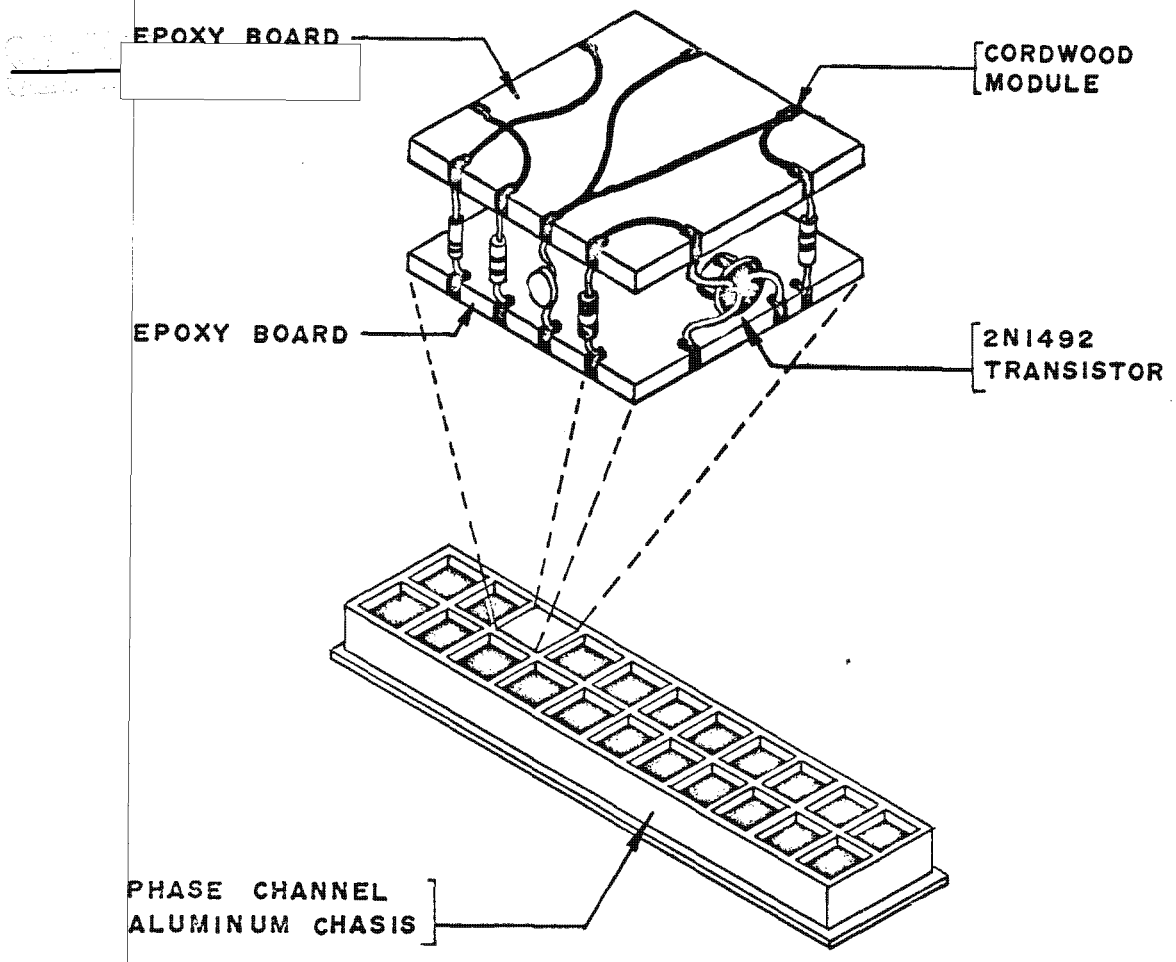

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Figure 4.10-6. IF Phase Channel Thermal Layout

coupling with the chassis (the printed circuit boards are generally in good contact with the chassis and thus, at essentially the same temperature) of 0.001 watts/ F. The transistor case also has a total area of 0.35 in^2 which is gold plated. If the gold plate were the only finish on the case then the low emissivity of the plating would create a worst case radiation coupling to the chassis of only 0.01 in^2. However, the Humiseal dip coating of each cordwood module can deposit a layer of high emissivity Humiseal on the case, in which event the radiation

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coupling would be increased to approximately 0.31 in^2. Both situations were analyzed to determine the possible spread in temperature due to an incomplete coating of Humiseal on the transistor case.

In the analysis, the chassis is assumed to be at an average temperature determined by the radiation coupling of the chassis to the surrounds and the orbital average power dissipation of 1.25 watts. The radiation coupling is determined by the top surface of a chassis and is equal to 26.5 in^2. This gives an average chassis temperature (T_c) above surrounds (T_s) of $T_c - T_s$ 21°F. The chassis temperature, with a maximum surrounds temperature of 100°F (the center bay) is then 121°F.

The hot-spot temperature of the transistor case is calculated assuming that a steady state condition exists between the transistor case temperature (T_{tc}) and the chassis average temperature. The transistor case temperature is determined by either the minimum coupling condition:

$$0.01\ (\sigma T_{tc}^4 - \sigma T_c^4) + 0.001\ (T_{tc} - T_c) = 0.04 \text{ watts} \qquad 4.10\text{-}15$$

or the maximum radiation coupling condition:

$$0.31\ (\sigma T_{tc}^4 - \sigma T_c^4) + 0.001\ (T_{tc} - T_c) = 0.04 \text{ watts} \qquad 4.10\text{-}16$$

which results in a maximum transistor case temperature of:

$$142^\circ F \leq T_{tc} \leq 161^\circ F \qquad 4.10\text{-}17$$

The transistor is rated at 302°F (150°C) and thus is well within limits.

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4.10.4.6 Hot Spot Analysis of the Power Supply

The power supply weighs approximately 12.5 pounds and has 308 in^2 total surface area (excluding the mounting surface area). With a power dissipation of 103 watts during the Readin and Calibration operations, this represents a power density of 0.33 watt/in . A steady state analysis would result in an average orbital housing temperature in excess of 212°F. Some components within the power supply have temperature limits of 257°F while others may operate above 300°F. For these reasons, the components with highest thermal ratings and dissipations were separated from the components having reduced temperature limits, and allowed to operate at slightly higher temperatures. These higher rated components consist of 4 silicon power transistors, each dissipating 5 watts, maximum; and a large power transformer, dissipating 20 watts, maximum. These components are required to be in close proximity to each other to minimize lead lengths.

Figure 4.10-7 depicts the general layout of the power supply showing how separation was accomplished. Most of the components, including the critical items, are evenly distributed throughout the housing of the power supply.

The top cover of the unit forms a radiation heat sink plate. The power transistors are mounted on the approximate center of the plate. The plate is machined from aluminum and is 0.1" thick to minimize the gradients that will exist

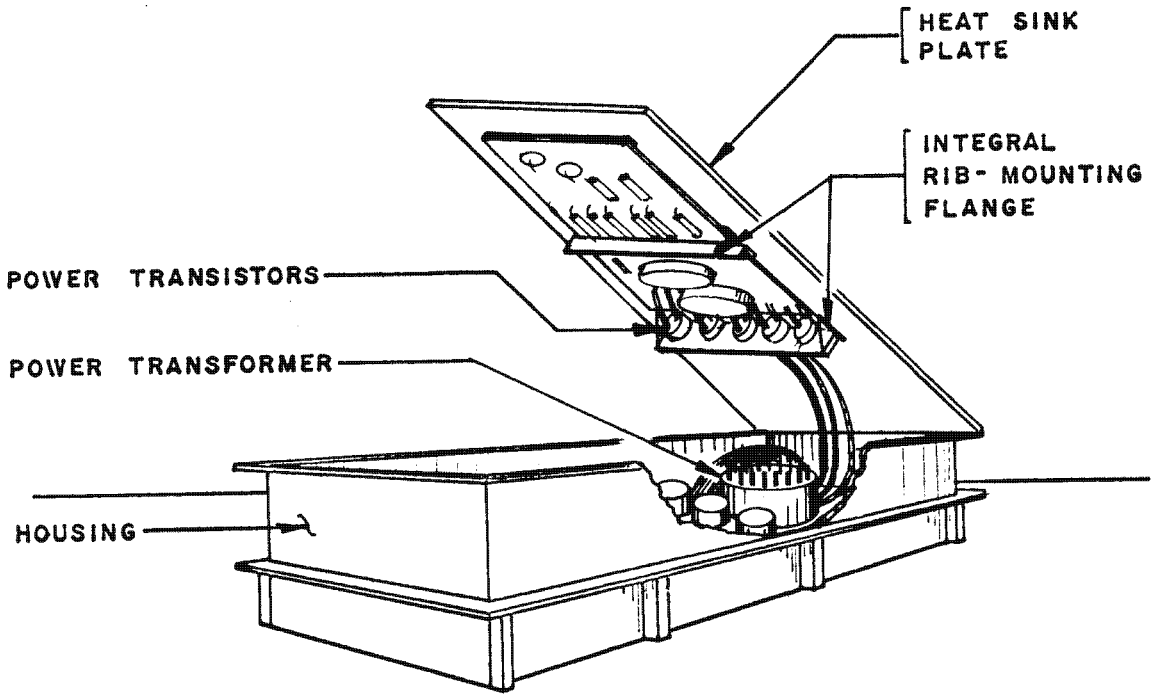

Figure 4.10-7. Power Supply Thermal Layout

from the power dissipating components to the extreme ends of the plate. The mounting web of the transistors is an intimate machined part of the plate to also eliminate gradients. The plate and associated components have a total radiating area of 98 in^2 to the surrounds, weighs 3 pounds, and dissipates 45 watts, chiefly at the power transistor locations.

To further enhance the thermal response of the power supply, the location of the unit in the +Y bay was carefully selected. This location places the unit into a surrounds that has the minimum temperatures during the worst case orbital conditions (See Table 4.10-1). The maximum orbital surrounds temperature in this bay is only 70°F, which aids considerably in maintaining the power supply within reasonable temperature limits.

Transient analysis of the average housing temperature and the average temperature of the heat sink plate was performed. The internal gradients within the housing and plate are calculated using thermodynamic reasoning based upon the thickness of the conduction webs and the local concentration of power.

In the analysis the following assumptions are made:

(a) Power is on a maximum of 30 minutes of the 95 minutes orbital period.

(b) There is no conduction exchange with the aluminum honeycomb baseplate.

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(c) There is little conduction or radiation exchange between the main housing and the heat sink plate.

Assumption (b) is the same assumption used in the analysis of the other units. In the power supply analysis it may seem overly conservative. An estimate was made of the power that could be conducted into the honeycomb face sheet and then radiated from the face-sheet to the surrounds. The analysis indicated that due to the thin face- sheets, only about a one-inch strip of face sheet around the lower edge of the unit would be effective in removing heat by conduction and radiation. This corresponds to about 6 watts of power or only 5.8% of the total power dissipation.

Assumption (c) was based on the belief, before the analysis was performed, that the final, average temperature of the housing and the top heat sink plate would be approximately the same, in which event there would be no exchange due to the isothermal condition. The subsequent analysis essentially confirmed this assumption.

Using these assumptions, transient analysis was performed on the two sections of the power supply. The analysis involved solving the two temperature-time equations:

Radiation Heating Equation

$$t/\tau_H + C_1 = 2\left[\tanh^{-1}\frac{T}{T_H} + \tan^{-1}\frac{T}{T_H}\right] \qquad 4.10\text{-}18$$

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Radiation Cooling Equation

$$t/\tau_c + C_2 = 2\left[\coth \frac{T}{T_L} - \cot \frac{T}{T_L}\right] \qquad 4.10\text{-}19$$

Where:

T	=	temperature
t	=	time
τ_H	=	radiation heating time constant = $mc/4\epsilon A\sigma T_H^3$
τ_c	=	radiation cooling time constant = $mc/4\epsilon A\sigma T_L^3$
T_H	=	maximum temperature which unit would reach if power (Q) were on continuously ($\sigma T_H^4 = Q/\epsilon A$)
T_L	=	minimum temperature which unit would reach if power were to be off continuously (T_L would then be the radiation surrounds temperature)
C_1, C_2	=	integration constants depending upon the initial conditions ($t = 0$, $T = T_1$) and ($t = 30$ min, $T = T_2$)

From the mass, available radiating area, surface finish ($\epsilon = 0.9$), and power dissipation of the main housing and the heat sink

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plate. The greater mass of the housing (9.5 lbs as opposed to 3 lbs) causes slower transient response. The possibility of gradients within the housing will be less, due to a more even distribution of power.

Temperature-time equations were solved using an inerative process. First, one assumes an initial temperature T_1 and obtains a value for C_1. Using this value of C , the temperature when t = 30 minutes can be calculated. This temperature is then taken as the initial temperature during the cooling cycle and C_2 determined. The final temperature after 65 minutes of cooling can then be determined. If final temperature is equal to the originally assumed initial temperature T_1, the solution is complete. If not, one takes the final temperature as a new initial temperature and performs another cycle of calculations. Usually two or three cycles results in a closed solution.

Figure 4.10-8 shows the results of this analysis with the expected gradients that will exist in the top heat sink plate. The transient analysis results in temperatures well under the derated limits of the separate components.

4.10.3.5 Thermal Analysis of the LO Control Box

In the design of the LO control box there were three thermal constraints applied to insure that the LO controls (including the high and low band YIG oscillators and current drivers) would operate within electrical specifications.

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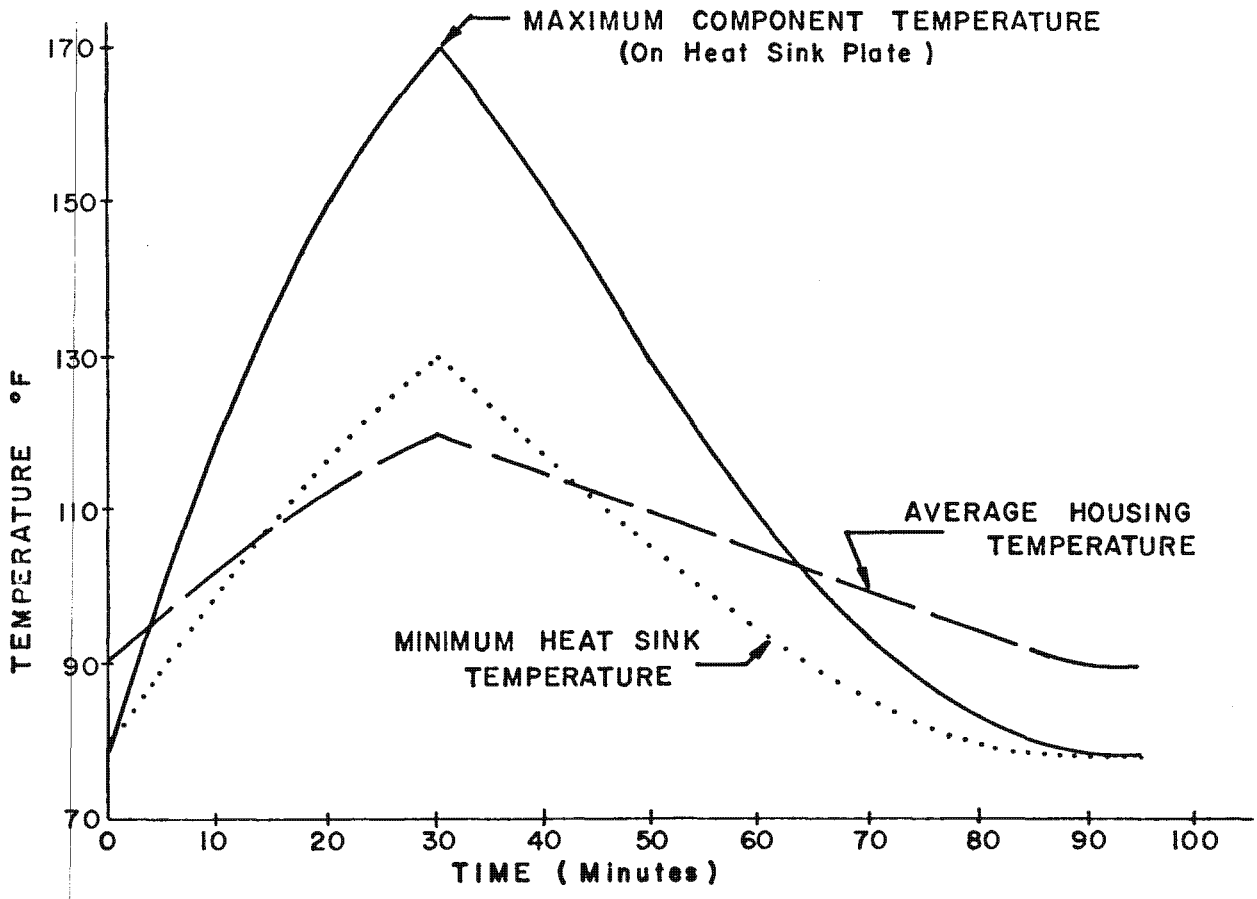

Figure 4.10-8. Power Supply Transient Response - Worst Case

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Thes traints were:

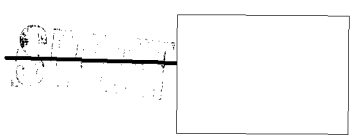
(a) Temperatures of critical components should not exceed 185°F

(b) Temperatures of critical components should not fall below 120°F

(c) During the on-cycle of the current drivers a critical power resistor should not change temperatures at a rate exceeding ± .72°F/min.

During operation, the critical components of the LO controls have the worst case power profile as shown in Figure 4.10-9. Maintaining the desired minimum temperature of 120°F during all orbital (T_{min} = 20°F) and test (T_{min} =-30°F) conditions, required isolating the components to some extent from the mounting surface of the honeycomb. Otherwise, it would take an excessive amount of heater power to maintain a worst case 150°F gradient between the components and the base plate when the components are off.

Thermal isolation means, however, that during power cycling the components will act in a purely transient response mode which will depend only on the thermal inertia of the components and the structure to which they are mounted. The temperature response during any period will then be given by $\frac{T}{t} = Q/mc_p$ where Q is the power dissipation and mc_p is the thermal inertia of the components-mounting structure combination.



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It is not possible to smooth out this transient response by cycling a heater out of phase with the component power.

From Figure 13, Q_{max} = 4.25 watts and $\frac{T}{t}$ = .72°F/min thus mc_p = 4.25/.72 = 5.9 watts-min/°F

= .335 BTU/°F

The YIG oscillators weigh approximately 2 pounds, but they are composed mainly of material with a low specific heat (iron with a C_p of 0.11 BTU/lb-°F) giving a thermal inertia of 0.22 BTU/°F. Thus an additional 0.11 BTU/°F is still required. This additional inertia is supplied by the mounting plate which is made of copper, with a specific heat of 0.10 and weight of 1.13 pounds.

Copper is used instead of aluminum, which has a C_p of 0.22, because of the required configuration of this plate. To hold components, other than the critical components, the plate must be at least 5" X 5". The critical components, from the transient standpoint, are two power transistors which create a highly local concentration of power on the plate. In order to be able to use the total mass of the plate, the power must be readily distributed into all corners of the plate, i.e., a material with a high thermal conductivity must be used. Copper, with a thermal conductivity almost three times aluminum, was selected as the better material.

With the thermal inertia of the plate and components combination, the orbital response of the critical components will

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oscillate ±4.5°F about an average which is determined by the average orbital power dissipation of the components within the oven (Figure 4.10-9), the value of the thermal resistance from the copper plate to the surrounds, and the magnitude of available controllable heater power within the oven.

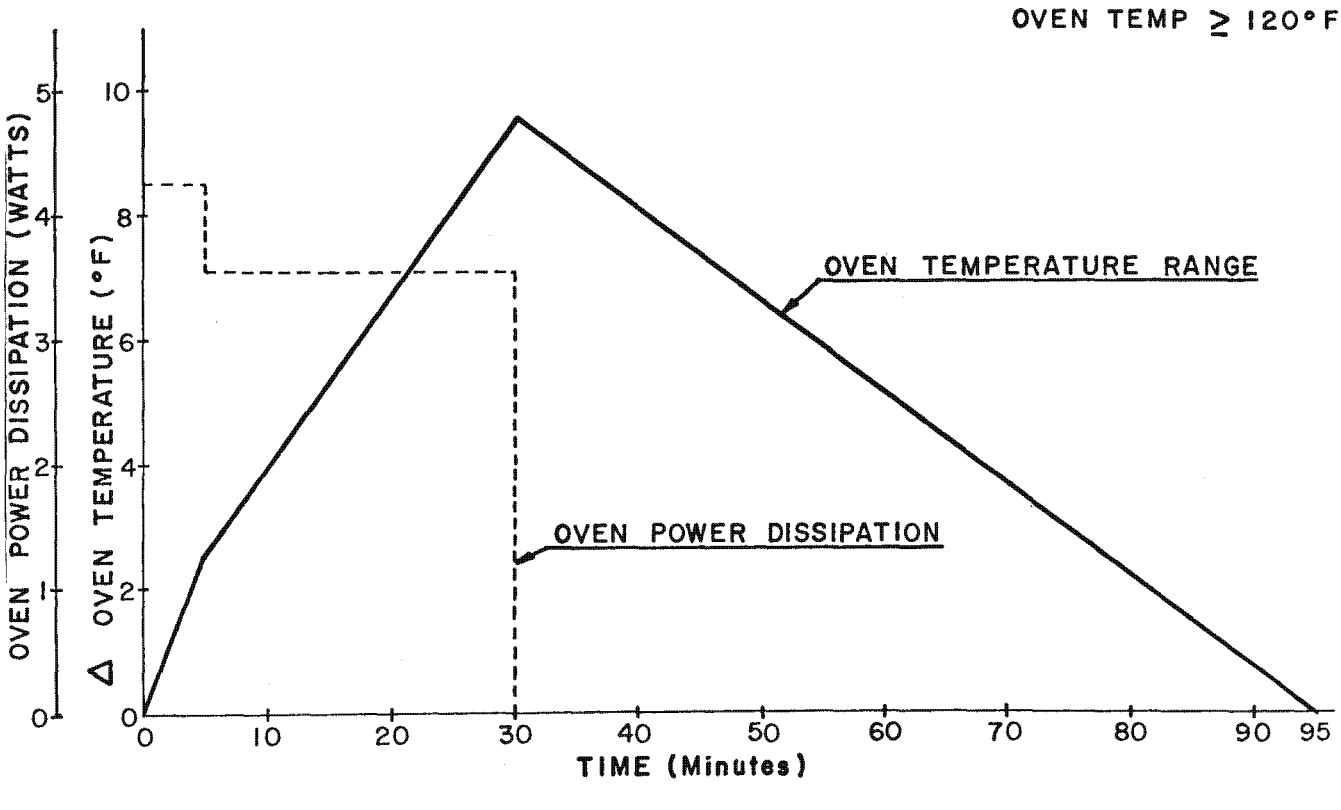

Figure 4.10-9 LO Oven Transient Temperature Response

Figure 4.10-9 shows the orbital average power of the components within the oven to be 1.25 watts. One possible test condition will involve a surrounds of 160°F. In order not to exceed a maximum of 185°F within the oven, a conductive thermal resistance of 15°F/1.25 watts = 12°F/watt is required (with a ±4.5°F transient response this gives a maximum temperature of

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179.5°F). During the worst possible cold test, the surrounds will be at -30 F. A total power requirement of (120°+ 30°)/12°F/watt = 12.5 watts must be supplied to maintain component temperature above 120 F. Since this condition must exist even when the components themselves are not dissipating power (for example, during extended periods in which the total system may be inactivated), the additional power must be supplied by heating elements. In order that these heating elements not operate when the components are above 120°F due to high base plate temperatures, a proportional controller is employed which de-activates the heaters once the internal oven temperature is above 120°F.

The final form of the LO control oven is shown in Figure 4.10-10. The oven consists of an outer shell of magnesium

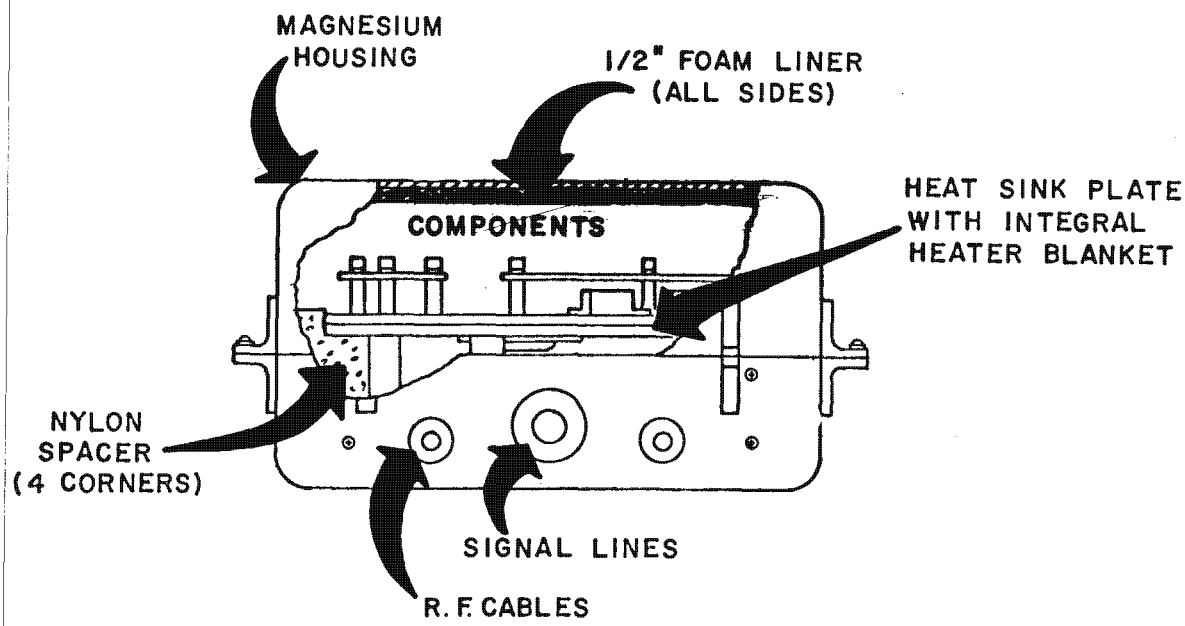

Figure 4.10-10. LO Oven Thermal Layout

an insulating layer $\frac{1}{2}$" thick of low density polyurethane foam ($\rho \approx 2$ lb/ft3, k .01 BTU/hr-ft-^{o}F), insulating structural stand-offs made of nylon, and the heat sink plate with four heater blankets mounted in small cutouts on the plate. The response of the heater-oven combination versus base plate temperature is shown in Figure 4.10-11.

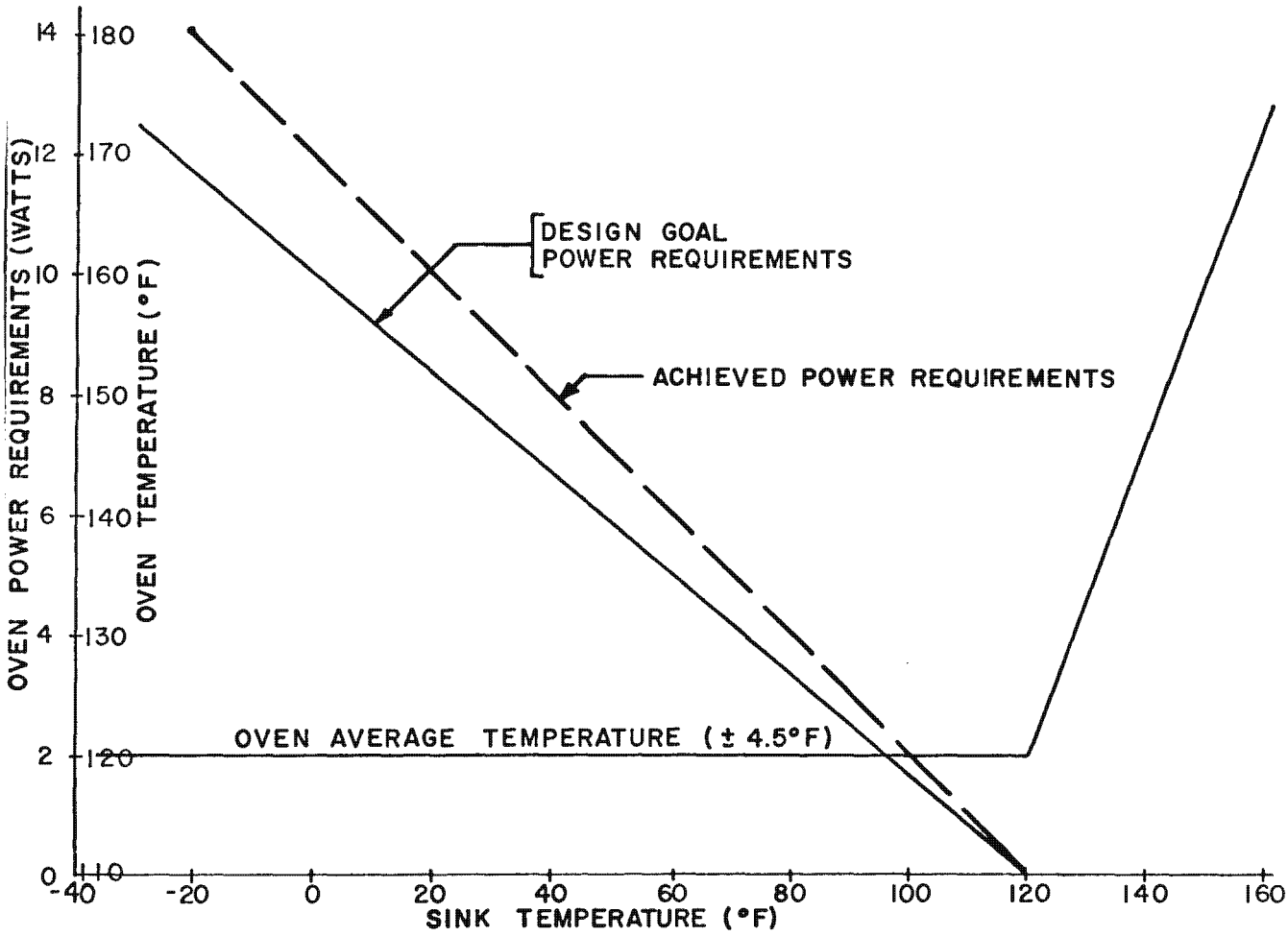

Figure 4.10-11. LO Oven Power Requirements

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4.11 Electromagnetic Interference Control

4.11.1 Introduction

The objectives of the Electromagnetic Interference Control measures applied to the Reaper System are to insure that the various subsystems of the system are mutually compatible and that the system will be compatible with the power line requirements as stated in the official interface document. A further objective is generally to reduce the susceptibility of the system to outside EMI and to reduce the EMI radiated and conducted from the system.

To achieve these objectives, the interference control plan, LTVE Specification 52000-R420, was originated early in the program and these basic requirements were implemented during the design phase. Additionally, military specifications MIL-I-618D, MIL-E-6051C and MIL-B-5087 were utilized as design guides.

4.11.2 Purpose

The purpose of this section is to briefly summarize the electromagnetic interference control measures that were applied to the system.

4.11.3 General EMI Control Concepts

Interference control and compatibility techniques were applied in the design of each subsystem of the system. Basic interference control techniques of grounding, bonding, shielding and filtering were used.

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4.11.3.1 Grounding Philosophy - The basic grounding philosophy presented herein evolved from the following analysis of the subsystem signal and secondary power interconnection requirements.

4.11.3.1.1 Shield Grounds - Since binary and RF data is interconnected between each of the units and because the characteristic nature and frequency spectrum of this data contains RF interference frequency components above 150 kc, the interconnecting signal lead shields were grounded to the subsystem equipment cases at each end. Because the interconnecting shield would provide a ground path between units of the subsystem and due to the consideration of other subsystem interconnecting signals leads and associated signal levels, it was determined that a multipoint grounding philosophy, with respect to the structure, was the most practical method from a standpoint of System EMI considerations.

4.11.3.1.2 Signal Returns - Subsystem signal returns forming interconnections between units of the system, are multipoint grounded i.e. grounded at the source and at the load. The multipoint method was selected as the most practical concept to be consistent with type of circuitry involved and the shield ground philosophy.

4.11.3.1.3 Power Grounds - Primary power inputs to the system are balanced and are not grounded at or internal to the system in accordance with the interface requirements. The power supply unit has as an integral component, a DC-to-DC converter that

provides primary power input return isolation with respect to the vehicle ground point and provides regulated DC secondary power to the structure. However, to reduce secondary power ground currents in the structure the secondary power returns have been distributed to each internal subsystem module and then grounded to the chassis at each individual module.

4.11.3.1.4 Interface - The systems command, control, binary and analog interfaces have been grounded as specified by the LMSC Specification AA11654-3.

4.11.3.2 Bonding - Installation of the system in the carrier vehicle influences to a high degree the EMI integrity of the Reaper system. The shielding effectiveness of the individual units and interconnecting cables are dependent on the electrical bonding of the individual subsystems of the Reaper to the mating structure. The mating surfaces of the Reaper System and the vehicle are free of paint or other non-conductive finishes.

4.11.3.2.1 Surface Treatments - All mechanical assemblies, chassis, covers, panels, etc., constructed of aluminum have been treated with Alodine 1200 (s) process and/or tin-over-nickel plating. Mating surfaces of units, parts, cases and structures have been masked or assembled prior to prining, painting or mechanical bond. The electrical bond between mating surfaces has been maintained, however, where mechanical integrity was required, a fluid adhesive was used. The fluid adhesive, prior to hardening, is compressed by mechanical integrity was required, a fluid adhesive was used. The

fluid adhesive, prior to hardening, is compressed by mechanical fasteners and is extruded from between the mating metal to metal surfaces, at the fasteners. The adhesive therefore fills the air voids between mating surfaces but still permits good electrical contact at the joint.

4.11.3.3 Shielding - The cases of all critical units comprising the system have been designed to form a continuous metallic enclosure with a minimum number of mechanical discontinuities, such that the maximum effectiveness of the case can be realized for electrostatic and electromagnetic shielding.

4.11.3.4 Filtering

4.11.3.4.1 Primary Power Line Filters - Primary power line filters have been installed in the main power supply. The required attenuation and design characteristics of these filters has been determined from preliminary EMI tests on the breadboard units and by interference prediction techniques. Optimum attenuation to achieve specification compliance in accordance with the interface requirements was provided.

4.11.3.4.2 External Command and Control Leads - EMI control methods applied with respect to command and control leads consisted of shielding and filtering where required.

4.11.4 EMI Test Program

4.11.4.1 Requirements - The System is intended to comply with the applicable requirements of MIL-I-6181D and MIL-E-6051C with exception to those requirements which conflict with the

basic Reaper design concepts, however, no formal EMI qualification tests were required by the customer.

4.11.4.2 Design Evaluation Tests - Limited EMI design evaluation tests have been performed on some engineering model components deemed critical to the EMI performance of the System. These limited tests have been performed using the measurement techniques of MIL-I-6181D. Reports of the design evaluation tests were prepared as informal documentation. The prime purpose of these reports have been to inform the Program Manager of the EMI status of the components of the system with regard to compliance or non-compliance with the requirements of the Reaper Statement of Work, to identify any significant problem areas, and to recommend improvement changes.

5.0 TEST PROGRAM

5.1 Introduction

The system test program provides a comprehensive program of testing piece parts, components, subassemblies, assemblies, and subsystems used in the system. The objective of the test program is to achieve a high degree of confidence that the system will perform satisfactorily over its desired life span.

5.2 Classification of Tests

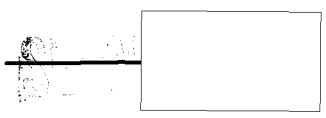
The test program consists of the following test classifications.

5.2.1 Receiving Inspection

All functional components and piece parts, purchased or used in the fabrication of the Reaper system, receive 100% inspection and test. Receiving Acceptance Test Specifications are provided and all tests are conducted in accordance with the specification, using currently dated, calibrated test equipment.

5.2.2 Parts Conditioning

All piece parts are conditioned and tested in a parts conditioning facility, operated as a unit of the Inspection and Test section of the Reliability and Quality Assurance Department.



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5.2.3 Developmental Testing

5.2.3.1 Circuit Testing

Breadboard tests, which are conducted to prove design adequacy, include: temperature tests, input parameter variation tests, and device interchangeability tests. Temperature tests are conducted in all areas where new circuit designs are involved. Parameter variation and device interchangeability tests are conducted where potential problem areas exist.

Specific design areas where tests are conducted include the Digital, IF, RF, and Power Supply areas. Test temperatures as shown below have evolved through termal analysis aimed at establishing the maximum component operating temperatures in the final environment.

Digital	-30°F to +200°F
IF	-30°F to +185°F
RF	-30°F to +185°F
Power Supply	-30°F to 212°F

The basic objective of development temperature testing is to verify circuit designs to temperatures exceeding the expected orbital maximum and minimum values by at least 30°F.

5.2.3.2 Structure Testing

Vibration and shock tests were performed on a sample of the honeycomb material to test bonding and resonant frequency characteristics. Simulated structures were mounted on the honeycomb deck with various types of inserts, and the

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structure was vibrated and shocked to test the adequacy of insert design.

5.2.3.3 Antenna Testing

Each antenna design was tested in order to assure correct operation and specification compliance as described below:

a) Circularity (axial ratio) - Data taken as a function of frequency and azimuth and elevation from the boresight axis.

b) Absolute Gain - Data taken to determine the absolute gain of each antenna using swept frequency techniques.

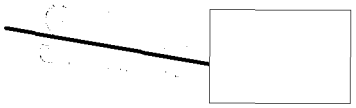
c) Amplitude Patterns - Data taken and amplitude patterns plotted for each antenna as a function of azimuth, elevation, and frequency.

d) VSWR - Data taken on the VSWR characteristics of each antenna using swept frequency techniques.

e) Antenna Array Mockup - Antenna amplitude-pattern data taken using mechanical configurations that approximate the actual array.

5.2.3.4 Procured Subassembly Testing

Developmental tests were performed on two major purchased subassemblies; a) the local oscillators and b) the core memories. The core memories were tested to acceptance levels of shock, vibration, temperature, and vacuum at the



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vendor's establishment and, prior to shipment, the core memories were tested to a 100% operational verification test, designed to exercise every core. The LO was fully qualified at the vendor's establishment and was further tested at LTV where it is to be stressed to end-of-life using qualification test models to determine the design margin.

5.2.4 Subassembly and Assembly Testing

The test program for Reaper hardware at the subassembly and assembly level is conducted in two major phases. The first phase is the individual testing of all subassemblies to assure their correct operation prior to integration into an assembly. The second phase is the series of integration tests that assure the correct operation of the various assemblies when they are connected as a system.

5.2.4.1 Phase 1, Subassembly Testing

Each subassembly is tested as described below after fabrication, assembly, and initial inspection have been completed.

5.2.4.1.1 IF Subassembly and Assembly Testing

Each IF subassembly is properly aligned where necessary by the selection of passive components (resistors, thermistors, etc.) in test. Some subassemblies are connected and aligned as a group rather than individually.

All IF subassemblies are completely tested at temperatures of +77°F, +165°F and -30°F, measured on the sub-

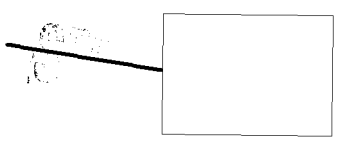
assembly chassis. Inputs which simulate actual input parameters (including power) are varied over the operating limits and all outputs are observed for correct operation. In addition, the outputs of the subassembly are monitored for correct operation over the temperature range for a selected set of input parameters. In the cases where two or more subassemblies are to be connected for correct alignment, they are also tested together.

Each IF subassembly is covered with a protective coating after successfully completing the dynamic tests above. After the coating has been applied, each subassembly is retested over the same dynamic test conditions.

The subassemblies are connected to form the IF assembly, and tests are first conducted at room temperature to ensure correct operation and then over the test conditions described for the IF subassemblies above. Data handler, preamplifier, and power supply inputs to the IF are simulated, and the ability of the IF assembly to adjust for boresight is determined.

5.2.4.1.2 Data Handler Subassembly and Assembly Testing

Each card in the Data Handler is tested at room temperature by using appropriate logic signal and power inputs (varied over the allowable ranges) to ensure correct operation of each integrated circuit module on the card. Every input and output is monitored. After successfully completing the designated tests, the card is reinspected, covered with a pro-



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tective coating and retested.

The tested cards are connected in a subassembly and tested at -30°F, +77°F and +200°F with the input parameters varied over the allowable ranges. All outputs are monitored and correct operation is verified. In addition, a selected set of input signals and power parameters are used and the subassembly outputs are monitored to check for correct operation as the temperature is varied from -30°F to +200°F.

The core memories of the Data Handler are constructed and tested as subassemblies. Initial testing involves a room temperature core test to assure correct operation of each core and associated drivers in each subassembly. The subassembly is then operated and tested at -30°F, +77°F and 175°F, measured on the housing.

The Data Handler card rack is periodically inspected for construction and good workmanship as it is being wired. Upon completion of the wiring, an "all possibility" continuity test is conducted to assure that every wire specified is correctly connected and that there are no shorts nor other undesired connections between card connections.

Each of the discrete component cards, integrated circuit cards and core memory assemblies are connected and tests are conducted at -30°F, +77°F and +175°F, measured on the housing to ensure correct operation of all Data Handler functions over the complete range of allowable input conditions. Simu-

lated IF inputs and external commands are used in these tests.

The wiring of the TM subassembly is checked as a part of the Data Handler rack wiring. Circuits are tested and correct operation is verified as a function of temperature from -30°F to +165°F. Where required, thermistor calibration is accomplished prior to installation in the system.

5.2.4.1.3 Power Supply Testing

Several power supply components require testing at a component level. Among the components requiring special tests are the following.

a) Power transformer - turns-ratio test

b) Switching transistor - Beta matching

c) Driver transformer - turns-ratio test

Integrated circuits subassemblies used for power supply control are functionally tested at -30°F, +77°F and +212°F with inputs varied over the allowable ranges. In addition, a selected set of input parameters is used and correct operation of the control circuits is verified as the temperature is varied from -30°F to +212°F. The integrated circuit cards are covered with a protective coating and retested after successful completion of specified tests and inspections.

The power section, including the rectifiers and drivers, is tested as a subassembly at -30°F, +77°F, and +212°F. Control inputs are supplied by the previously tested control circuits. Correct operation is verified over the allowable

range of all input parameters. Power dissipation of individual components is calculated from voltage and current measurements. Efficiency of the power section is calculated as a function of load, temperature and input voltage variables.

After the initial tests, the assembly is completed (protective coating, inspection, etc.) and retested.

The reference-source circuits and error-sensor circuits are functionally tested at room temperature. Components are selected for temperature compensation and are temporarily connected to the circuits. Repeated tests over the temperature range are conducted for different selections of compensation until a satisfactory compensation network is achieved. The temperature compensation network is then permanently soldered on the circuit board and is inspected before a protective coating is applied. It is retested after the protective coating is applied.

The tested cards and components are then connected as an assembly and functionally tested at -30°F, +77°F, and +190°F, measured on the housing, over its required limits of input voltage and output load. Temperature monitors are used to indicate hot spots in the power supply. Input and output voltage and current measurements are made to determine overall regulation and efficiency. Voltage ripple of each output is measured with an oscilloscope with particular attention given to high frequency spikes caused by the oscillator and input

switching circuits. Requirements of minimum level transients are imposed upon the power supply outputs. A test is conducted on the power supply to assure correct operation, with no degradation nor failure, in the presence of 30-volt, 10-usec pulses on the power input lines.

5.2.4.1.4 RF Assembly Testing

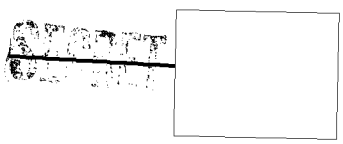
The RF section of the RF assembly is tested as follows.

a) Coupler - Swept-frequency measurements of phase tracking, VSWR and coupling are made over the RF frequency ranges on the coupler at temperatures of -30°F, +77°F and +165°F.

b) RF Checkout Board (7-Way Divider) - Swept-frequency measurements of phase tracking, VSWR and amplitude are made at -30°F, +77°F and +165°F.

c) Bandpass Filter - Swept-frequency measurements of phase tracking, insertion loss, amplitude rejection and VSWR are made at -30°F, +77°F and +165°F.

d) Main Stripline - Swept-frequency measurements of phase tracking, amplitude, noise figure, VSWR, bandwidth, and gain are made at -30°F, +77°F and +165°F. The system IF preamplifier is integrated with the stripline prior to



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stripline measurement tests.

e) RF Section Integration - The coupler, checkout board, and bandpass filter are connected to the stripline and the resulting RF package is functionally tested by performing swept-frequency measurements of phase tracking, noise figure, amplitude tracking and VSWR at -30°F, +75°F and +165°F. In addition, selected input parameters are used and phase tracking, noise figure, amplitude tracking and VSWR measurements are made as the temperature is increased from -30°F to +165°F.

Spurious rejection measurements are made on the Signal Indicate (SI) channels at +77°F.

The LO section of the RF assembly is tested as follows:

a) Reference Power for D/A Converter - Voltage regulation, ripple, including high frequency components, and efficiency are measured as a function of input voltage variation at -30°F, +75°F and +165°F.

b) Digital-to-Analog Converter - The subassembly is tested by using digital inputs of every possible combination while measuring the output voltage. The tests are conducted at -30°F, +75°F and +165°F. After successfully completing specified tests, the subassembly is

reinspected, covered with a protective coating and retested.

c) Current Driver - The current drivers which supply current to the local oscillator coils are tested by measuring the output current as a function of input voltage at temperatures of -30°F, +75°F and +185°F. Protective coating is not added to the current driver at this time because of necessary summing resistor selection during the driver-LO integration.

d) Local Oscillator Section Integration - Frequency, power output, and spurious frequency measurements are made as a function of input current at temperatures of -30°F, +75°F and +165°F. The LO and its associated drive circuits (D/A reference power, D/A converter, and current driver) and oven are connected to form the Local Oscillator subassembly. Summing resistors are selected as frequency, frequency stability and linearity tests are conducted over the temperature range. After correct operation of the LO subassembly has been verified, the selected components are permanently soldered in place and the current driver is covered with a protective coating. Tests are

repeated to ensure correct frequency, frequency stability, linearity, and output power compliance over the temperature range.

The RF section and the LO section are integrated and the resulting RF assembly is functionally tested to determine noise figure, LO accuracy and frequency linearity at -30°F, +75°F and +165°F. Phase tracking and spurious rejection measurements are made at room temperature. In addition, tests are conducted on the RF package using selected input parameters while varying the temperature from -30°F to +165°F. All RF outputs are monitored and correct operation of each output is verified.

5.2.4.1.5 Antenna Tests

Each antenna is tested in order to ensure correct operation and compliance in the areas listed.

a) Circularity (axial ratio) - Circularity data is taken as a function of frequency and azimuth and elevation from the boresight axis.

b) Absolute Gain - Data is taken to determine the absolute gain of each antenna using swept-frequency techniques.

c) Amplitude Patterns - Data is taken and amplitude patterns are plotted for each antenna as a function of azimuth, elevation, and frequency.

d) VSWR - Data is taken on the VSWR characteristics of each antenna using swept-frequency techniques.

The tested antennas are mounted on the honeycomb plate and tested.

e) Mechanical Boresight - The mechanical boresight alignment of each antenna is measured and antenna pairs are mechanically aligned. Axial alignment of each antenna is fixed in accordance with the data taken in paragraph 5.2.4.1.5a.

f) Circularity - Circularity tests are conducted on each antenna in the array as a function of frequency and azimuth and elevation from the boresight axis.

g) Amplitude Patterns - Data is taken and amplitude patterns are plotted for each antenna as a function of azimuth, elevation, and frequency.

5.2.4.2 Phase 2, Integration Testing

System integration is conducted on a step-by-step basis by conducting tests and taking sufficient measurements at each assembly interface to assure compatibility and correct operation before proceeding to the next step.

5.2.4.2.1 Power Supply/IF Integration

The IF assembly is connected to the power supply and voltage measurements are made on the IF deck as the power

supply input is varied from 22.0 VDC to 29.3 VDC. IF outputs are monitored and correct operation of the IF assembly is verified. IF outputs are loaded by passive loads to simulate the actual loads.

5.2.4.2.2 Power Supply/DH Integration

The data handler is connected to the power supply. Voltage measurements are made on the data handler as the power supply input voltage is varied from 22.0 VDC to 29.3 VDC. DH inputs are simulated and DH outputs are monitored. Correct operation of the DH and power supply assemblies is verified.

5.2.4.2.3 Power Supply/IF/DH Integration

The power supply, IF, and DH assemblies are connected and simulated signals are applied to the IF assembly. Command and control signals to the DH are simulated. Correct operation of the three assemblies is verified.

5.2.4.2.4 RF/Antenna

The RF and antenna assemblies are connected and tests are run to determine correct operation of the integrated pair. Mechanical alignment and electrical antenna tests are conducted to determine antenna characteristics as specified in paragraph 5.2.4.1.5e, f, and g. Power inputs are from commercial power supplies. RF inputs are phase-controlled signals supplied by the RF console of the STE or RF signals emanating from a dish antenna.

5.2.4.2.5 Power Supply/IF/DH/RF Integration

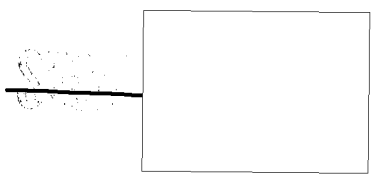
All assemblies are connected. Voltage measurements are made on each of the assemblies as the input voltage to the power supply is varied from 22 VDC to 29.3 VDC. RF input to the system is supplied by the STE RF console and commands to the system are supplied by the STE command and control console. Correct operation of the system (exclusive of the antennas) is verified as the DC power and RF input parameters are varied over their dynamic range. Telemetry outputs are monitored by the STE T/M scanner and correct telemetry voltage output of each TM point is verified.

5.2.4.2.6 System Temperature Test

The system is subjected to a temperature test with test levels equal to those required for the acceptance test thermal soak. The test sequence includes a temperature stabilization and a performance test at +160°F and at -30°F. After correct system operation at the two temperature extremes has been verified, correct performance is verified at room temperature.

5.2.4.2.7 Range Integration Tests

The system is then transported to the range where further testing is conducted and necessary range adjustments are made.



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5.2.5 Qualification Test

The qualification test consisted of environmental tests and range performance tests as described in the following paragraphs.

5.2.5.1 Qualification Environmental Test

a) Sinusoidal Vibration - 1 g rms from 10 to 2000 cps with a duration of 2 minutes/octave in each of 3 axes.

b) Random Vibration - 20.2 g rms overall for 3 minutes/axis.

c) Pyrotechnic Shock - As shown in Figure 5.2-1 in each of three axes.

d) Thermal Cycle - +160°F at less than 10^{-5} torr pressure for 12 hours and then at -30°F at less than 10^{-5} torr pressure for 12 hours.

e) Thermal Soak - +160°F for 20 hours after stabilization and then -30°F for 20 hours after stabilization.

5.2.5.2 Range Performance Test

A range performance test was performed to provide verification of system performance.

5.2.5.2.1 Payload/Vehicle Interface Compatibility

The payload/vehicle interface compatibility was verified with tests of the following functions.

a) Input Power

b) Telemetry Data Output

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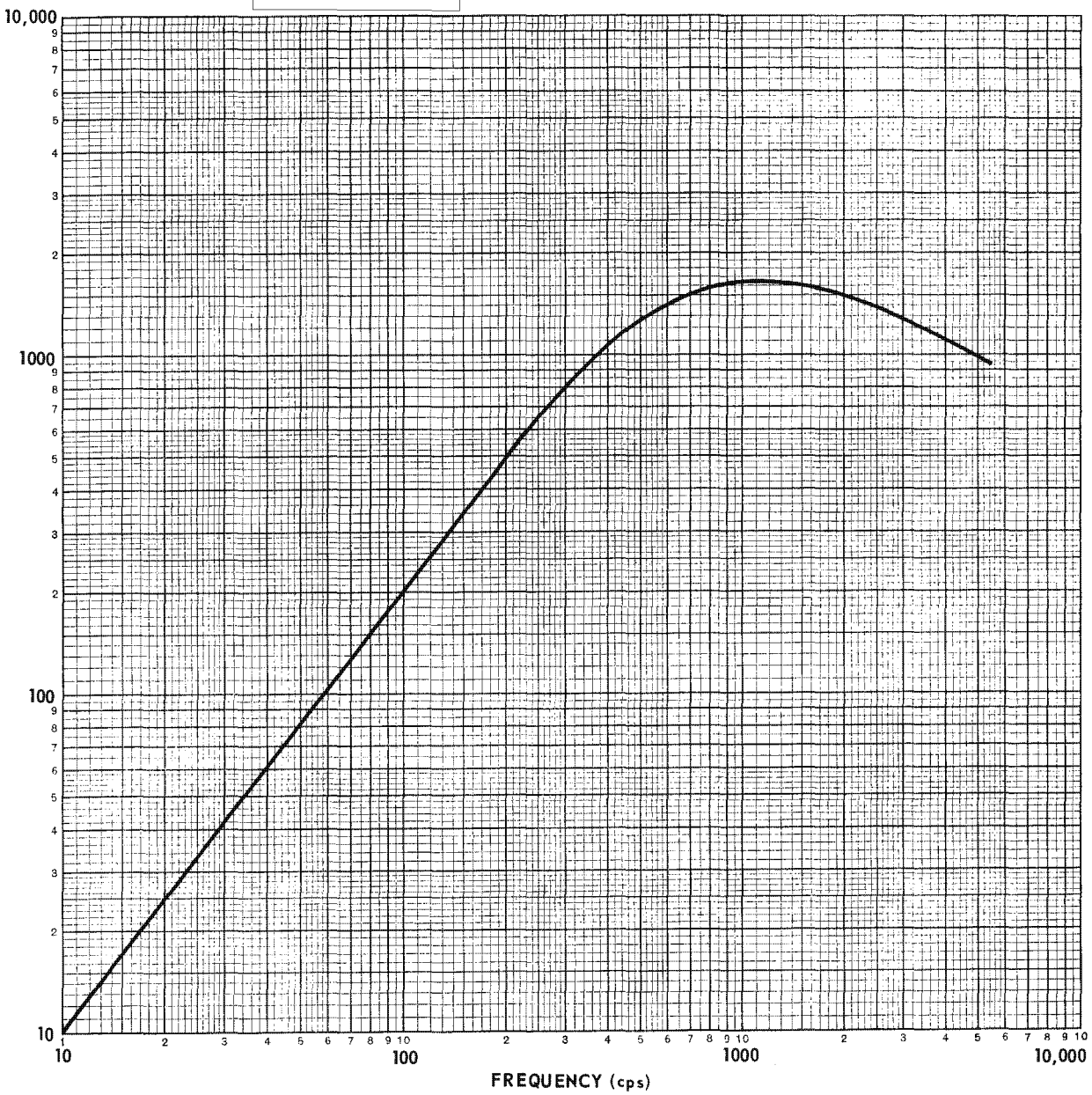

Figure 5.2-1. Pyrotechnic Shock Response Spectrum (Q-10)

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c) Digital Data Output

d) Analog Data Output

e) Payload Commands

f) Memory Loading

g) Vehicle Clock Input

h) Vehicle Attitude Input

i) RF Signal Insertion

5.2.5.2.2 EOB Functional Operation

The Electronic Order of Battle (EOB) functional operation was verified with tests of the following functions.

a) LO Dwell Time and Scan Time

b) Partial Scan

c) Confirm Bandwidth

d) Operational Frequency Range

e) Phase Field-of-View

f) Amplitude Inhibit Circle

g) Sensitivity Versus Frequency

h) Sensitivity Variations by Command

i) Dynamic Range

j) Space Window

k) Interleaved Pulse Train

l) CW Operation

m) CW Plus Pulse Train

n) Ambiguity Resolution

o) Amplitude Pokethrough

p) RF Calibrator

5.2.5.2.3 EOB Parameter Measurement Accuracies

The EOB parameter measurement accuracies were verified with tests of the following functions.

a) Pulse Width

b) Pulse Repetition Interval

c) Signal Amplitude

d) Frequency

e) Location

5.2.5.2.4 TI Functional Operation

The Technical-Intelligence (TI) operation was verified with tests of the following functions.

a) Recognizer Operation

b) Predetection Data

c) Marker Words

5.2.5.2.5 TI Measurement Capabilities

The TI measurement capabilities were verified with tests of the following functions.

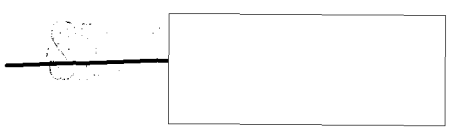
a) Pulse Width

b) Bandwidth

c) Amplitude

5.2.6 Acceptance Test

An acceptance test is performed on each FM system. The acceptance test consists of environmental tests and range performance tests as described in the following paragraphs.



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5.2.6.1 Acceptance Environmental Test

a) Random Vibration - 10.2 g rms overall for 3 minutes/axis.

b) Thermal Soak - +160°F for 20 hours after stabilization and then -30°F for 20 hours after stabilization.

c) Vacuum - Less than 10^{-5} torr pressure for 12 hours.

5.2.6.2 Range Performance Test

Following acceptance environmental test, the range performance test is repeated. This range test is essentially the same as described in paragraph 5.2.5.2.

5.3 Documentation

LTVE documents that specify the test procedures used in performing the subassembly tests, the assembly tests, the integration tests, the pre-qualification tests, the qualification tests, the pre-acceptance tests, and the acceptance tests are listed in Table 5.3-1.

TABLE 5.3-1

TEST PROCEDURES

LTVE NUMBER	TITLE
	System Test Procedures
4124-00005	Reaper Acceptance Test Procedure
4124-00007	Reaper Pre-Acceptance Test Procedure
4124-00004	Reaper Qualification Test Procedure
4124-00006	Reaper Pre-Qualification Test Procedure
4124-	Reaper Final Integration Test Procedure
	Integration Test Procedures
4124-	RF/IF/Power Supply Integration Procedure
4124-11100	RF/Antenna Integration Procedure
4124-11099	RF Subsystem Integration Procedure
4124-	Data Handler Integration Procedure
	RF Section Assembly and Subassembly Test Procedures
4124-11170	High Band Antenna Test Procedure
4124-11171	Low Band Antenna Test Procedure
4124-11022	RFCO Board Test Procedure
4124-11020	RF Filter Test Procedure
4124-11134	RFTSG Test Procedure
4124-11019	20 db Coupler Test Procedure
4124-11023	Stripline Subassembly Test Procedure
4124-13107	Diode and Holder Test Procedure
4124-11008	Preamp Test Procedure

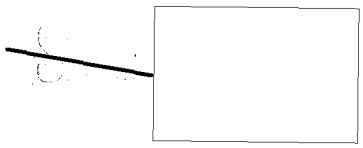

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TABLE 5.3-1 (Continued)

TEST PROCEDURES

LTVE NUMBER	TITLE
4124-11007	Preamp Switch Test Procedure
4124-11056	Signal Combiner Test Procedure
4124-11106	Local Oscillator Subassembly Test Procedure
4124-11047	9-Bit D/A Test Procedure
4124-11046	8-Bit D/A Test Procedure
4124-11045	Reference Regulator Test Procedure
4124-11048	Low Band Current Driver Test Procedure
4124-11049	High Band Current Driver Test Procedure
IF Section Assembly and Subassembly Test Procedure	
4124-11096	IF Subsystem Test Procedure
4124-11010	Phase Channel Test Procedure
4124-11013	Log IF Test Procedure
4124-11011	Frequency Confirm Test Procedure
4124-11015	SI Generator Test Procedure
4124-11017	A/D Converter Test Procedure
4124-11014	Amplitude Ratio Test Procedure
4124-11016	Real/Image Test Procedure
4124-11057	IF Hybrid Test Procedure
4124-11018	Recognizer Threshold Test Procedure
4124-11009	Pre-Detector Test Procedure

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TABLE 5.3-1 (Continued)

TEST PROCEDURES

LTVE NUMBER	TITLE
	Power Supply Assembly and Subassembly Test Procedure
	Power Supply Subsystem Test Procedure
	Switch Assembly Test Procedure
	Regulator/Distribution Assembly Test Procedure
	Recognizer Assembly and Subassembly Test Procedure
	Recognizer Rack Test Procedure
4124-11167	Recognizer Programmer Test Procedure
4124-11103	Turn-On Control Test Procedure
4124-11105	Frequency Limit Comparator Test Procedure
4124-11107	Pulse Width Limit Comparator Test Procedure
4124-11104	Record Mode Control Test Procedure
4124-11110	PRI Limit Comparator Test Procedure
4124-11108	PRI Buffer Test Procedure
4124-11139	Recognizer Memory Logic Test Procedure
4124-11101	Memory Logic A Test Procedure
4124-11102	Memory Logic B Test Procedure
4124-11111	Memory Logic C & D Test Procedure
4124-11113	Memory Logic E & F Test Procedure
4124-11116	Memory Logic G & H Test Procedure
4124-11138	Memory Logic J Test Procedure

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TABLE 5.3-1 (Continued)

TEST PROCEDURES

LTVE NUMBER	TITLE
4124-11168	Discrete Component Interface Test Procedure
	Memory Assembly and Subassembly Test Procedure
4124-11024	Buffer Storage Assembly Test Procedure
4124-11032	SWI Memory Test Procedure
4124-11030	Recognizer Memory Test Procedure
4124-11025	Buffer Storage Z Driver #1 Test Procedure
4124-11026	Buffer Storage Strobe Driver #2 Test Procedure
4124-11027	Buffer Storage Sense Amp #5 Test Procedure
4124-11028	X & Y Driver #3 Test Procedure
4124-11029	X & Y Switch #4 Test Procedure
4124-11120	Buffer Storage Sense Amp #6 Test Procedure
4124-11031	Recognizer Sense Amp #5 Test Procedure
4124-11121	Recognizer Z Driver Test Procedure
4124-11033	SWI Z Driver #1 Test Procedure
4124-11034	SWI Stobe Driver #2 Test Procedure
4124-11035	SWI Sense Amp #5 Test Procedure
	Relay and T/M Assembly Test Procedure
	Relay Assembly Test Procedure
	T/M Assembly Test Procedure

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TABLE 5.3-1 (Continued)

TEST PROCEDURES

LTVE NUMBER	TITLE
	Data Handler Assembly and Subassembly Test Procedure
	Data Handler Rack Test Procedure
4124-11157	Coder/Combiner Subassembly Test Procedure
4124-11059	Coder/Combiner A Test Procedure
4124-11060	Coder/Combiner B Test Procedure
4124-11061	Coder/Combiner C Test Procedure
4124-11062	Coder/Combiner D Test Procedure
4124-11161	SWI Subassembly Test Procedure
4124-11083	SWI A Test Procedure
4124-11084	SWI B Test Procedure
4124-11088	SWI C Test Procedure
4124-11085	SWI D Test Procedure
	Clock/Pulse Width Subassembly Test Procedure
4124-11070	Clock Oscillator Test Procedure
4124-11066	Clock Logic Test Procedure
4124-11065	Pulse Width Encoder Test Procedure
4124-11135	Marker Generator Subassembly Test Procedure
4124-11092	Marker Generator A & B Test Procedure
4124-11094	Marker Generator C & D Test Procedure
4124-11136	Scan Control Subassembly Test Procedure

TABLE 5.3-1 (Continued)

TEST PROCEDURES

LIVE NUMBER	TITLE
4124-11089	Control A & B Test Procedure
4124-11091	Control LO Counter Test Procedure
4124-11069	Programmer A & B Test Procedure
4124-11068	Programmer C & D Test Procedure
4124-11067	Programmer E Test Procedure
4124-11076	Programmer F Test Procedure
4124-11126	Isolation Buffers A & B Test Procedure
4124-11028	PRI Encoder Buffers Test Procedure
4124-11073	PRI Encoder A Test Procedure
4124-11071	Time Reset/Encoder-Calibrator Test Procedure
4124-11098	Interface A Test Procedure
4124-11063	A & B Encoder Test Procedure
4124-11137	LO & PS/K Interface Test Procedure
4124-11140	Buffer Storage Subassembly Test Procedure
4124-11078	Bit/Search Counter Test Procedure
4124-11086	Memory Driver A & B Test Procedure
4124-11087	XY Selector Logic Test Procedure
4124-11074	Input Gating A & B Test Procedure
4124-11077	Interface Logic A & B Test Procedure
4124-11080	Input Gate Control and Section Counter Test Procedure

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TABLE 5.3-1 (Continued)

TEST PROCEDURES

LTVE NUMBER	TITLE
4124-11079	Command Logic A & B Test Procedure
4124-11081	BS Output Register & Word Counter Test Procedure

6.0 [redacted]ABILITY PROGRAM

6.1 Introduction

This section summarizes the major activities of the reliability program and presents numerical reliability values for the system in different modes of operation.

6.2 Reliability Requirements

The primary elements of the reliability program are as follows:

1) Parts Program
2) Design Reviews
3) Subcontractor Control
4) Limited Life Items
5) Trouble and Failure Reporting
6) Log Books
7) Reliability and Quality Assurance Interfaces

6.2.1 Reference Documents

LTV Document No. 52000-R400	Black Hawk Reliability Program Plan
LTV Document No. 52000-R401	General Procedure for Reliability Screening and Conditioning of Electrical and Electronic Parts
LTV Document No. 53000-R368	Standard for Parts Selection and Application

6.3 Reliability Implementation

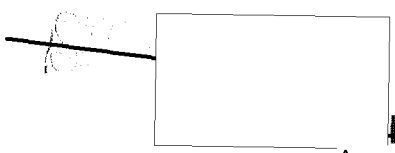
The following reliability activities were implemented to assure the most reliable design within the limitations of weight, volume, schedule and cost.

6.3.1 Parts Control

The parts control program consisted of three major phases, these being parts selection, parts application and parts conditioning.

6.3.1.1 Parts Selection - The primary document used to control parts selection was LTV Electrosystems, Inc., Document No. 53000-R368, "Standard for Parts Selection and Application". This document lists preferred types of common electronic parts that either by previous military usage and/or by previous LTV Electrosystems, Inc., usage have demonstrated high inherent reliability. In many instances the design engineer is directed to use a particular part as described by the applicable MIL-Standard.

In other instances, notable in the case of transistors and diodes, the design engineer is directed to use devices described by the applicable LTV Electrosystems, Inc., Specification Control Drawing (SCD). These transistor and diode SCD's in many instances require that the devices meet X-ray, visual, acceleration and leak test requirements in addition to meeting all of the requirements of the applicable MIL-S-19500.



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[redacted] There is another large group of parts that are described only by SCD. Within this group are such items as integrated circuits, the newer type diodes and transistors and other miscellaneous components that have no military equivalent.

6.3.1.2 Parts Application - Document No. 53000-R368 also contains general rules for the reliable application of piece parts. Design goal derating factors are specified for the use of the particular part type. Normally this design goal rating is 10 percent of the vendor's rating. There is also an approved derating for each part, normally 25 percent of vendor rating. For each individual application where the applied stress level exceeds the approved stress level the application must be approved by Special Projects Reliability Engineering.

6.3.1.3 Parts Conditioning - LTV Electrosystems, Inc., has built a facility for aging and screening of parts destined for use in future production units. This operation is described in more detail in LTV Document No. 52000-R401 and documents referenced therein. The primary objective of the parts conditioning activity is to increase the inherent reliability of the system by eliminating those parts that are initially defective or marginal and those parts that show a marked tendency to drift with usage.

6.3.2 Design Reviews

All electronic and mechanical designs were reviewed and signed by Reliability Engineers prior to release.

The electronic design reviews were conducted to determine that all parts used were approved parts, that all parts were adequately derated, and that the circuitry was inherently reliable. The mechanical design reviews consisted of a review of all artwork, module construction, interconnection of various subassemblies, and all mounting structures. These design reviews were conducted to assure that the inherent reliability of the electronic circuitry was not degraded by poor mechanical design.

6.3.3 Subcontractor Control

Reliability requirements have been placed directly on the component part manufacturers in many instances through the requirements as specified on various SCDs. In addition to the control of vendor parts, Reliability and Quality Assurance has closely monitored subassembly subcontractors through the process of electrical and mechanical design reviews such as were conducted on equipment designed and constructed at our own facilities. Additionally, reliability engineers have visited the facilities of subcontractors in order to closer monitor the subcontractor activities and to instill in subcontractor personnel the importance of the reliability requirements of the particular subassembly.

6.3.4 Limited Life Items

There are no parts used in the system that have an anticipated wear out prior to end of life of the equipment.

There are some relays used in the system that are expected to wear out after a certain number of cycles; however, when the relay use cycle is considered, it is easily determined that wear-out will not occur until long after the anticipated life of the system.

6.3.5 Trouble and Failure Reporting

The trouble and failure reporting (TFR) system described in Section 4.6 of 52000-R400 is in operation. At this time, all TFR records are being maintained by reliability engineers.

As applicable, the information obtained on TFR follow-up is being fed back into system design to remove all possibility of certain type failures. Beginning with STM qualification testing, all critical TFRs will be reported in a monthly malfunction report as required by 52000-R400.

The TFRs being processed at this time are forming a background of history to be drawn upon in the evaluation of failures and discrepancies reported on future production equipment.

6.3.6 Log Books

Each system will have log books that will be used to record system operating time, system performance data, system failures and malfunctions and system repairs. These log books, coming into existence at the time the parts are assembled into a system, along with the TFR records and the Quality Assurance

assembly, inspection and test records will constitute a complete history of each system.

6.3.7 Reliability and Quality Assurance Interfaces

With the emphasis on high inherent reliability, the activities of the Special Projects Reliability Engineering has extended into certain areas that are related to Quality Assurance or Quality Control. The primary areas of interface being manufacturing control, parts storage and control, and unit and subassembly testing. One of this group of activities is the requirement that all Material Review actions require the signature of a reliability specialist in addition to Quality Assurance and Engineering Design signatures.

6.4 Reliability Estimate

Operating and non-operating failure rates have been assigned to each component part within the system. The operating failure rates reflect the stresses applied to each part as was determined during the electrical design review as described in paragraph 6.3.2. The failure rates used in this estimate are lower than those found in MIL-HDBK-217 and similar publications for two reasons: First, technological advances in part manufacturing have produced parts of greater inherent reliability and second, the screening and conditioning of parts as described in paragraph 6.3.1.3 has removed the marginal and unstable parts from the system. Therefore, the failure rates used in this estimate closely follow the failure rates obtained on the Minuteman and other high reliability programs.

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6.4.1 Module Failure Rates

Table 6.4-1 Module Failure Rates, tabulates by major modules the system failure rate attributable to each major module. In each instance there is an operating and non-operating failure rate assigned to the module. In addition to the piece-part failure rate, this failure rate includes a failure rate for the solder and weld junctions within that module.

6.4.2 Reliability Diagram

The reliability diagram, Figure 6.4-1, shows the modules of Table 6.4-1 grouped into six major blocks with sub-block within some major blocks. The failure rate shown in the block is the operating failure rate.

6.4.3 System MTBF

From the classical reliability prediction standpoint, all components within the system are in a series configuration. On this basis, the system has an operating MTBF of 3270 hours and a non-operating (storage) MTBF of 14,800 hours. This prediction is based on the assumptions that all failures cause catastrophic failure of the system. This is pessimistic as all systems have items such as decoupling capacitors which could fail in the open mode causing increased noise within the system but not complete system failure.

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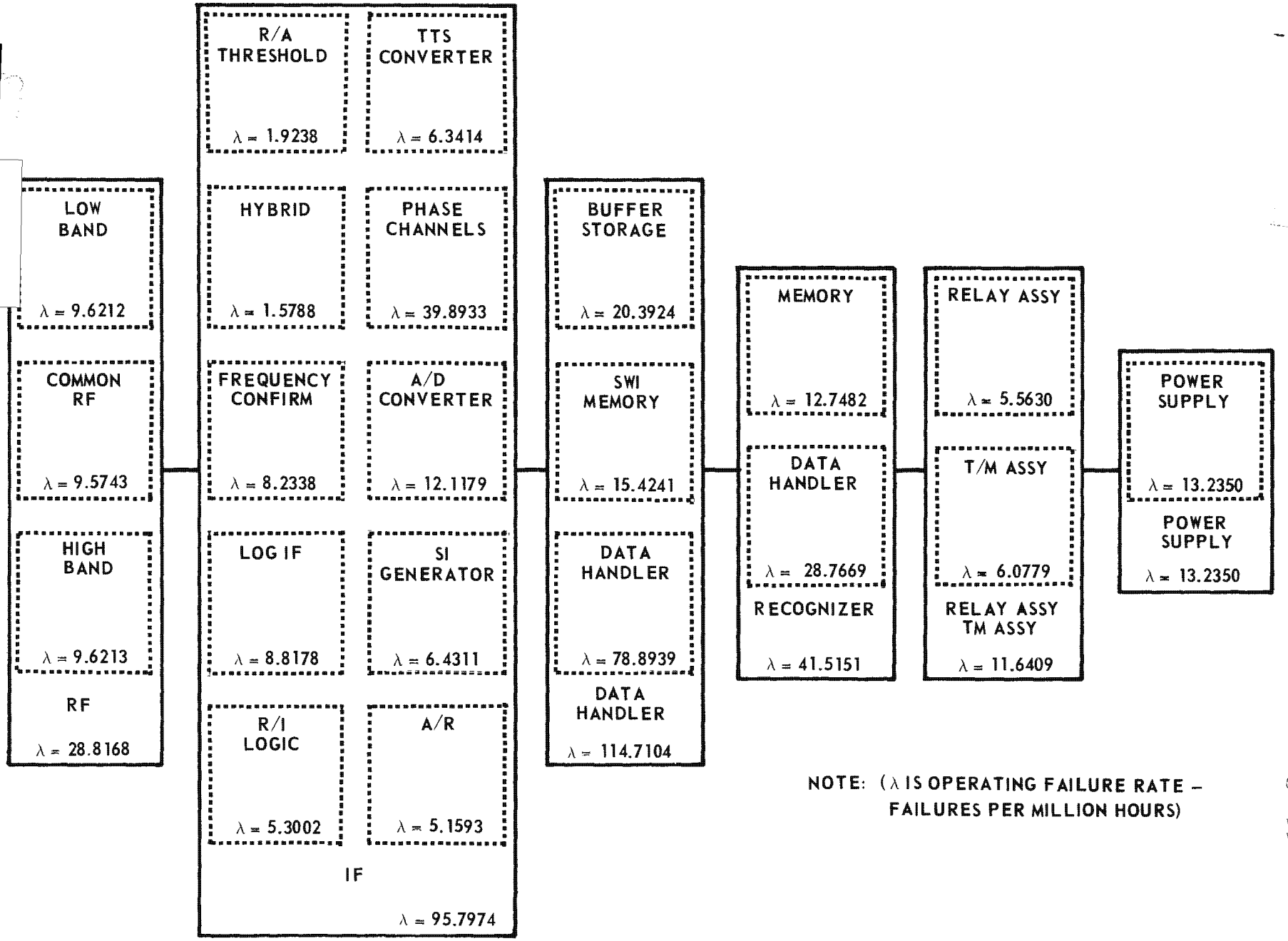
TABLE 6.4-1 MODULE FAILURE RATES

MODULE	PART NUMBER	FAILURE RATES - FAILURES PER 10^9 HOURS	
		OPERATING	NON-OPERATING
D/A Converter	18100	5,025.1	855.0
LO Oven	15000	3,449.8	445.8
RF Syst. Calibrator	14200	1,099.4	128.0
Preamp Switch (2 ea)	16100	136.4	36.8
Signal Combiner	16200	5,423.7	451.6
IF Preamp No. 2 (2 ea)	13500	1,701.2	122.8
IF Preamp No. 1 (14 ea)	13300	11,981.2	865.2
R/A Threshold	59500	1,923.8	278.8
TTS Converter #1	58000	4,958.2	568.8
TTS Converter #2	58500	1,383.2	117.5
Hybrid	59000	1,578.8	108.0
IF Phase Channel (3 ea)	51000	29,916.0	2,568.9
IF Phase Channel No. 2	51100	9,977.3	856.8
Frequency Confirm	57000	8,233.8	625.6
A/D Converter	54000	12,117.9	1,496.9
Log IF (2 ea)	56000	8,817.8	873.4
SI Generator	55000	6,431.1	630.0
R/I Logic	53000	5,300.2	568.8
Amplitude Ratio	52000	5,159.3	500.7
Power Distribution Assy.	65500	5,570.6	970.3
Power Supply	65000	7,664.4	1,312.2

TABLE 6.4-1 MODULE FAILURE RATES

MODULE	PART NUMBER	FAILURE RATES FAILURES PER 10^9 HOURS	
		OPERATING	NON-OPERATING
Buffer Storage	60000	20,392.4	6,397.9
Recognizer Memory	61000	12,748.2	2,479.0
SWI Memory	62000	15,424.1	4,206.5
Relay Assembly	66000	5,563.0	2,039.8
Data Handler	64000	78,893.9	27,029.1
Data Handler No. 2	63000	28,766.9	10,082.1
T/M Assembly	68000	6,077.9	829.1
TOTAL		305,715.6	67,445.4



NOTE: (λ IS OPERATING FAILURE RATE – FAILURES PER MILLION HOURS)

Figure 6.4-1. Reliability Diagram

[redacted]

6.4.4 Probability of Survival

The system has five major operational modes, these being (1) normal (EOB) data processing, (2) normal (EOB/TI) data processing, (3) recognizer memory load, (4) partial scan memory load and (5) memory readout. These operational modes are described in Sections 2.0 and 3.0 of this report. Probability of survival calculations will be made for the first two modes of operation. No calculations were made for the last three modes as these modes are an essential part of the second mode.

6.4.4.1 Mode 1 Probability of Survival - The following units and cards are not used in Mode 1:

1) 61000, Recognizer Memory
2) 63000, Data Handler #2
3) 68000, T/M Assembly
4) 64240, Scan Control
5) 64249, PS/K Interface
6) 64328, Scan Control A and B
7) Part of 66000, Relay Assembly

These units and cards contribute 54,132.9 failures x 10^{-9} hours to the operating failure rate and 16,098.4 failures x 10^{-9} hours to the non-operating failure rate. This leaves a total operating failure rate of 251,582.27 failures x 10^{-9} hours and a non-operating failure rate of 51,347.0 failures x 10^{-9} hours.

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[redacted]

The maximum duty cycle for the system is 30 minutes of operation during each 95-minute orbit. This will give an average failure rate of 114,579.4 failures x 10^{-9} hours, which is 30/95ths of the operating failure rate and 65/95ths of the non-operating failure rate. The probability of system survival for time T is calculated from the classical reliability equation.

$$P_S = e^{-\lambda T}$$

where

P_S = probability of success

e = base of natural logarithmic system

λ = predicted failure rate (per hour)

T = mission duration in hours

Figure 6.4-2 is a plot of this equation for a period of one year.

6.4.4.2 Mode 2 Probability of Success - The only unit not essential to Mode 2 operation is the 68000 module. This leaves a total operating failure rate of 299,637.7 failures x 10^{-9} hours and a non-operating failure rate of 66,616.3 failures x 10^{-9} hours. The average failure rate for this mode is 140,202.0 failures x 10^{-9} hours. Figure 6.4-3 is a plot of the probability of Mode 2 operation for a period of one year.

6.5 Summary and Conclusions

Among the many factors that influence the inherent reliability of an equipment are parts selection, parts application, circuit design, packaging, manufacturing and final test-

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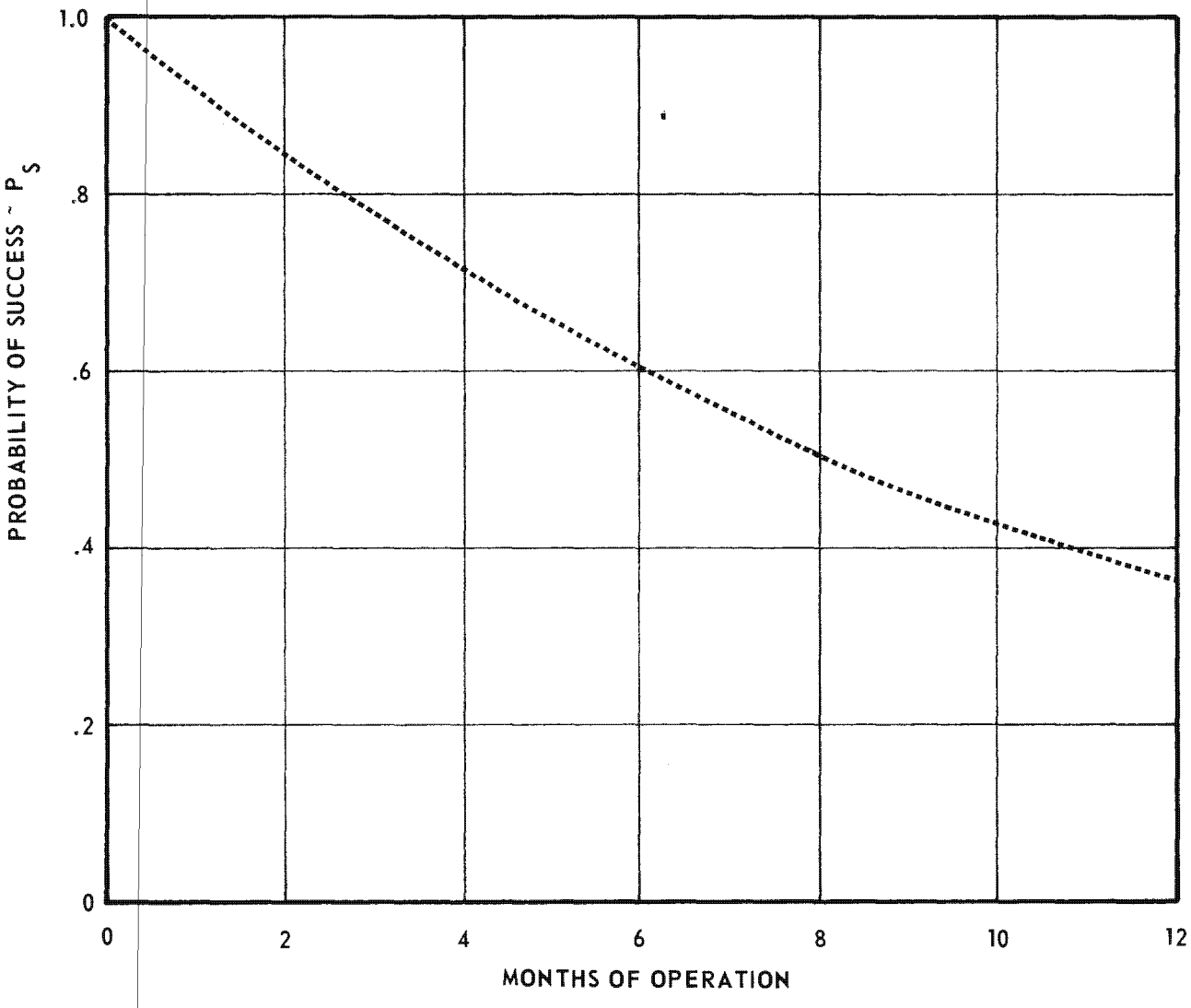

Figure 6.4-2. Probability Of Successful Operation In Mode 1

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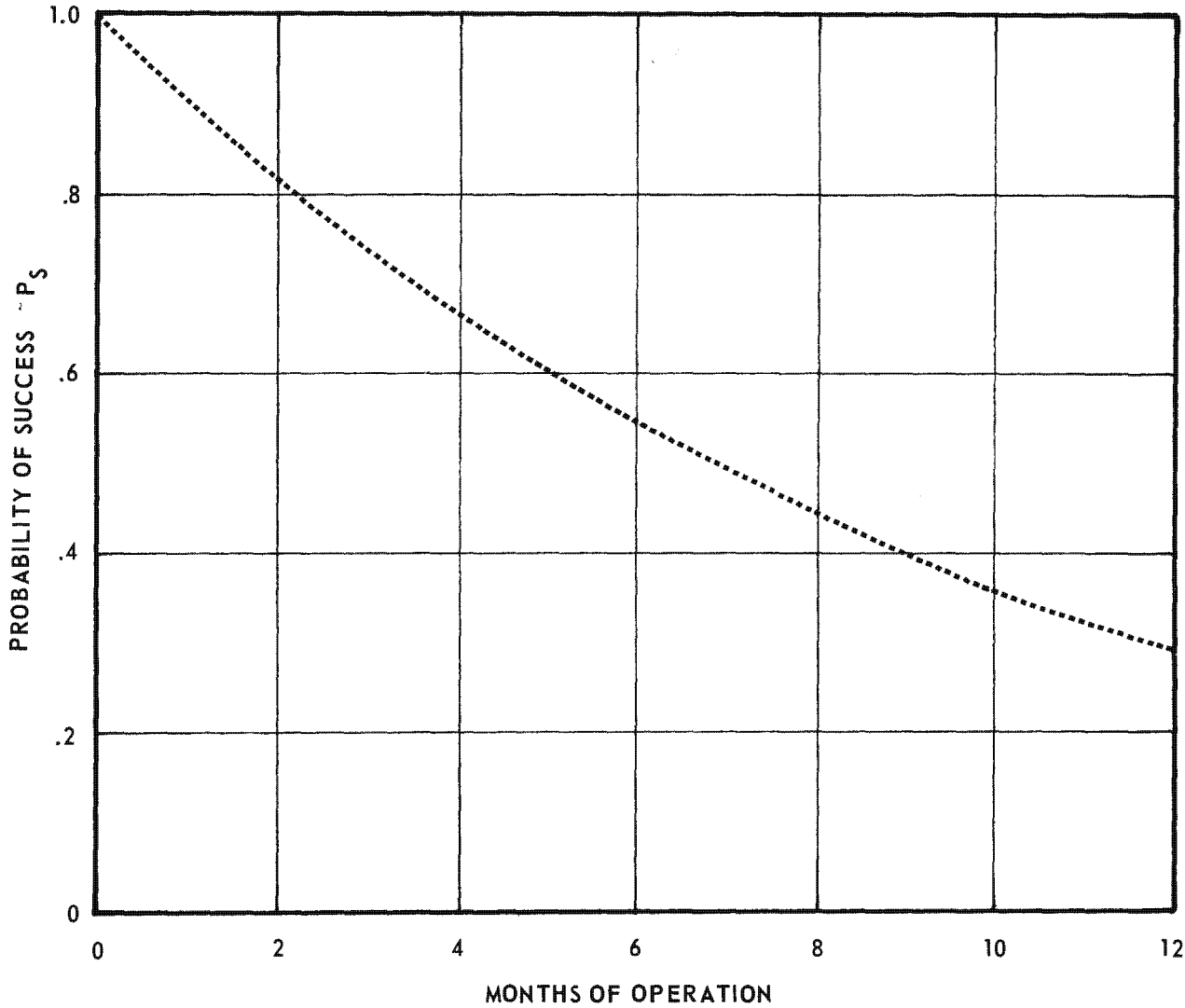

Figure 6.4-3. Probability Of Successful Operation In Mode 2

ing. When all of these factors have been carefully controlled the inherent reliability of an equipment is then directly a function of the complexity of the equipment with the application of redundancy the only remaining method of improving reliability.

Weight and power limitations prohibit the use of widespread redundancy within the system and the equally likely failure of so many different modules within the system negates localized redundancy.

Of the six factors mentioned above, all but two have already been discussed. These two are circuit design and final testing.

Many of the circuits used in this system are identical to circuits used in other systems that have demonstrated successful operation to show that they were reliable even without the use of conditioned parts. The use of the conditioned parts should extend the useful life of these circuits beyond the required mission duration.

There is some new circuitry and some innovations used in this system that are unproven in actual flight vehicles at this time. Notable in this area is the use of the solid state local oscillator. Although this device has no previous flight history, it was chosen for its simplicity and apparent high inherent reliability when compared with the reliability of a more complex, older type local oscillator.

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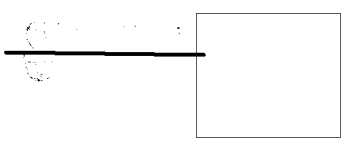
Testing in itself will not induce an otherwise unreliable equipment to be reliable. However, extensive testing has been and will continue to be conducted on the system and will establish that the design and the manufacturing process have combined to produce a system with high inherent reliability over the specified operating range.



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7.0 GROUND SUPPORT AND TEST EQUIPMENT

The ground support equipment for the Reaper system is required to provide the capability for system checkout and adjustment in a laboratory environment. The equipment includes 1) a system holding fixture, 2) cables and connections required to operate the system, 3) a Command and Control Console, 4) a line printer, 5) a Data Acquisition Console, 6) an RF Console, 7) a payload positioner and positioner control for range tests, and 8) a Range test facility for conducting the detailed system performance tests.

7.1 Functional Description

The primary function of the Ground Support Equipment is to provide a means of complete verification of the performance of the Reaper system. This verification is accomplished by conducting the following tests:

1) System Environmental Tests - These tests require the use of the Ground Support Equipment during the functional tests that are performed to determine the effect of the environmental conditions imposed upon the Reaper system.

2) Range Performance Tests - These tests require the use of the three consoles, the line printer, and the Range Test Facility for complete verification of the system performance.

3) Simulated Flight Tests - These tests are conducted by the Integrating Contractor during integration of the system and orbital vehicle.

To support these tests, the Ground Support Equipment provides the functions described in the following paragraphs.

7.1.1 Power Control

The Power Control Panel (Figure 7.1-1) is a part of the Command and Control Console. This panel provides control of power to the console and to the system, monitoring of the system main and auxiliary current and voltage, and accumulates operating time for the system. Voltage is adjustable over a range that is determined by the setting of the Lambda 103 power supply. Normally the range is 19 to 36 VDC. This adjustment controls both the system auxiliary voltage input level and the system main voltage level input.

Auxiliary current is monitored on a 0 to 5 ampere current meter that contains an adjustable upper limit control. If the upper limit of current is exceeded, both the auxiliary and main power will be turned off and a visual and an audible alarm will be initiated. The elapsed time meter that provides auxiliary power-on time in hours and tenths of hours, is turned off when the auxiliary power to the system is turned off.

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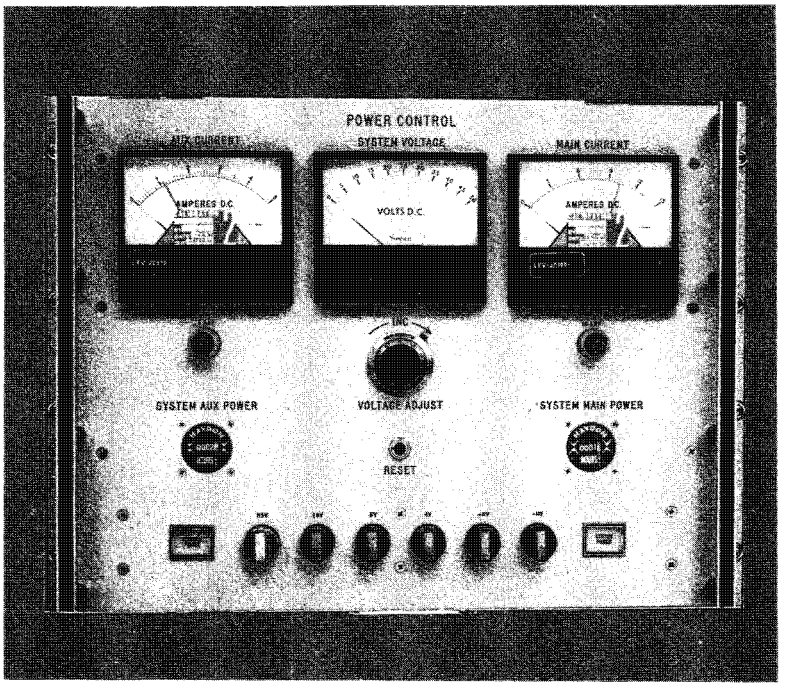

FIGURE 7.1-1 POWER CONTROL PANEL

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Main current is monitored on a 0 to 15 ampere current meter that contains an adjustable upper limit control. If the upper limit of main current is exceeded, the system main power will be turned off and a visual and audible alarm will be initiated. The elapsed time meter that provides main power-on time in hours and tenths of hours, is turned off when the main power to the system is turned off.

In case of an "excessive current cutoff" a reset switch restores power to the payload. This reset switch is also used to initially apply power if the System Power switch is actuated prior to actuating the Console Power switch.

7.1.2 Command and Control

The C&C (Command and Control) panel is a part of the Command and Control Console. See Figure 7.1-2. This panel is the source of all system commands, attitude inputs, change frequency controls, Time inputs, and DSU status controls.

7.1.2.1 Normal Stored Program Commands

Forty-eight of the 60 payload commands are controlled by the NSPC (Normal Stored Program Command) section of the C&C panel. Eight electrically interlocked switches (Command Select) and eight momentary action switches (Command Operate) are utilized in a matrix to issue the 48 commands. Table 7.1-1 gives the switch combinations required to issue the payload commands. The commands controlled by the command

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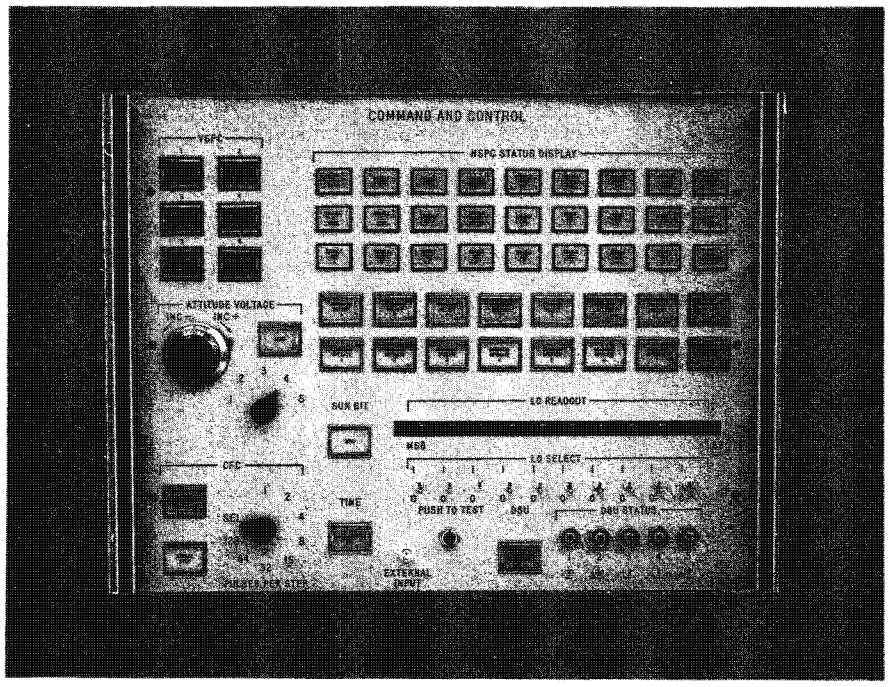

FIGURE 7.1-2 COMMAND AND CONTROL PANEL

TABLE 7.1-1

NSPC COMMANDS

GSE COMMAND SELECT	GSE COMMAND OPERATE	P/L COMMAND NUMBER	COMMAND FUNCTION
A	1	R11	Payload On
A	2	R13	Readin On
A	3	-	Not Used
A	4	-	VSPC Enter
A	5	-	Enable Rec & PS R/O (GSE Cmd.)
A	6	R51	Enable Rec & PS R/O
A	7	R14	Readin Off
A	8	R12	Payload Off
B	1	R18	Disable Memories
B	2	R19	Disable FOV Inhibit
B	3	R20	Disable Tmin Confirm
B	4	R21	Disable Tmax Inhibit
B	5	R22	Disable A/R Inhibit
B	6	R23	Disable Real/Image Confirm
B	7	R24	Disable PW Confirm
B	8	R25	Disable Freq. Confirm
C	1	R15	Disable Upper Freq. Band
C	2	R16	Disable Lower Freq. Band
C	3	R27	Disable CW - SI
C	4	R29	Disable Rec. Buffer

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TABLE 7.1-1 (Continued)

NSPC COMMANDS

GSE COMMAND SELECT	GSE COMMAND OPERATE	P/L COMMAND NUMBER	COMMAND FUNCTION
C	5	R50	Disable Rec & PS R/I
C	6	R32	Disable RF Calibrator
C	7	R52	Disable Rec/PS R/O
C	8	R26	Reset Cmd Sel B Disables (Reset R18 through R25)
D	1	R17	Enable Upper & Lower Freq. Bands
D	2	R28	Enable CW - SI
D	3	R30	Enable Rec Buffer
D	4	R31	Enable RF Calibrator
D	5	-	Enable Rec. Input Mode (GSE Command)
D	6	-	Enable PS Input Mode (GSE Cmd)
D	7	R49	Enable Rec. Input Mode
D	8	R61	Enable PS Input Mode
E	1	R34	Disable Rec Set A
E	2	R36	Disable Rec Set B
E	3	R38	Disable Rec Set C
E	4	R40	Disable Rec Set D
E	5	R42	Disable Rec Set E
E	6	R44	Disable Rec Set F
E	7	R46	Disable Rec Set G

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TABLE 7.1-1 (Continued)

NSPC COMMANDS

GSE COMMAND SELECT	GSE COMMAND OPERATE	P/L COMMAND NUMBER	COMMAND FUNCTION
E	8	R48	Disable Rec Set H
F	1	R33	Enable Rec Set A
F	2	R35	Enable Rec Set B
F	3	R37	Enable Rec Set C
F	4	R39	Enable Rec Set D
F	5	R41	Enable Rec Set E
F	6	R43	Enable Rec Set F
F	7	R45	Enable Rec Set G
F	8	R47	Enable Rec Set H
G	1	R53	Rec Threshold Bit A "1"
G	2	R54	Rec Threshold Bit B "1"
G	3	-	Not Used
G	4	R58	Time Reset
G	5	-	Not Used
G	6	-	Not Used
G	7	R62	Rec Threshold Bit A "0"
G	8	R63	Rec Threshold Bit B "0"
H	1	-	Not Used
H	2	-	Not Used
H	3	-	Not Used

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Page 6

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TABLE 7.1-1 (Continued)

NSPC COMMANDS

GSE COMMAND SELECT	GSE COMMAND OPERATE	P/L COMMAND NUMBER	COMMAND FUNCTION
H	4	-	Not Used
H	5	-	Not Used
H	6	-	Not Used
H	7	-	Not Used
H	8	-	Not Used

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select switches are grouped in categories to provide an efficient commanding system. The groups (or categories) are as follows:

1) Command Select A - These commands place the system in operation or turn it off. Also the Recognizer/Partial Scan Memory readout is controlled.
2) Command Select B - These commands basically control the system confirm-inhibit logic.
3) Command Select C - These commands are system function disables. Also the reset command for the confirm-inhibit disable commands is provided.
4) Command Select D - These commands are basically the enable commands for those functions disabled by command select C.
5) Command Select E - These commands are the recognizer memory set disables.
6) Command Select F - These commands are the recognizer memory set enables.
7) Command Select G - These commands provide control of the recognizer threshold and provide a time reset for the system time accumulator.
8) Command Select H - These are unused to allow for expansion.

This grouping of commands prohibits issuing conflicting commands (enable, disable) simultaneously except for the case of placing the system in operation; in which case it might be desirable to have the capability of immediately turning the system off.

7.1.2.2 Variable Stored Program Commands

Twelve of the 60 payload commands are controlled by the VSPC (Variable Stored Program Command) section of the C&C panel. Six alternate action switches are used to program six parallel entry commands to the system. Each switch is labeled "Send 1," "Send 0," "Rcvd 1," and "Rcvd 0." Switch operation causes either the Send 1 or Send 0 to be set up. An entry into the system is initiated by a command from the NSPC section (Command Select A, Command Operate 4). Table 7.1-2 gives the switch positions required to issue the 12 payload commands.

7.1.2.3 Command Status Display

Status of the 48 payload commands issued through the GSE NSPC function is displayed on 27 lamps on the C&C panel. The status of each command is in the state indicated on the lamp front when the lamp is lighted. Status of the 12 payload commands issued through the GSE VSPC function is indicated by the "Rcvd 1" and "Rcvd 0" VSPC switch lamps. These lamps are lighted by monitoring the T/M lines out of the payload and lighting the appropriate lamps indicating what commands the system received.

TABLE 7.1-2

VSPC COMMANDS

VSPC SWITCH NO.	SWITCH POSITION	P/L COMMAND NUMBER	COMMAND FUNCTION
1	"1"	R1	Increase Dwell Time
1	"0"	R2	Decrease Dwell Time
2	"1"	R9	Recognizer Enable
2	"0"	R10	Recognizer Disable
3	"1"	R5	Threshold Control A
3	"0"	R6	Threshold Control $\overline{A}$
4	"1"	R7	Threshold Control B
4	"0"	R8	Threshold Control $\overline{B}$
5	"1"	R3	Partial Scan A On
5	"0"	R4	Partial Scan A Off
6	"1"	R59	Partial Scan B On
6	"0"	R60	Partial Scan B Off

7.1.2.4 Attitude Voltage

Attitude voltage (Pitch and Roll) supplied to the system is controlled on the C&C panel. The pitch and roll voltage is controlled by a selector switch to provide the following voltages:

a) Pitch and Roll both variable between +11 volts and -11 volts.

b) Pitch fixed at -11 volts, Roll variable between +11 volts and -11 volts.

c) Pitch variable between +11 volts and -11 volts, Roll fixed at +9.92 $\pm$ .78 volts.

d) Pitch fixed at +9.92 $\pm$ .78 volts, Roll variable between +11 volts and -11 volts.

e) Pitch variable between +11 volts and -11 volts, Roll fixed at -11 volts.

A "Lost Horizon" signal can also be supplied to the system by the C&C panel.

7.1.2.5 Time

The time signal input to the system is controlled on the C&C panel. The GSE provides a choice between a fixed 8 PPS signal to the payload and an external time signal input. External input pulses must have the following characteristics:

Source Impedance	50 ohms
Input Voltage	1.0 to 4.0 volts
Rise Time	0.4 to 0.5 usec

Pulse Width	10 ± 5 usec
Frequency	0 to 24 kHz

7.1.2.6 DSU Status

A lamp on the C&C panel indicates when the system has requested the use of a DSU. A DSU available signal control switch on the C&C panel allows an operator to provide the available signal to the system.

The C&C panel also provides control of the five DSU status bits into the system. The status bits are as follows:

Switch No.	Function
1	Thresher Recognizer Enable/Disable
2	Reaper Recognizer Enable/Disable
3	DSU R/I
4	Reaper DSU Select
5	DSU Steady State Actuate

7.1.2.7 Change Frequency Command

The C&C panel provides control and monitoring of the system local oscillator, either for automatic operation or manual operation. With automatic CFC (Change Frequency Command) selected, the system utilizes its own internally generated CFC pulses. With manual CFC selected, the system internal CFC pulses are inhibited and pulses are entered into the system by operation of the manual switch. The number of pulses entered into the system per operation of the manual switch may be selected by the operator. This selection pro-

vides 1, 2, 4, 8, 16, 32, 64, or 128 local oscillator steps for each manual switch operation. Also, the operator may choose to select any of the Reaper local oscillator frequency steps by setting in the ten-bit code of the local oscillator step desired. Ten lamps are provided which monitor the system local oscillator frequency telemetry lines. In the local oscillator frequency select mode, CFC pulses are sent to the system until the local oscillator readout exactly matches the selected frequency. When the match is made, the CFC pulses stop and the system remains on the selected frequency.

7.1.3 Data Monitoring

System data monitoring is provided by the command and control console. The following types of data are available from the payload for monitoring:

a) EOB Data - 182 bit digital

b) Status Words - 182 bit digital

c) Marker Words - 48 bit digital

d) Pre-Detected Data - 0.5 MHz to 5.5 MHz Analog

e) Telemetry Data - Analog voltages and discrete levels

7.1.3.1 EOB Data Monitoring

The system EOB data is monitored on the BRO (Binary Readout) panel (See Figure 7.1-3) and on the DRO (Decimal Readout) panel (See Figure 7.1-4). A selector switch is provided so that the EOB data may be monitored directly from the system, as it comes out of the core (part of the data recording unit,

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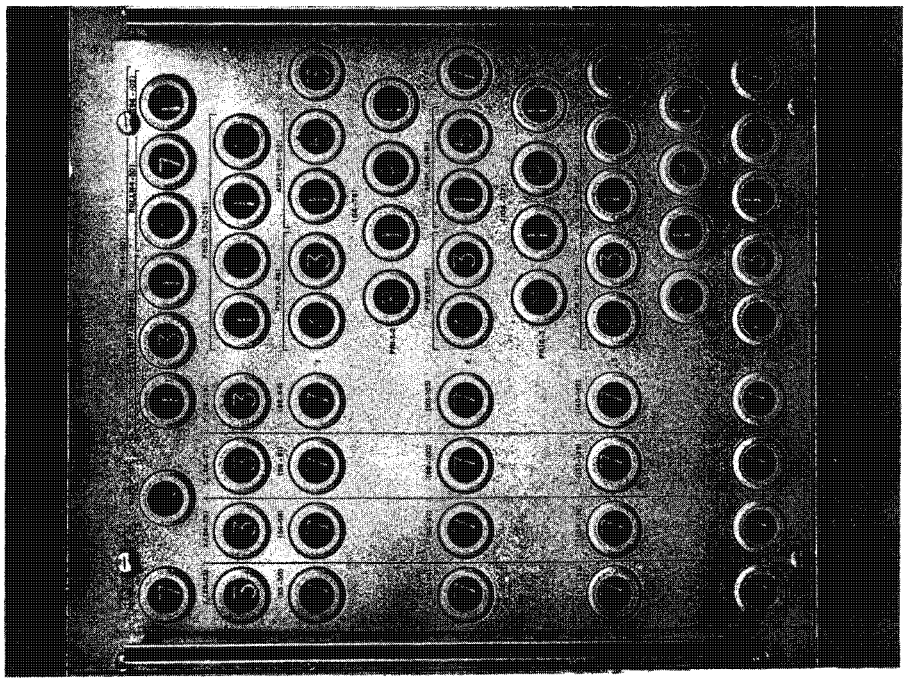

FIGURE 7.1-4 DECIMAL READOUT PANEL

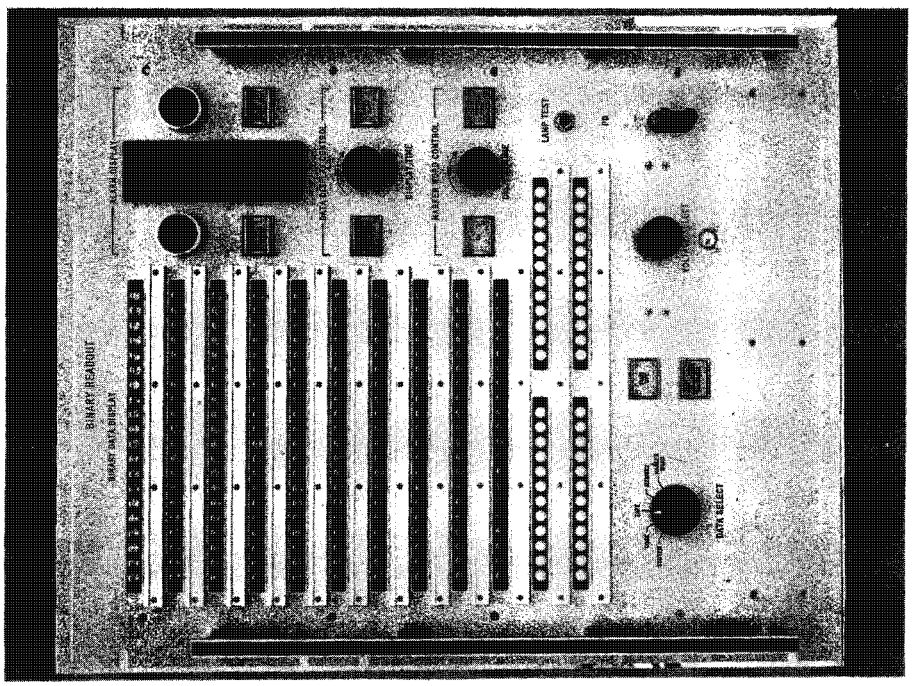

FIGURE 7.1-3 BINARY READOUT PANEL

see paragraph 7.1.4), or as it is played back from the magnetic tape (see paragraph 7.1.4). The real-time data out of the system and the data out of the core is sampled and displayed at a rate selected on the BRO panel. The data display from the magnetic tape is a display of each data word recorded on the tape.

7.1.3.2 Status Word Monitoring

The system status words (start, stop, and time-attitude words) are displayed on the BRO and partially on the DRO. The decimal display consists only of pitch, roll, word ID, and CW bit. All other parts of the status words are displayed only on the binary panel.

7.1.3.3 Marker Word Monitoring

The Marker Words from the system may be displayed in binary form on the BRO panel. The data is sampled, for display, at a rate determined by operation of the display time control on the BRO panel.

7.1.3.4 Pre-Detected Data Monitoring

The system pre-detected video signal is available on the front panel of the BRO panel. This signal may be monitored on an oscilloscope in the Command and Control Console.

7.1.3.5 Telemetry Data Monitoring

The system T/M (telemetry) data is monitored on a DVM (digital voltmeter). The T/M data monitor Control (See Figure 7.1-5) provides a selection of either automatic scanning

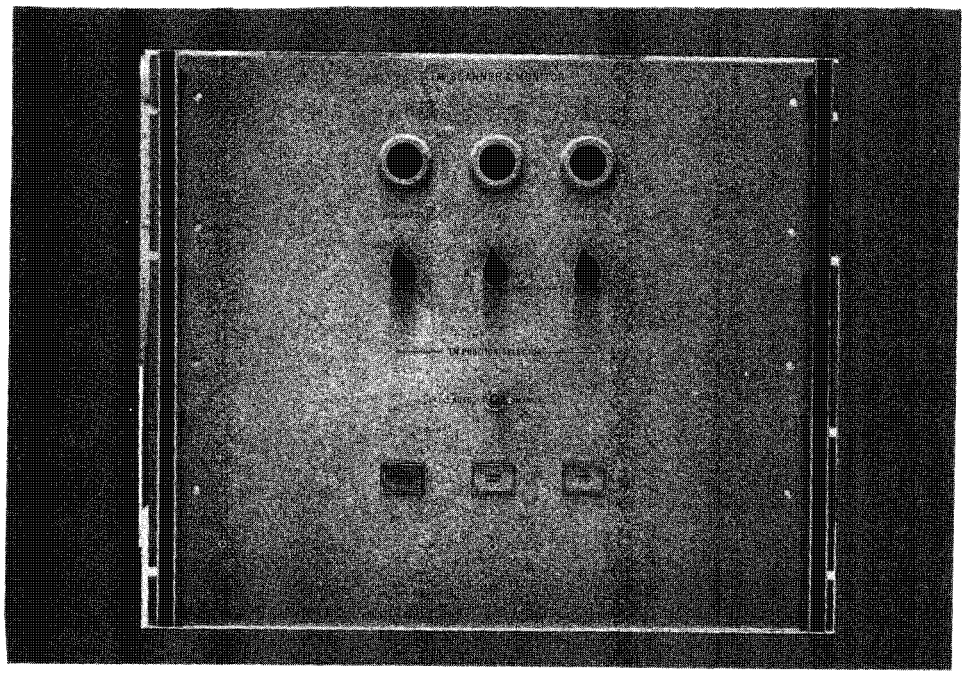

FIGURE 7.1-5 T/M SCANNER

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of the T/M points or manual selection of the desired point. The T/M point number and the voltage level of that T/M point is displayed.

In the automatic scan mode each of the 160 T/M points is sampled and displayed in sequence. If one of the sampled T/M points is not within the acceptable limits for that particular point, the automatic scan stops and visual and audible alarms are turned on (see paragraph 7.1.6).

7.1.4 Data Recording

The system EOB data and status words may be recorded for later analysis on the GSE equipment or by a computer. The data is recorded on magnetic tape (See Figure 7.1-6). The system data output rate is not compatible with the input data rate of the magnetic tape unit so a buffer storage unit is inserted between the data source and the magnetic tape unit. This buffer storage unit is a core memory that is read out at a rate that is compatible with the magnetic tape input.

7.1.5 Data Printing

The following system data may be printed on the GSE line printer (See Figure 7.1-7):

a) EOB data and Status Words

b) Marker Words

c) Recognizer/Partial Scan Memory Contents

d) Telemetry Data

The printing of data is controlled by the Printer Control Panel. See Figure 7.1-8.

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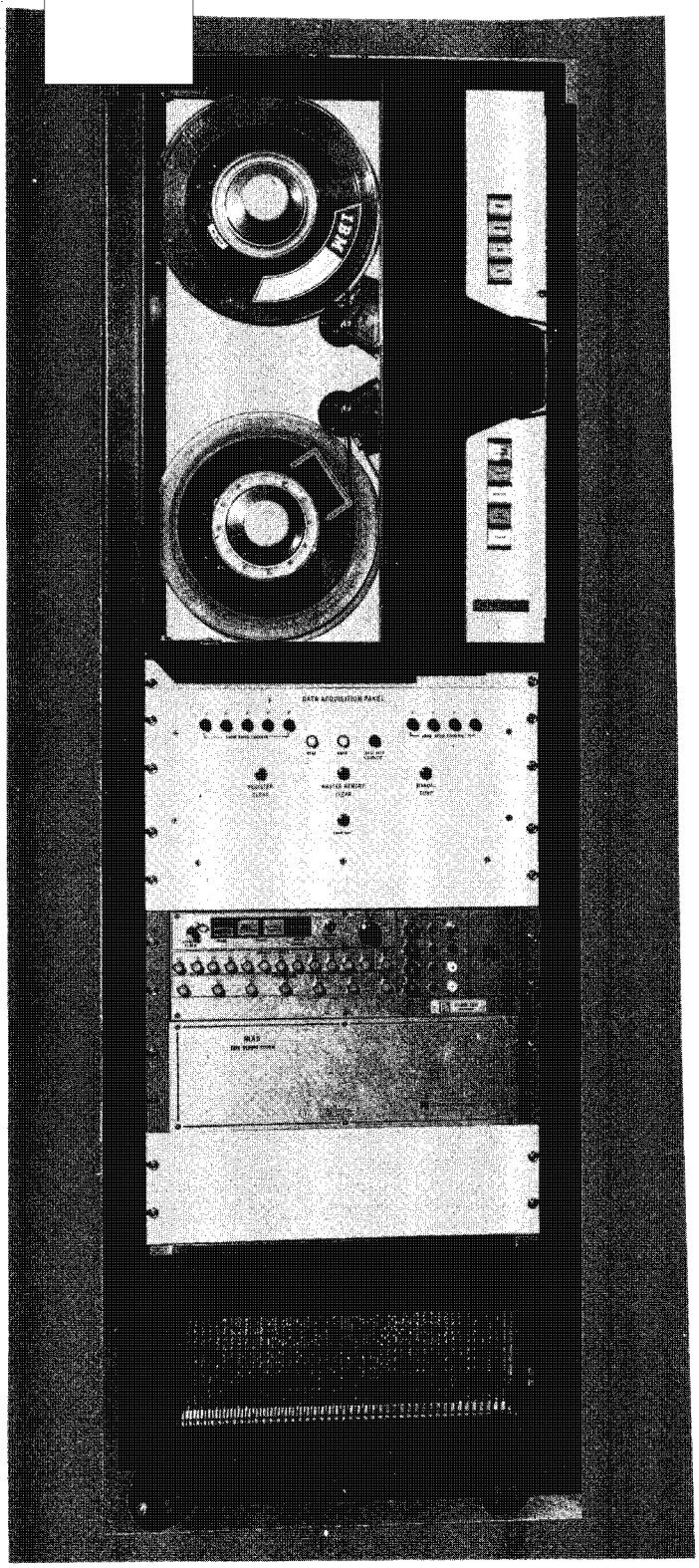

FIGURE 7.1-6 DATA ACQUISITION CONSOLE

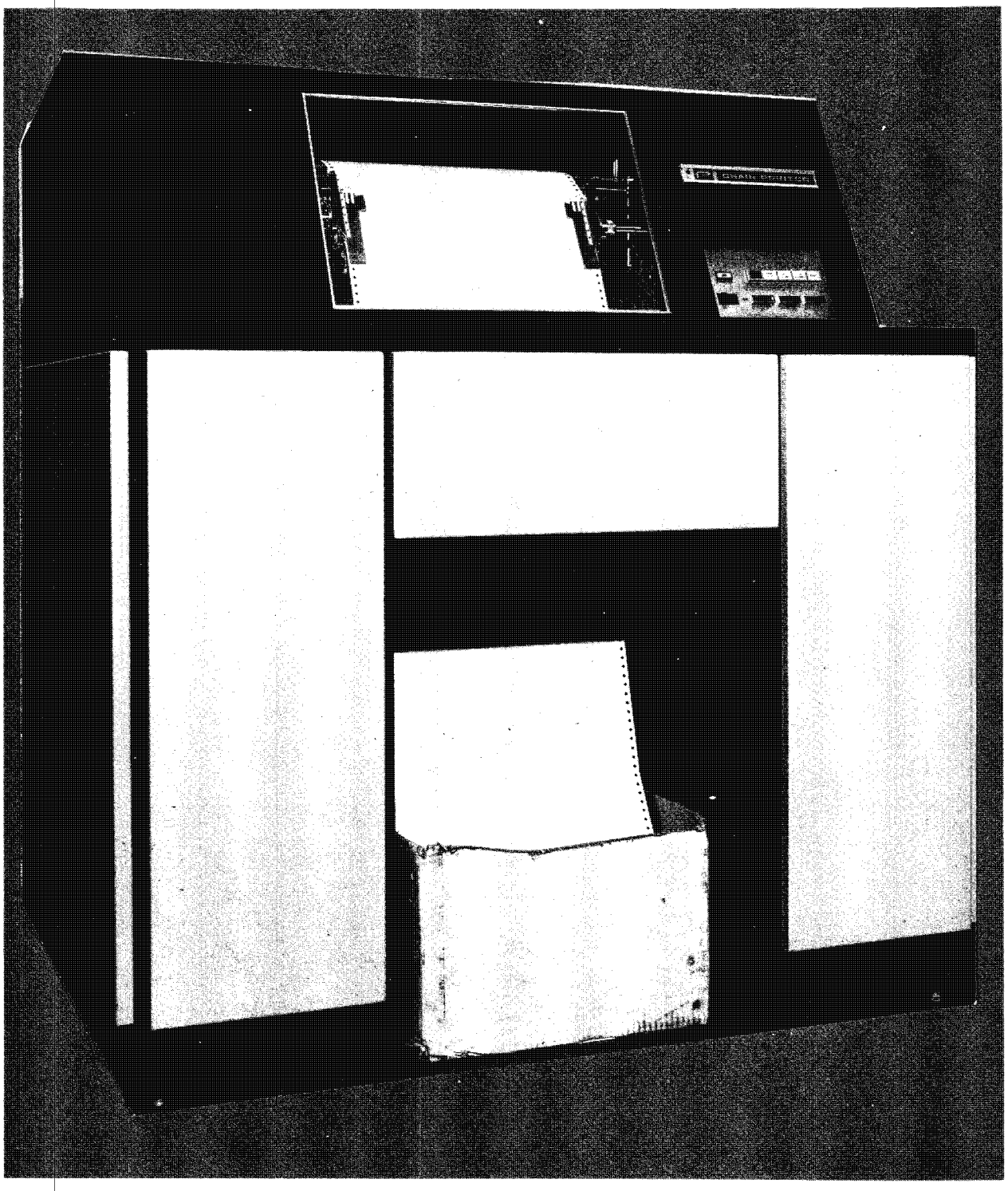

FIGURE 7.1-7 PRINTER

7.1.5.1 EOB and Status Data Printing

The EOB data may be printed only as it is played back from the magnetic tape unit. A selector switch allows the operator to print the EOB data either in decimal or binary. Status words are always printed in binary form regardless of the form selected for EOB data. The EOB decimal printing is a decimal equivalent of the payload binary output codes. Decimal printing in engineering units must be obtained from computer processing.

7.1.5.2 Marker Word Printing

Marker words are printed in real-time from the system. This printing is in binary form and is the only method of recording the system marker words.

7.1.5.3 Recognizer/Partial Scan Memory Printing

The contents of the Recognizer and Partial Scan memories is printed in binary form in real-time from the system. This binary word is 484 bits long and represents the partial scan frequency limits and the parameters set into the 8 system parameter sets.

7.1.5.4 Telemetry Data Printing

The printing of the system T/M data is in real-time and includes the T/M number, the voltage level, the upper limit allowed for each point and the lower limit for each point. A switch allows a selection of "full scan" or "continuous." The full scan mode causes all 160 T/M points to be scanned and

printed one time. In the continuous mode, all 160 T/M points are printed, in sequence, over and over until the printing is manually stopped.

If any of the T/M points are out of tolerance (above upper limit or below lower limit) a note is printed to indicate that the point was out of tolerance and whether it was high or low.

7.1.6 Error Detecting

The GSE provides an error detecting function and indicates the error by audible and/or visual alarm (See Figure 7.1-3). The visual alarms on the BRO panel indicate the following errors have been detected:

a) Parity 1 - Indicates a parity error in the first 65 bits of the 182 bit system output word.

b) Parity 2 - Indicates a parity error in bits 66 through 104 of the 182 bit system output word.

c) Parity 3 - Indicates a parity error in bits 105 through 143 of the 182 bit system output word.

d) Parity 4 - Indicates a parity error in bits 144 through 182 of the 182 bit system output word.

e) Power Aux. - Indicates a system auxiliary and main power cut-off due to excessive auxiliary current being used by the system.

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f) Power Main - Indicates a system main power cutoff due to excessive main current being used by the system.

g) Telemetry - High - Indicates a TM point has exceeded the + tolerance as set into the upper limit/lower limit matrix.

h) Telemetry - Low - Indicates a TM point has exceeded the - tolerance as set into the upper limit/lower limit matrix.

i) Redundant Data - Indicates a difference in the data located in bit positions 4 through 26 and the data in bit positions 108 through 130, or the data in bit positions 37 through 43 and the data in bit positions 89 through 95, or the data in bit positions 44 through 50 and the data in bit positions 96 through 102 for status words.

There are nine more error lamps on the BDM/DTU (Binary Digital Module/Digital Telemetry Unit) Simulator panel. These lamps indicate errors in Recognizer/Partial Scan Memory Contents when the data is read out.

7.1.7 Recognizer/Partial Scan Memory Loading

The BDM/DTU Simulator (Figure 7.1-9) provides the capability of loading and reading out the system recognizer and partial scan memories. For memory loading, there are 402

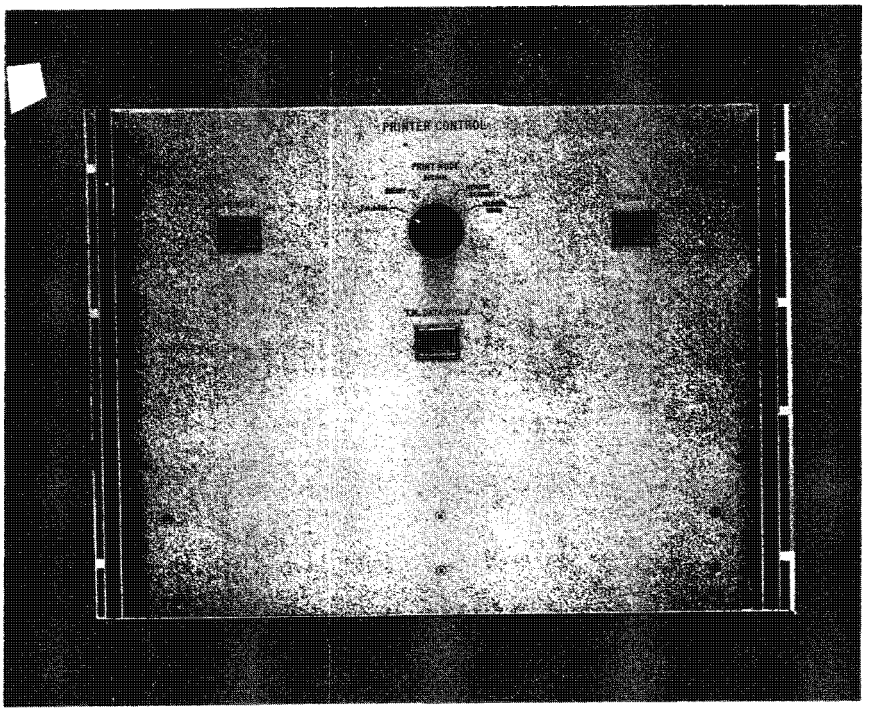

FIGURE 7.1-8 PRINTER CONTROL PANEL

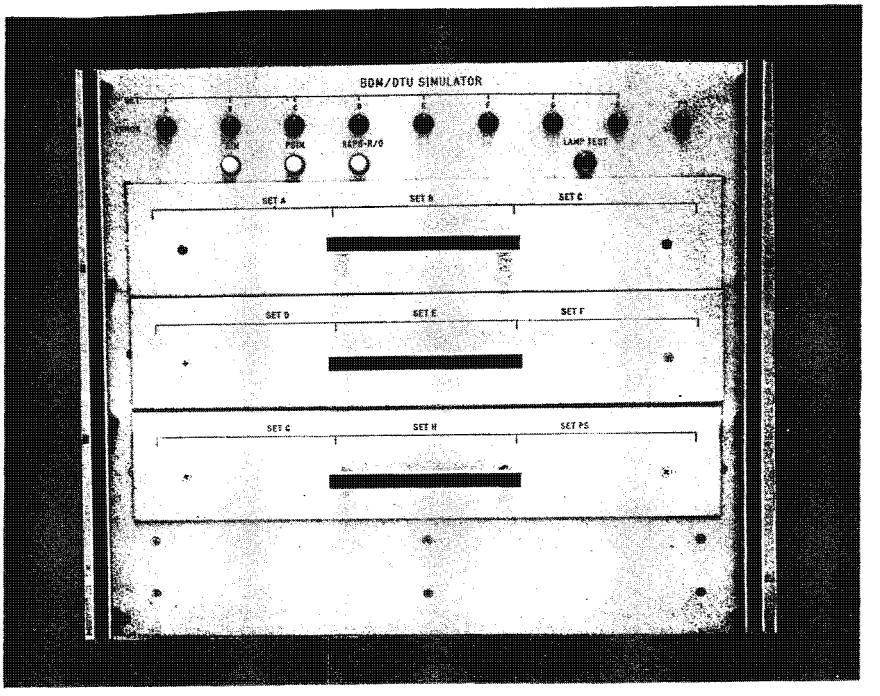

FIGURE 7.1-9 BDM/DTU PANEL

switches that allow programming of the memories. Thirty-six switches are used in programming the frequency limits in the partial scan memory and each recognizer set has 47 switches and 9 pre-wired zeros. Front panel lamps indicate that data has been read into the recognizer memory, into the partial scan memory, or out of the recognizer/partial scan memories.

7.1.8 RF Signal Input

The RF signals required for testing the Reaper operation are provided by the RF console (See Figure 7.1-10). Signals are provided for system tests in a laboratory or on a simulated free-space test range.

7.1.8.1 RF Signals in a Laboratory

The RF console provides two RF sources to the system. The phase shifter panels provide a means of adjusting the phase of the signal to simulate different angles of arrival of the signals. An attenuator in the channel F-2 line provides a means of adjusting the amplitude of channel F-2 relative to channel C (A/R inhibit channels).

7.1.8.2 RF Signals on the Range

The RF consoles are used during range tests to provide two signal sources through the range source antenna (See Figure 7.1-11). The phase shift panels are not used in range tests. The signals are fed through air dielectric coax from the test building to the source antenna and then transmitted through "free-space" back across the 575 foot range.

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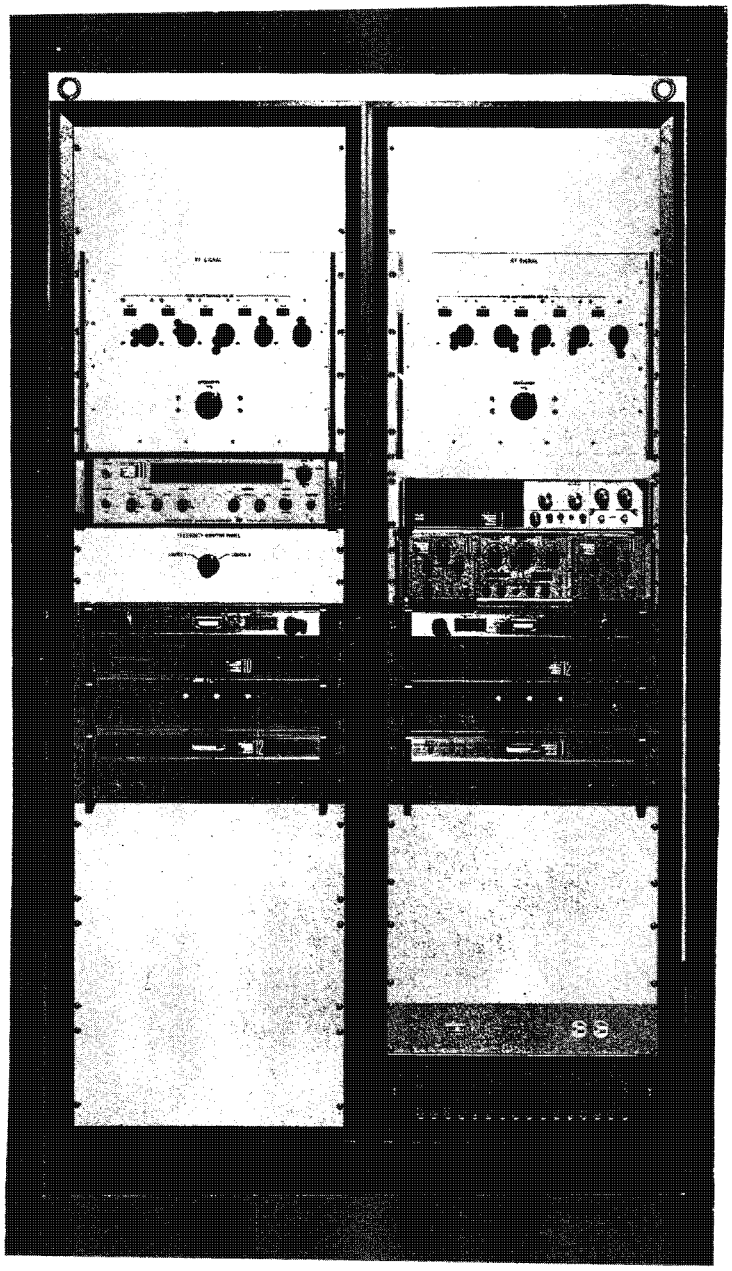


FIGURE 7.1-10 RF CONSOLE

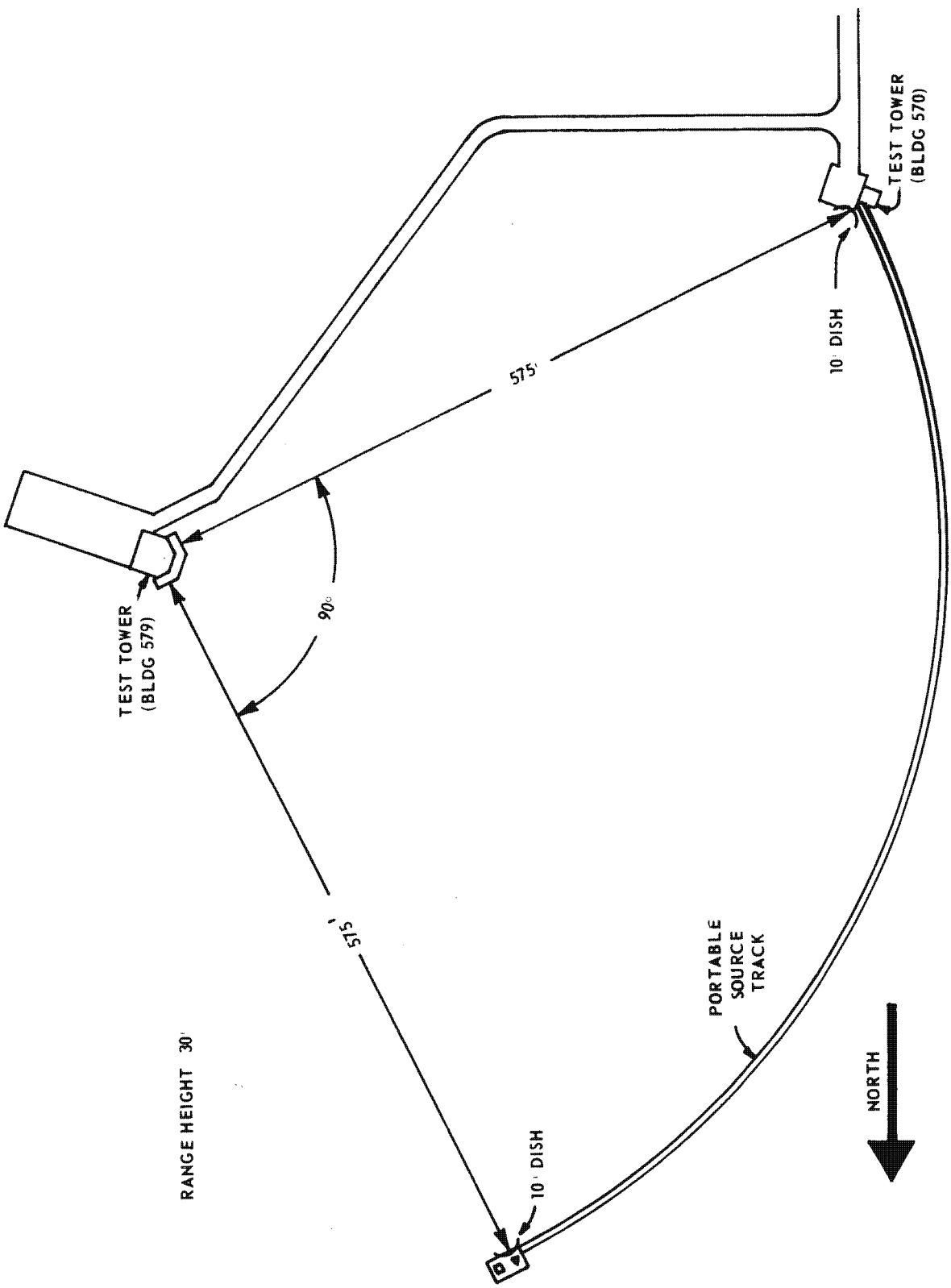


Figure 7.1-11. Test Range Plan View

[redacted]

50X1

7.1.9 RF Parameter Digitization

The parameters of the RF signals being inserted into the system are converted to digital form by the RF Digitization Section of the RF Console (See Figure 7.1-12). The parameters digitized are:

a) Frequency - 100 kHz resolution, ± 100 kHz accuracy

b) Pulse Repetition Interval - 1 usec resolution, ±1 usec accuracy

c) Pulse Width - 125 usec resolution, ±250 usec accuracy

d) Amplitude - 2.5 db resolution, ±3 db accuracy

e) Phase -

Phase Shifters: 0.1 degree resolution, ±0.1 degree accuracy

Range: 0.03 degree resolution, ±0.03 degree accuracy

f) Time - Payload time as sampled from the payload telemetry lines

The output of the RF digitization section is available in two forms. A 3-LRZ (three-level return to zero) signal that has a 10 kHz bit rate will drive 300 feet of RG-59 cable terminated in 75 ohms. The word is 148 bits long. The word content includes permanent "zero" bits sufficient to allow data output to represent a 4-bit BDC character for each 4 bit read-out.

There is also a punched paper tape output. The paper tape is primarily for use during tests at LTV.

50X1

[redacted]

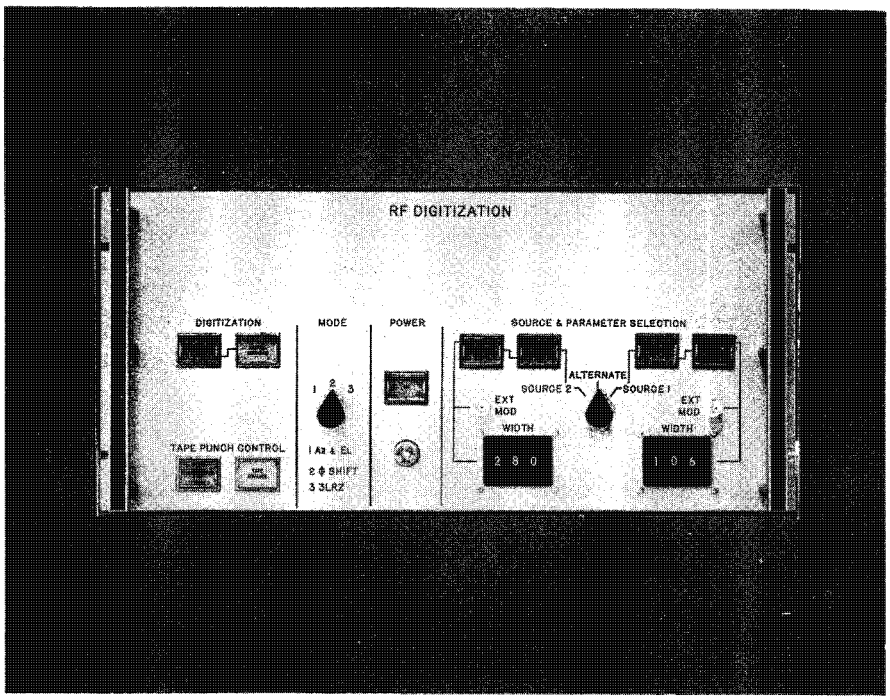


FIGURE 7.1-12 RF DIGITIZATION PANEL

7.2 Description of Equipment

The ground support equipment designed to provide the functions described in paragraph 7.1 is contained in three consoles, a line printer, and a holding fixture as shown in Figures 7.2-1 and 7.2-2. Figure 7.2-3 shows the block diagram of the equipment excluding the RF console.

7.2.1 Command and Control Console

The command and control console contains the following panels:

1) Binary Readout (BRO)
2) Printer Control (PC)
3) T/M Scanner and Monitor (T/M)
4) T/M Upper Limit/Lower Limit Diode Matrix
5) Power Control
6) Decimal Readout (DRO)
7) Command and Control (C&C)
8) BDM/DTU Simulator
9) HP 3460B Digital Voltmeter (DVM)
10) Tektronix RM547 Oscilloscope
11) Lambda LE103 Power Supply
12) Fans (2)
13) Main Power (2)

7.2.2 Data Acquisition Console

The data acquisition console is an Ampex Tape Memory Console with two auxiliary units installed. The console

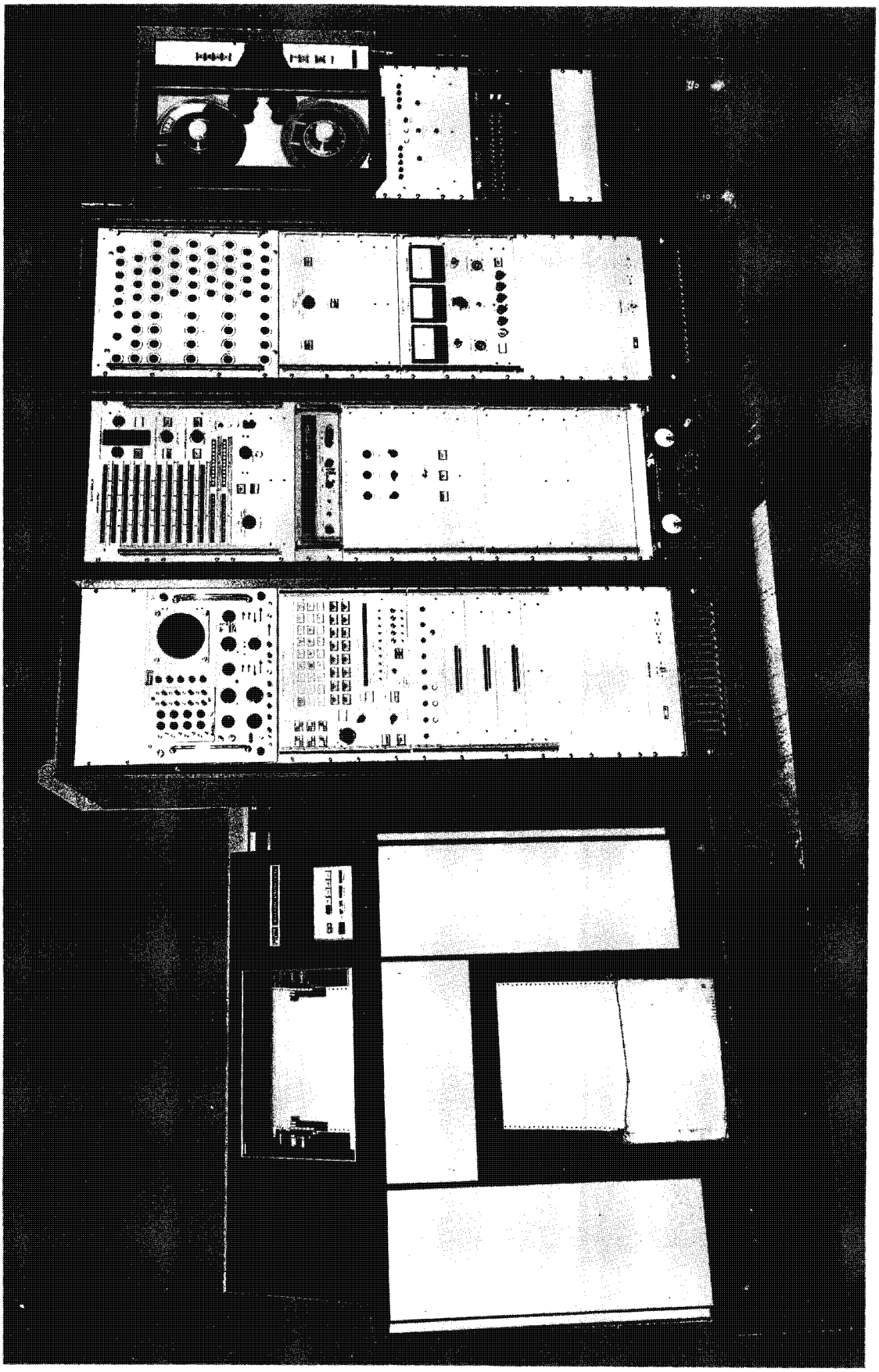
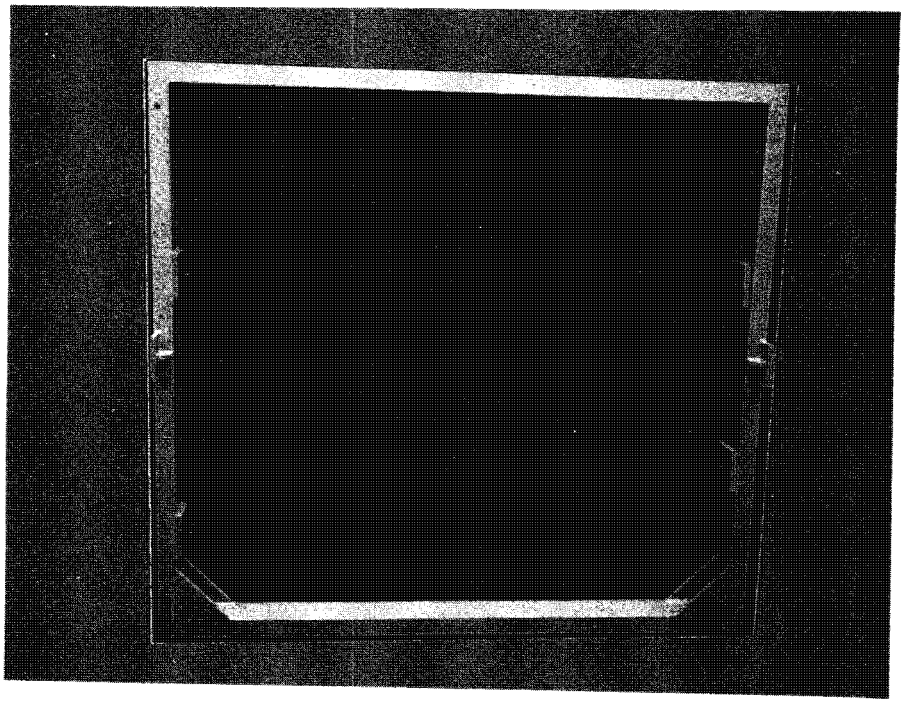


FIGURE 7.2-1 GROUND SUPPORT EQUIPMENT

50X1



7.2-2 HOLDING FIXTURE

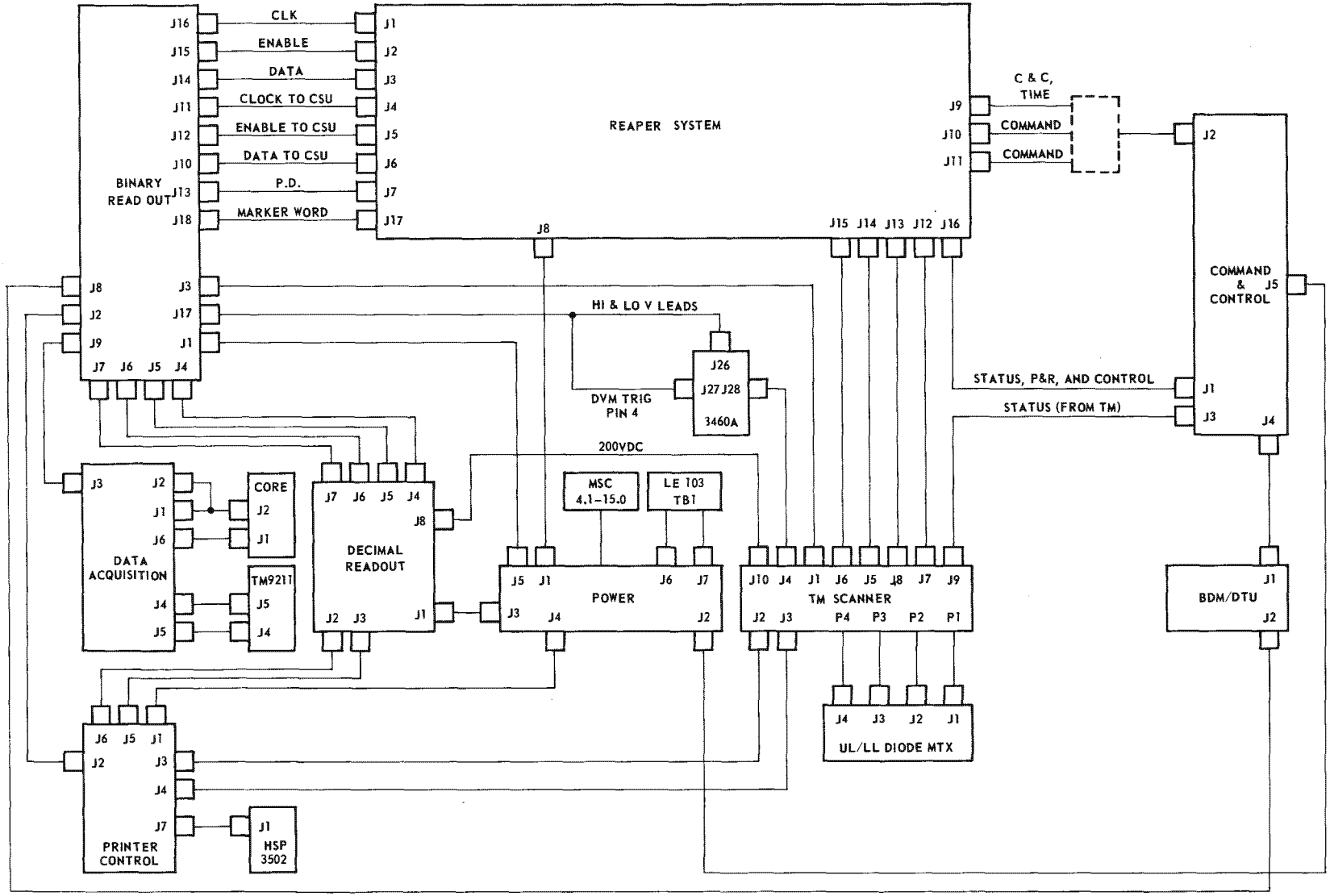


Figure 7.2-3. Block Diagram

contains the following:

1) Data Acquisition Unit
2) Fabritek MLA5 Core Memory
3) Ampex TM9211 Tape Recorder

7.2.3 Printer

The printer is a Potter HSP3502 chain printer.

7.2.4 RF Console

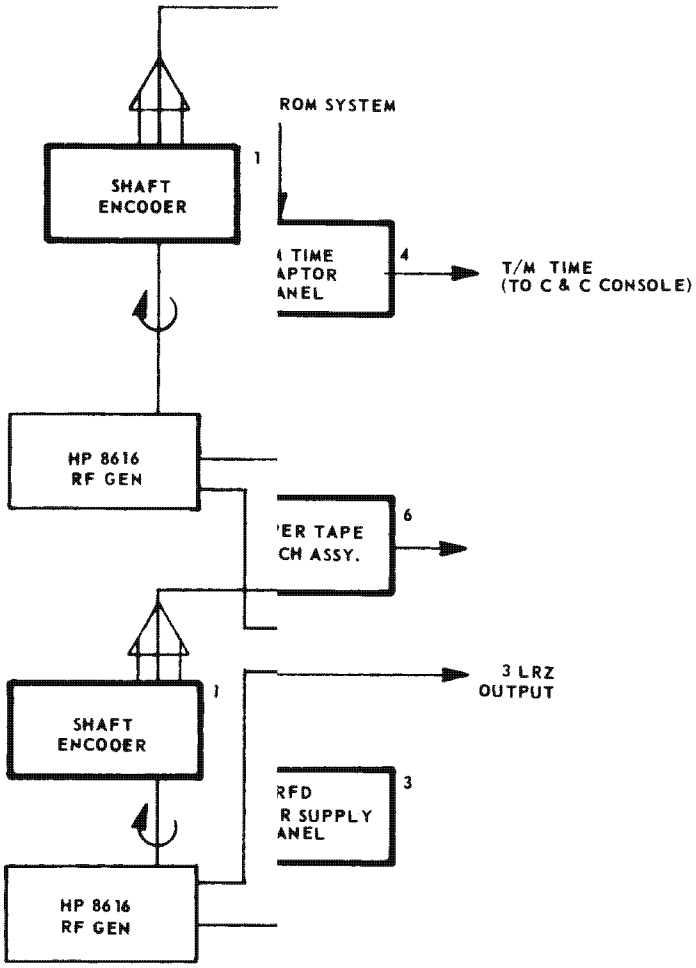
The RF console contains the following equipment:

1) HP8616A RF Signal Generator (2)
2) HP8403 Modulator (2)
3) HP491C TWT Amplifier (2)
4) Eldorado 950 Frequency Counter
5) Monsanto 1010 Counter/Timer
6) Data Pulse 103 Pulse Generator
7) Invac P135 Tape Punch
8) RF Signal (Phase Shifter Panels) (2)
9) RF Digitization (RFD)
10) Fans (2)
11) Main Power

Figure 7.2-4 is a block diagram of the RF console and Figure 7.2-5 is a block diagram of the RF path in the phase shifter panels.

7.2.5 Positioner and Positioner Control

The positioner and positioner control (See Figure 7.2-6) are used during the Reaper range tests to position



7.2-4. RF Console Block Diagram

SECRET
SPECIAL HANDLING

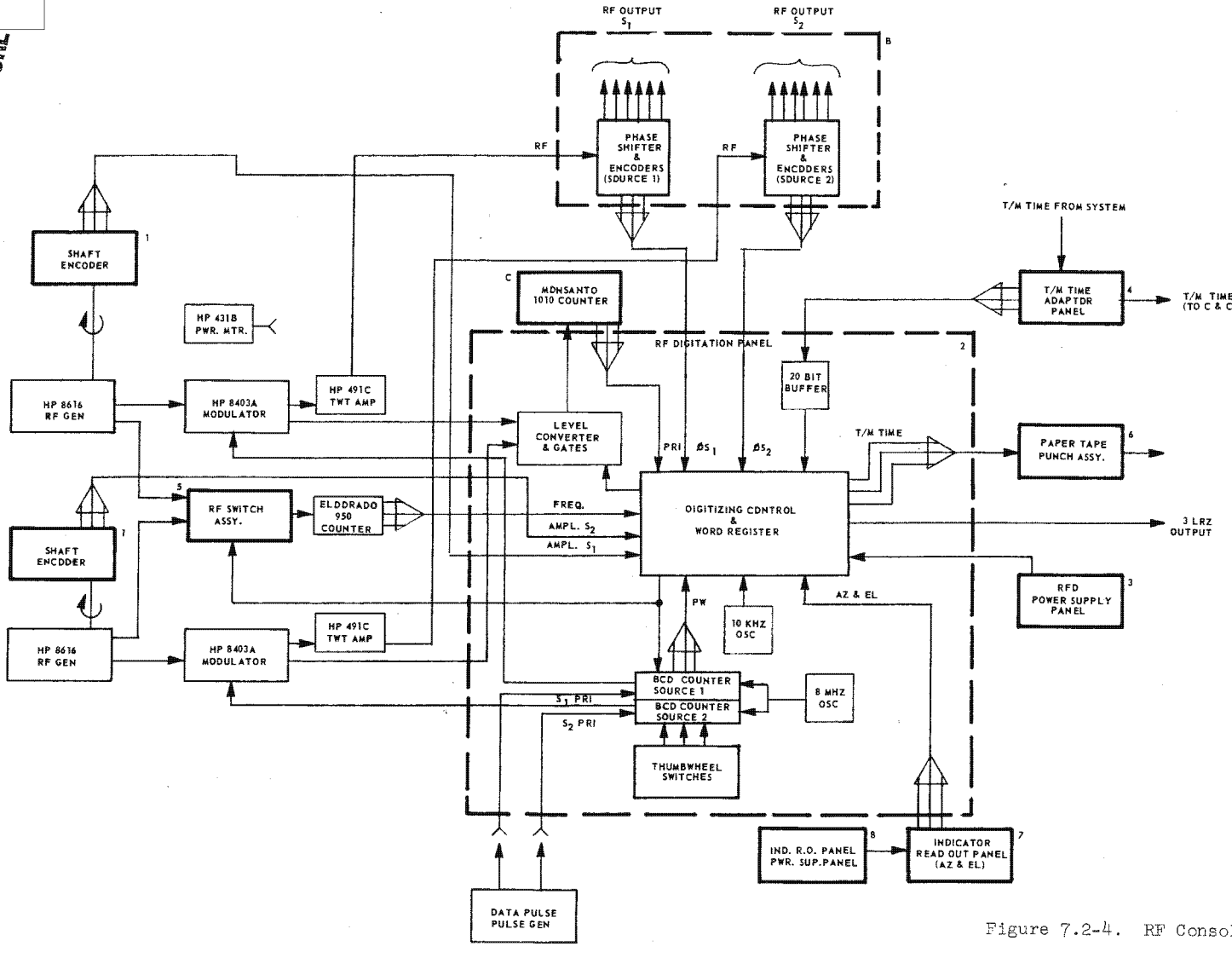


Figure 7.2-4. RF Console Block Diagram

SECRET
SPECIAL HANDLING

Approved for Release: 2017/08/16 C05099935

SECRET
SPECIAL HANDLING

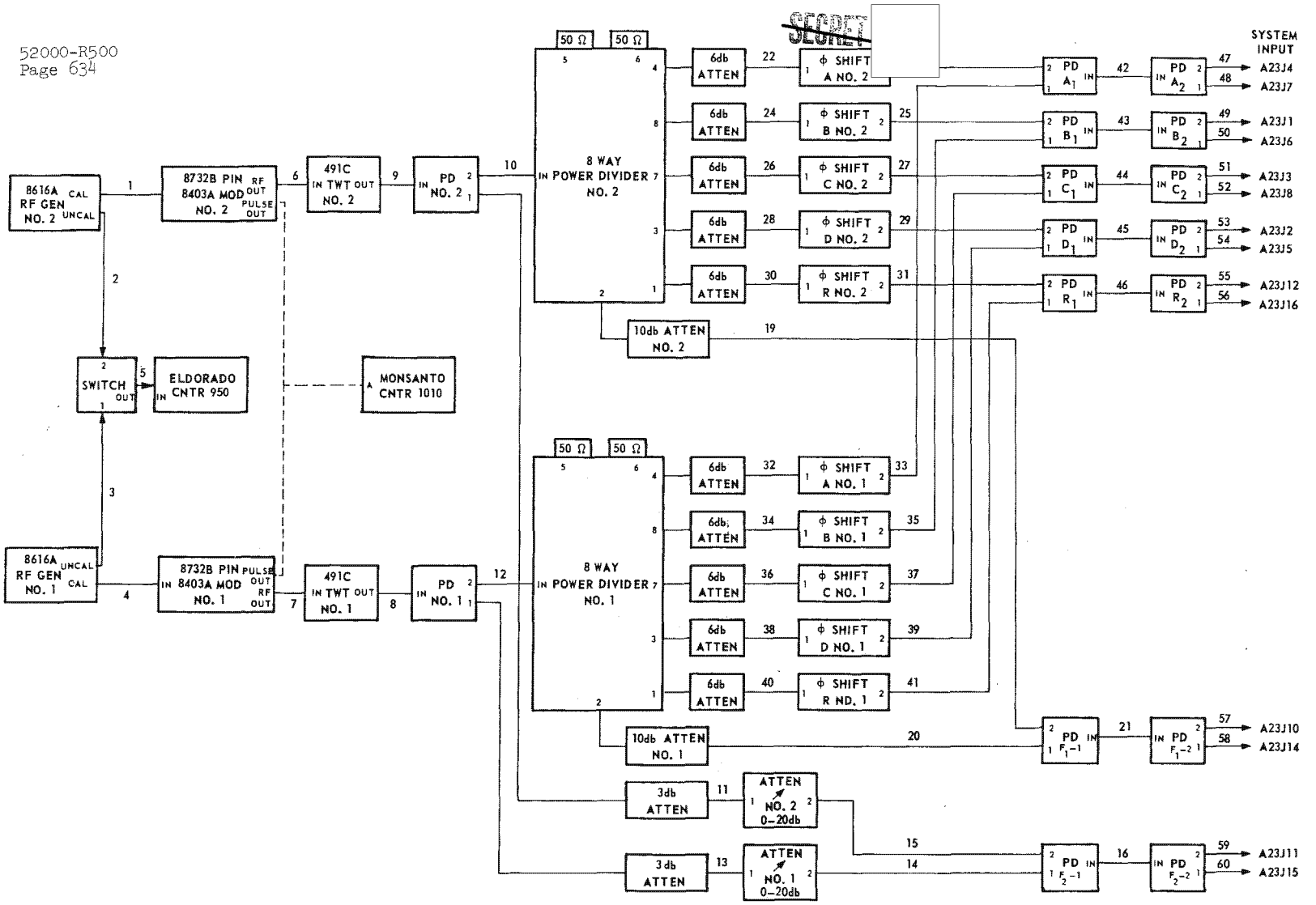


Figure 7.2-5. RF Path Diagram

SECRET
SPECIAL HANDLING

SECRET
SPECIAL HANDLING

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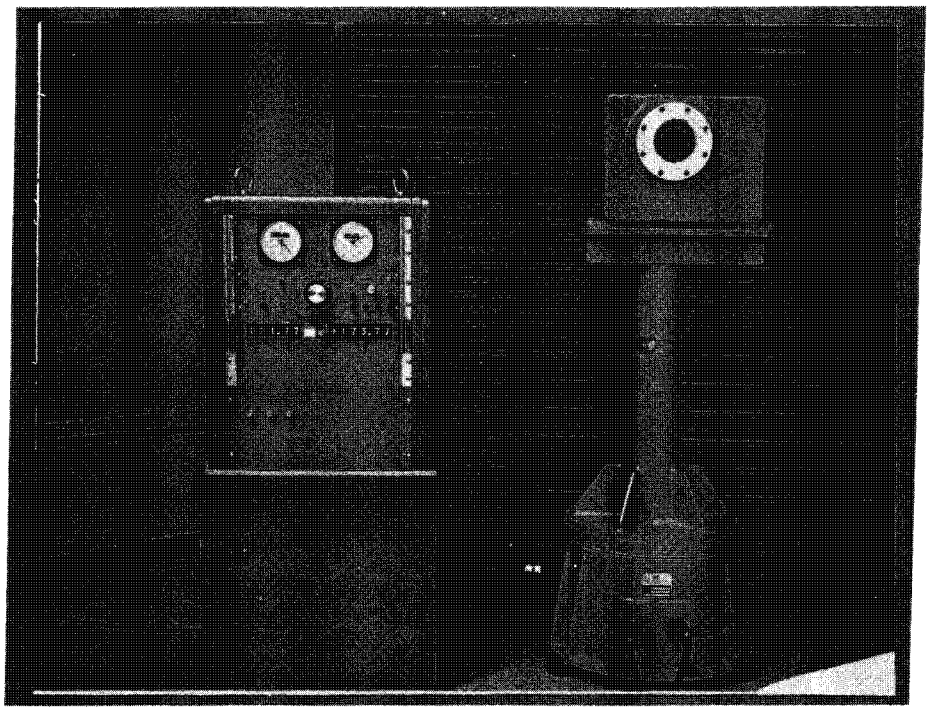

FIGURE 7.2-6 POSITIONER AND POSITIONER CONTROL

[redacted]m with respect to the signal source.

7.2.6 Holding Fixture

The Holding Fixture is shown in Figure 7.2-2.

7.3 GSE Specification

The Ground Support Equipment Specification is given in LTVE document 4124-11152.

7.4 Operation Description

The description of the Ground Support Equipment operation is given in the PLCO Operation Manual, LTVE document number 4124-11191.

7.5 PLCO Compatibility

The PLCO compatibility is demonstrated by testing the LTVE document number 4124-11192, Reaper PLCO Compatibility Test Procedure.